SPECTRUM DIGITAL INCORPORATED

XEVM642 4VSX35 Daughter Card

Technical Reference

2006 DSP Development Systems

XEVM642 4VSX35
Daughter Card
Technical Reference

508475--0001 Rev. A
June 2006

SPECTRUM DIGITAL, INC.
120502 Exchange Drive, #440 Stafford, TX. 77477
Tel: 281.494.4500 Fax: 281.494.5310
sales@spectrumdigital.com www.spectrumdigital.com

IMPORTANT NOTICE

Spectrum Digital, Inc. reserves the right to make changes to its products or to discontinue any product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

Spectrum Digital, Inc. warrants performance of its products and related software to current specifications in accordance with Spectrum Digital's standard warranty. Testing and other quality control techniques are utilized to the extent deemed necessary to support this warranty.

Please be aware that the products described herein are not intended for use in life-support appliances, devices, or systems. Spectrum Digital does not warrant nor is liable for the product described herein to be used in other than a laboratory development environment. Use in any other environment voids the warranty.

Spectrum Digital, Inc. assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does Spectrum Digital warrant or represent any license, either express or implied, is granted under any patent right, copyright, or other intellectual property right of Spectrum Digital, Inc. covering or relating to any combination, machine, or process in which such Digital Signal Processing development products or services might be or are used.

WARNING

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

TRADEMARKS

Windows 2000, and Windows XP are registered trademarks of Microsoft Corp.

4VSX35 is a trademark of Xilinx Inc.

Contents

About This Manual

This document describes the module level operations of the XEVM642 4VSX35 Daughter Card. This daughter card is designed to be used with the TMS320DM642 Evaluation Module designed by spectrum Digital.

Notational Conventions

This document uses the following conventions.

The XEVM642 4VSX35 Daughter Card will sometimes be referred to as the Daughter Card.

The TMS320DM642 Evaluation Module will sometimes be referred to as the EVM DM642 or the EVM.

Program listings, program examples, and interactive displays are shown is a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Xilinx 4VSX35 Data Sheet
Technical Reference, EVM DM642

Chapter 1

Introduction to the XEVM642 4VSX35 Daughter Card

This chapter provides you with a description of the XEVM642 Daughter Card along with the key features.

Topic **Page**

1.0 Overview of the XEVM642 4VSX35 Daughter Card

The XEVM642 4VSX35 Daughter Card is designed to be used with DM642 Evaluation Board designed by Spectrum Digital. By programming the FPGA the user can accelerate certain data processing functions thereby increasing the overall performance of the system

1.1 Key Features of the XEVM642 4VSX35 Daughter Card

The XEVM642 4VSX35 Daughter Card has the following features:

- Contains one Xilinx 4VSX35 FPGA
- Compatible with Spectrum Digital DM642 Evaluation Module.
- RS-232 Interface
- Multimedia Card Interface
- 6 User LEDs
- 3 System LEDS
- 8 Position DIP switch for user input
- 8 Position rotary switch for user input
- 5 Push button switches
- FPGA programming connector
- 13 Test points

1.2 Key Items on the XEVM642 4VSX35 Daughter Card

Figure 1-1 shows the top view of the XEVM642 4VSX35 Daughter Card. The key items identified are:

- Status LEDs
- DIP Switches
- Push Button Switches
- RS-232 DB9 connector
- Power supply connectors
- Rotary switch
- Memory Card Interface
- FPGA Programming connector
- Test Points

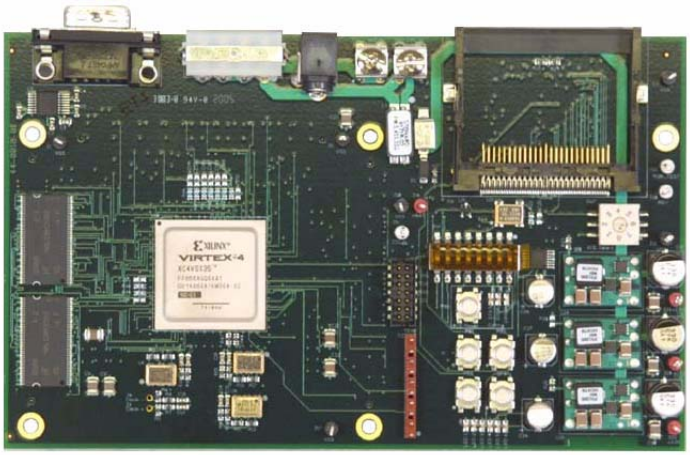


Figure 1-1, Top View XEVM642 4VSX35 Daughter Card

Figure 1-2 shows the bottom view of the XEVM642 4VSX35 Daughter Card. The key items identified are:

- Daughter Board Interface Connectors

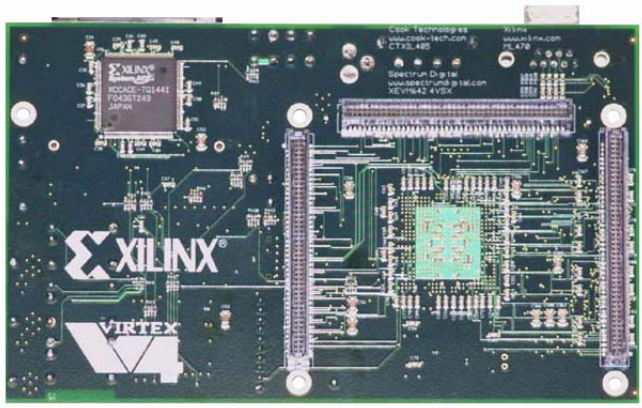


Figure 1-2, Bottom View XEVM642 4VSX35 Daughter Card

Chapter 2

Installing the XEVM642 4VSX35 Daughter Card

This chapter helps you install the XEVM642 4VSX35 Daughter Card on the EVM DM642.

Topic **Page**

2.1 What You'll Need

The following checklists detail items that are shipped with the XEVM642 4VSX35 Daughter Card and additional items you'll need to use these tools.

Hardware checklist

__	**Host**	An IBM PC/AT or 100% compatible PC or laptop with a hard-disk system and CD-ROM disk drive with a USB or Ethernet port
__	**Memory**	Minimum of 32MB
__	**Display**	Color VGA or LCD
__	**Target board**	Spectrum Digital DM642 EVM with power supply
__	**Daughter card**	XEVM642 4VSX35 Daughter Card with power supply
__	**JTAG emulator**	Spectrum Digital XDS510 USB JTAG Emulator
__	**FPGA Programmer**	Xilinx FPGA programming tool

Software checklist

__	**Operating system**	Win 2000, Win XP
__	**DSP software tools**	Compiler/assembler/linker for DSP
__	**Debugger**	Code Composer or Code Composer Studio
__	**Drivers**	Spectrum Digital drivers for TI Code Composer (available from Spectrum Digital's website)
__	**FPGA software tools**	Xilinx FPGA development tools for Virtrex 4 FPGA

2.2 Installing the XEVM642 4VSX35 Daughter Card

This section contains the steps for installing the XEVM642 4VSX35 Daughter Card on the EVM DM642.

WARNING !

Target Cable Connectors:

Be very careful with the target cable connectors. connect them gently; don't force them into position, or you may damage the connectors.

Do **not** connect or disconnect the 14-pin cable while the target system is powered up.

This section makes the assumption that the EVM DM642, Code Composer Studio, and the correct emulation drivers have been installed and that the DSP debug tool chain is operating correctly.

For more information regarding the DM642 EVM refer to the following support web page:

http://c6000.spectrumdigital.com/evmdm642/

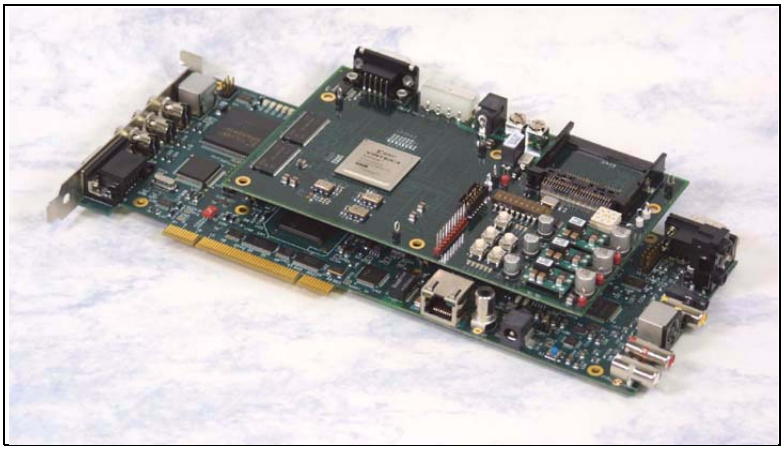
To install the XEVM642 4VSX35 Daughter Card onto the EVM DM642 execute the following checklist:

❏ Make sure the power to the EVM DM642 card is OFF.

❏ Make sure the power to the XEVM642 4VSX35 Daughter Card is OFF.

❏ Install the Xilinx FPGA development software on your PC or laptop computer.

❏ Mount the XEVM642 4VSX35 Daughter Card on the EVM DM642. This is shown in figure below.



❏ Connect the JTAG emulator to the EVM DM642.

❏ Connect the JTAG emulator to your PC or laptop.

❏ Connect the Xilinx FPGA programming device to the XEVM642 4VSX35 Daughter Card.

❏ Connect the Xilinx FPGA programming device to your PC or laptop.

CAUTION !

Be sure you use the +12V power supply with the XEVM642 Daughter Card.

❏ Provide power to the XEVM642 4VSX35 Daughter Card Driver via one of the power connectors described in chapter 3. If using a +12v power supply plug into an AC outlet.

CAUTION !

Be sure you use the +5V power supply with the DM642 EVM

❏ Attach the +5 volt power supply to the EVM DM642 and plug into an AC outlet.

❏ Download the DSP software via the JTAG emulator to the EVM DM642

❏ Download the FPGA logic to the XEVM642 4VSX35 Daughter Card

❏ Push the RESET push button switch (PB5, ACE RESET) on the XEVM642 4VSX35 Daughter Card

❏ Start executing the DSP code from Code Composer Studio

Chapter 3

Physical Description

This chapter describes the physical layout of the XEVM642 4VSX35 Daughter Card and its interfaces.

Topic **Page**

3.1 Board Layout

The XEVM642 4VSX35 Daughter Card is a 6.575 x 4.0 inch (167 x 101.6 mm.) multi-layer board which is powered by an external +5 volt only power supply. Figure 3-1 shows the connector and switch positions on the top side of the board.

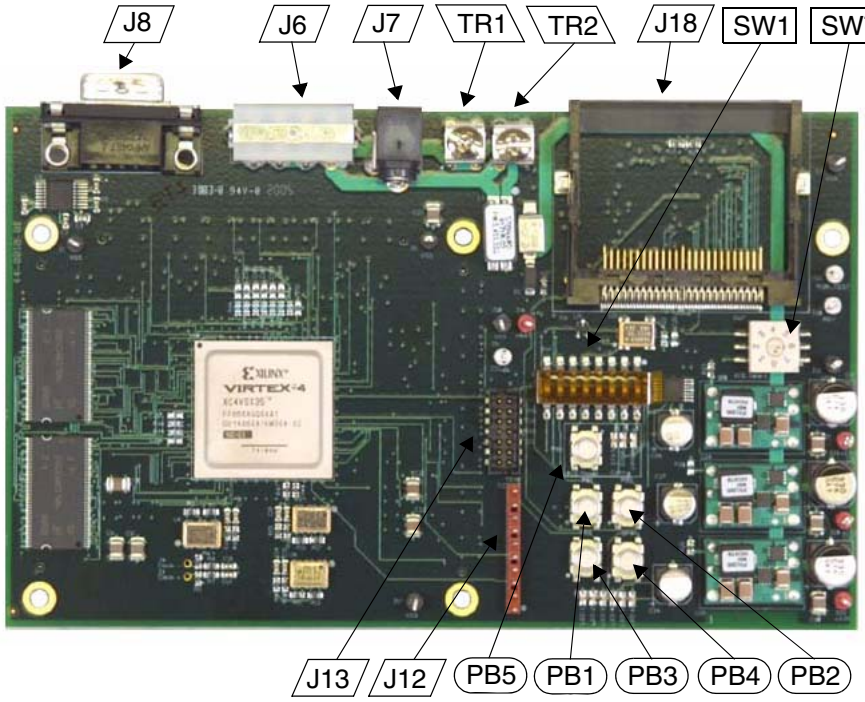


Figure 3-1, XEVM642 4VSX35 Daughter Card

Figure 3-2 shows the connectors positions on the bottom side of the XEVM642 4VSX35 Daughter Card.

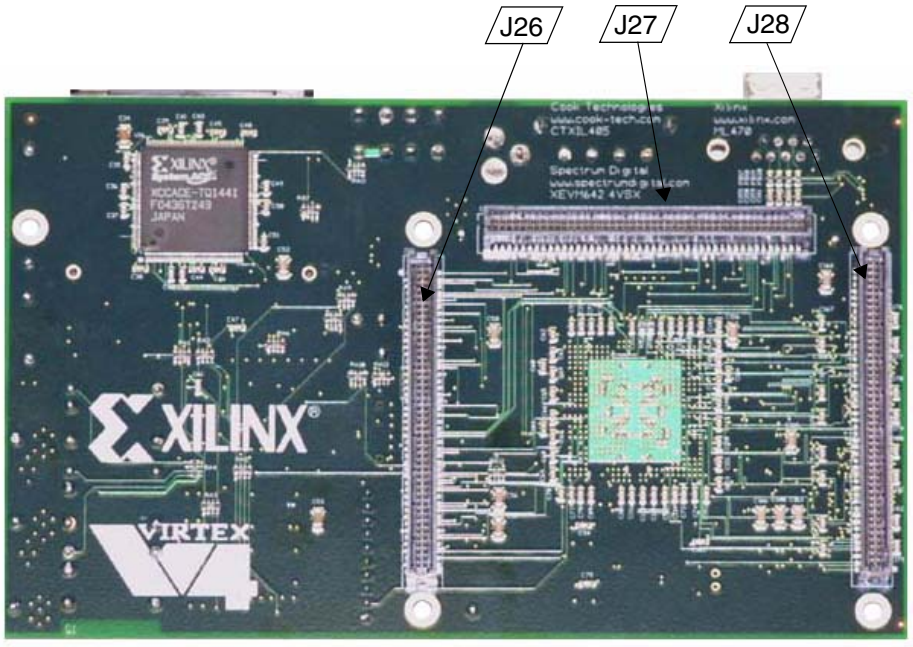


Figure 3-2, XEVM642 4VSX35 Daughter Card

3.2 Connector Index

The XEVM642 4VSX35 Daughter Card has 11 connectors. These connectors are listed in the table below.

Table 1: XEVM642 4VSX35 Daughter Card Connectors

Connector	# Pins	Function
J6	4	PC Power Supply Connector
J7	2	+12V Power Connector
J8	9	Male DB-9 Connector
J12	10	Test Connector
J13	14	FPGA Programming Connector
J18	2	MultiMedia Card Connector
J26		DM642 EVM DC_P1 Mating Connector
J27		DM642 EVM DC_P3 Mating Connector
J28		DM642 EVM DC_P2 Mating Connector
TR1	1	Ground In
TR2	1	+12V In

3.3 Power Connectors

The XEVM642 4VSX35 Daughter Card has 3 power connector interfaces. They are described in the following sections.

WARNING !
Only Use Power Connector interface at time.

3.3.1 J6, PC Power Supply Connector

This 4 pin male connector allows the use of a standard personal computer power supply to power the XEVM642 4VSX35 Daughter Card. The pin description for this connector is in the table below.

Table 2: J6, PC Power Supply Connector

Pin #	Voltage Level
1	+12 Volts
2	-12 Volts
3	Ground
4	+5 Volts

3.3.2 J7, +12V Power Connector

Power (+12 volts) is brought onto the XEVM642 4VSX35 Daughter Card via the J7 connector. The connector has an outside diameter of 5.5 mm. and an inside diameter of 2.5 mm. The A diagram of J5 is shown below.

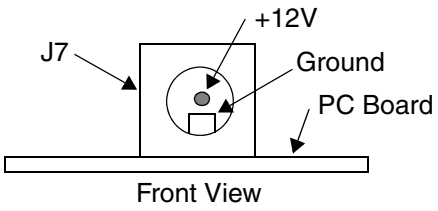


Figure 3-3, +12 Power Connector

3.3.3 TR1, TR2, Power Connectors

The TR1, TR2 connectors allow the user to connect external power supplies to the XEVM642 4VSX35 Daughter Card. The diagram below shows the TR1 and TR2 connectors from a card edge view.

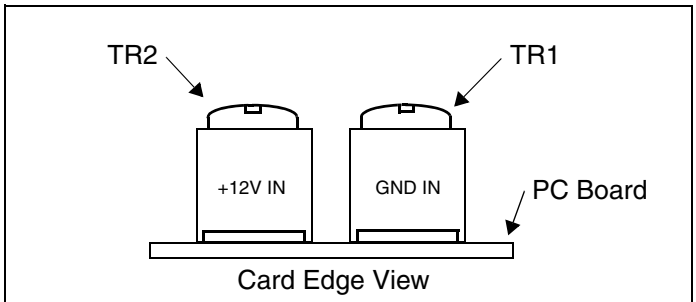


Figure 3-4, TR1, TR2 Power Connectors

3.4 J8, RS-232 Connector

The XEVM642 4VSX35 Daughter Card has a male DB9 connector. This connector interfaces to a MAX331 CAE. The pin positions for the J8 connector as viewed from the edge of the printed circuit board are shown below.

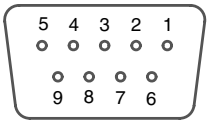


Figure 3-5, J8, DB9 Male Connector

The pin numbers and their corresponding signals are shown in the table below.

Table 3: J8, RS-232 Pinout

Pin #	Signal Name
1	No connect
2	RSORX
3	RSOTX
4	No Connect
5	GND
6	No Connect
7	RSORTS
8	RSOCTS
9	No Connect

3.5 J12, Test Connector

Connector J12 is a 1 x 10 test connector which brings out the FPGA test points. The pin numbers and their corresponding signals are shown in the table below.

Table 4: J12, Test Connector Pinout

Pin #	Signal Name
1	DBG_TP0
2	DBG_TP1
3	DBG_TP2
4	DBG_TP3
5	DBG_TP4
6	DBG_TP5
7	DBG_TP6
8	DBG_TP7
9	DBG_TP
10	DBG_TP09

3.6 J13, FPGA Programming Connector

Connector J13 is a 2 x 7 connector which allows the user to program the FPGA. The top view of the connector on the board is shown below is shown in the figure below.

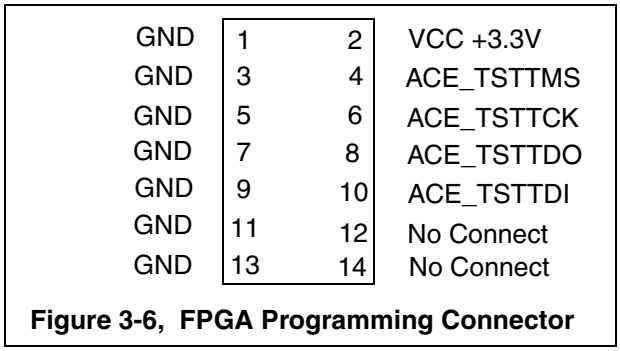


Figure 3-6, FPGA Programming Connector

The pin numbers and their corresponding signals are shown in the table below.

Table 5: J13, FPGA Programming Connector Pinout

Pin #	Signal Name	Pin #	Signal Name
1	GND	2	VCC +3.3V
3	GND	4	ACE_TSTTMS
5	GND	6	ACE_TSTTCK
7	GND	8	ACE_TSTTDO
9	GND	10	ACE_TSTTDI
11	GND	12	No Connect
13	GND	14	No Connect

3.7 J18, MultiMedia Card Connector

Connector J18 is a MultiMedia Card connector which allows the user to insert a MultiMedia Card into XEVM642 4VSX35 Daughter Card. The pinout for this connector is shown in the table below.

Table 6: J18, MultiMedia Card Connector

Pin #	Signal Name	Pin #	Signal Name
1	GND	2	D3
3	D4	4	D5
5	D6	6	D7
7	CE1#	8	A10
9	OE#	10	A9
11	A8	12	A7
13	Vcc, +3.3V	14	A6
15	A5	16	A4
17	A3	18	A2
19	A1	20	A0
21	D0	22	D1
23	D2	24	WP, No Connect
25	CD2#	26	CD1#
27	D11	28	D12
29	D13	30	D14
31	D15	32	CE2#
33	VS1#, No Connect	34	IORD#
35	IOWR#	36	WE#
37	RDY/BSY	38	Vcc, +3.3V
39	CSEL#	40	VS2#, No Connect
41	RESET	42	WAIT#
43	INPACK#, No Connect	44	REG#
45	BVD2, No Connect	46	BVD1,No Connect
47	D8	48	AFD9
49	D10	50	GND

3.8 DM642 EVM Mating Connectors

The XEVM642 4VSX35 Daughter Card has 3 male connectors, (J26, J27, J28), on the bottom side of the board that mate the female expansion connectors on the EVM DM642 board. Figure 3-2 shows the location of these connectors. The next 3 sections describe the signals on each connector.

3.8.1 J26, DM642 EVM DC_P1 Mating Connector

Table 7: J26, DM642 EVM DC_P1 Mating Connector

Pin	Signal	Description	Pin	Signal	Description
1	RESET#	Reset	2	CAPTURE1_EN#	Disable On Board Capture 1
3	AUDIO_EN#	Disable On Board Audio	4	CAPTURE2_EN#	Disable On Board Capture 2
5	GND	System Ground	6	GND	System Ground
7	VP0D0	Video Port 0 D0	8	VP0D1	Video Port 0 D1
9	VP0D2	Video Port 0 D2	10	VP0D3	Video Port 0 D3
11	GND	System Ground	12	GND	System Ground
13	VP0D4	Video Port 0 D4	14	VP0D5	Video Port 0 D5
15	VP0D6	Video Port 0 D6	16	VP0D7	Video Port 0 D7
17	VP0D8	Video Port 0 D8	18	VP0D9	Video Port 0 D9
19	GND	System Ground	20	GND	System Ground
21	VP0D10	Video Port 0 D10	22	VP0D11	Video Port 0 D11
23	VP0D12	Video Port 0 D12	24	VP0D13	Video Port 0 D 13
25	GND	System Ground	26	GND	System Ground
27	VP0D14	Video Port 0 D14	28	VP0D15	Video Port 0 D15
29	VP0D16	Video Port 0 D16	30	VP0D17	Video Port 0 D17
31	VP0D18	Video Port 0 D18	32	VP0D19	Video Port 0 D 19
33	GND	System Ground	34	GND	System Ground
35	VP0CTL2	Video Port 0 Control 2	36	GND	System Ground
37	GND	System Ground	38	VP0CTL0	Video Port 0 Control 0
39	VP0CTL1	Video Port 0 Control 1	40	GND	System Ground
41	GND	System Ground	42	GND	System Ground
43	GND	System Ground	44	VP0CLK1	Video Port 0 Clock 1
45	VP0CLK0	Video Port 0 Clock 0	46	GND	System Ground
47	GND	System Ground	48	GND	System Ground
49	GND	System Ground	50	VP1CLK1	Video Port 1 Clock 1
51	VP1CLK0	Video Port 1 Clock 0	52	GND	System Ground
53	GND	System Ground	54	VP1CTL0	Video Port 0 Control 0
55	VP01CTL2	Video Port 0 Control 1	56	GND	System Ground
57	GND	System Ground	58	VP1CTL1	Video Port 1 Control 1
59	GND	System Ground	60	GND	System Ground
61	VP1D18	Video Port 1 D18	62	VP1D19	Video Port 1 D19
63	VP1D16	Video Port 1 D16	64	VP1D17	Video Port 1 D17
65	VP1D14	Video Port 1 D14	66	VP1D15	Video Port 1 D15
67	GND	System Ground	68	GND	System Ground
69	VP1D12	Video Port 1 D12	70	VP1D13	Video Port 1 D13
71	VP1D10	Video Port 1 D10	72	VP1D11	Video Port 1 D11
73	GND	System Ground	74	GND	System Ground
75	VP1D8	Video Port 1 D8	76	VP1D9	Video Port 1 D9
77	VP1D6	Video Port 1 D6	78	VP1D7	Video Port 1 D7
79	VP1D4	Video Port 1 D4	80	VP1D5	Video Port 1 D5
81	GND	System Ground	82	GND	System Ground
83	VP1D2	Video Port 1 D2	84	VP1D3	Video Port 1 D3
85	VP1D0	Video Port 1 D0	86	VP1D1	Video Port 1 D1
87	GND	System Ground	88	GND	
89	DCARD_STCLK		90	GND	

3.8.2 J27, DM642 EVM DC_P3 Mating Connector

Table 8: J27, DM642 EVM DC_P3 Mating Connector

Pin	Signal	Description	Pin	Signal	Description
1	GND	System Ground	2	GND	System Ground
3	ED31	EMIF Data D31	4	ED30	EMIF Data D30
5	ED29	EMIF Data D29	6	ED28	EMIF Data D28
7	ED27	EMIF Data D27	8	ED26	EMIF Data D26
9	ED25	EMIF Data D25	10	ED24	EMIF Data D24
11	GND	System Ground	12	GND	System Ground
13	ED23	EMIF Data D23	14	ED22	EMIF Data D22
15	ED21	EMIF Data D21	16	ED20	EMIF Data D20
17	ED19	EMIF Data D19	18	ED18	EMIF Data D18
19	ED17	EMIF Data D17	20	ED16	EMIF Data D16
21	GND	System Ground	22	GND	System Ground
23	ED15	EMIF Data D15	24	ED14	EMIF Data D14
25	ED13	EMIF Data D13	26	ED12	EMIF Data D12
27	ED11	EMIF Data D11	28	ED10	EMIF Data D10
29	ED9	EMIF Data D9	30	ED8	EMIF Data D8
31	GND	System Ground	32	GND	System Ground
33	ED7	EMIF Data D7	34	ED6	EMIF Data D6
35	ED5	EMIF Data D5	36	ED4	EMIF Data D4
37	ED3	EMIF Data D3	38	ED2	EMIF Data D2
39	ED1	EMIF Data D1	40	ED0	EMIF Data D0
41	GND	System Ground	42	GND	System Ground
43	Reserved		44	ECLKOUT2	EMIF CLKOUT2
45	GND	System Ground	46	GND	System Ground
47	EBE3#	EMIF Byte Strobe	48	EBE2#	EMIF Byte Strobe2
49	EBE1#	EMIF Byte Strobe1	50	EBE0#	EMIF Byte Strobe0
51	GND	System Ground	52	GND	System Ground
53	ECE3#	EMIF Chip Enable 3	54	ECE2#	EMIF Chip Select 2
55	GND	System Ground	56	GND	System Ground
57	ECAS#	EMIF Read Strobe	58	ERAS#	EMIF Output Enable
59	EWE#	EMIF Write Strobe	60	EARDY	EMIF Ready
61	GND	System Ground	62	GND	System Ground
63	EA22	EMIF Address A22	64	EA21	EMIF Address A21
65	EA20	EMIF Address A20	66	EA19	EMIF Address A19
67	EA18	EMIF Address A18	68	EA17	EMIF Address A17
69	EA16	EMIF Address A16	70	EA15	EMIF Address A15
71	GND	System Ground	72	GND	System Ground
73	EA14	EMIF Address A14	74	EA13	EMIF Address A13
75	EA12	EMIF Address A12	76	EA11	EMIF Address A11
77	EA10	EMIF Address A10	78	EA9	EMIF Address A9
79	GND	System Ground	80	GND	System Ground
81	EA8	EMIF Address A8	82	EA7	EMIF Address A7
83	EA6	EMIF Address A6	84	EA5	EMIF Address A5
85	EA4	EMIF Address A4	86	EA3	EMIF Address A3
87	GND	System Ground	88	GND	System Ground
89	Reserved		90	Reserved	

3.8.3 J28, DM642 EVM DC_P2 Mating Connector

Table 9: 3.6.3 J28, DM642 EVM DC_P2 Mating Connector

Pin	Signal	Description	Pin	Signal	Description
1	GPIO3	DSP GPIO3	2	GPIO4	DSP Interrupt 4
3	GND	System Ground	4	GPIO5	DSP Interrupt 5
5	NMI	DSP NMI Interrupt	6	GND	System Ground
7	GND	System Ground	8	TINP1	DSP Timer In 1
9	TINP0	DSP Timer In 0	10	TOUT1	DSP Timer Out 1
11	TOUT0	DSP Timer Out 0	12	GND	System Ground
13	GND	System Ground	14	DISPLAY_EN#	Disable On Board Display
15	VP2CLK1	Video Port 2 Clock 1	16	GND	System Ground
17	GND	System Ground	18	GND	System Ground
19	VP2D18	Video Port 2 D18	20	VP2D19	Video Port 2 D19
21	VP2D16	Video Port 2 D16	22	VP2D17	Video Port 2 D17
23	VP2D14	Video Port 2 D14	24	VP2D15	Video Port 2 D15
25	GND	System Ground	26	GND	System Ground
27	VP2D12	Video Port 2 D12	28	VP2D13	Video Port 2 D13
29	VP2D10	Video Port 2 D10	30	VP2D11	Video Port 2 D11
31	GND	System Ground	32	GND	System Ground
33	VP2D8	Video Port 2 D8	34	VP2D9	Video Port 2 D9
35	VP2D6	Video Port 2 D6	36	VP2D7	Video Port 2 D7
37	VP2D4	Video Port 2 D4	38	VP2D5	Video Port 2 D5
39	GND	System Ground	40	GND	System Ground
41	VP2D2	Video Port 2 D2	42	VP2D3	Video Port 2 D3
43	VP2D0	Video Port 2 D0	44	VP2D1	Video Port 2 D1
45	GND	System Ground	46	GND	System Ground
47	VP2CLK0	Video Port 2 Clock 0	48	GND	System Ground
49	GND	System Ground	50	GND	System Ground
51	VP2CTL0	Video Port 2 Control 0	52	VP2CTL1	Video Port 2 Control 1
53	VP2CTL2	Video Port 2 Control 2	54	GND	System Ground
55	GND	System Ground	56	GND	System Ground
57	SCL	I^2C Clock	58	USER_GPIO_7	FPGA User I/O 7
59	SDA	I^2C Data	60	USER_GPIO_6	FPGA User I/O 6
61	GND	System Ground	62	GND	System Ground
63	USER_GPIO_4	FPGA User I/O 4	64	USER_GPIO_5	FPGA User I/O 5
65	USER_GPIO_2	FPGA User I/O 2	66	USER_GPIO_3	FPGA User I/O 3
67	USER_GPIO_0	FPGA User I/O 0	68	USER_GPIO_1	FPGA User I/O 1
69	GND	System Ground	70	GND	System Ground
71	GND	System Ground	72	GND	System Ground
73	Reserved		74	Reserved	
75	Reserved		76	Reserved	
77	Reserved		78	Reserved	
79	GND	System Ground	80	GND	System Ground
81	GND	System Ground	82	GND	System Ground
83	GND	System Ground	84	GND	System Ground
85	Reserved		86	Reserved	
87	Reserved		88	Reserved	
89	Reserved		90	Reserved	

3.9 User LEDs

The XEVM642 4VSX35 Daughter Card provides 6 LEDs which allow the user to provide visual feedback out of the FPGA. The position of these LEDs are shown in the figure below.

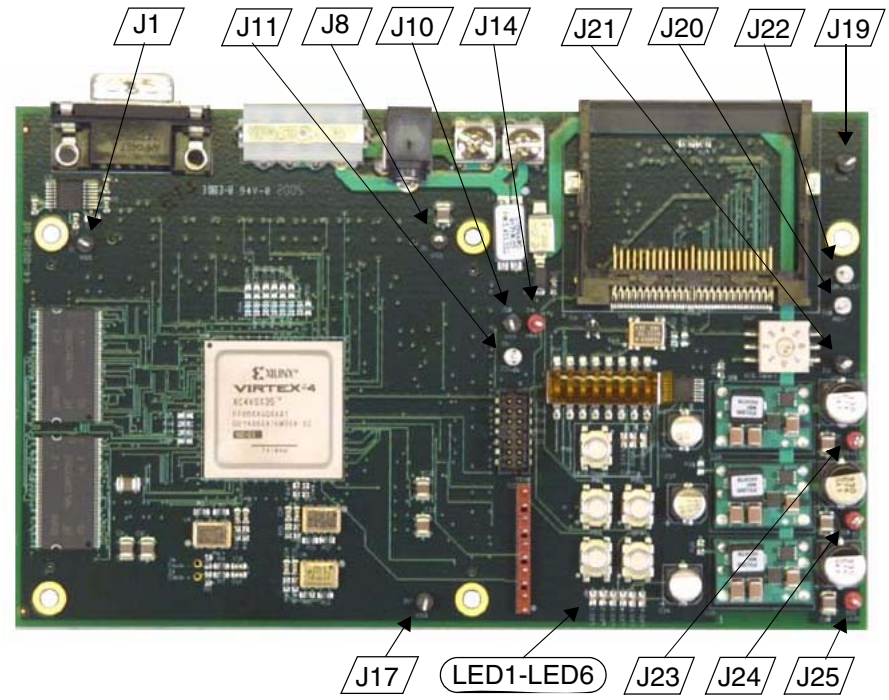


Figure 3-1, XEVM642 4VSX35 Daughter Card

The table below shows the user LEDs and the FPGA signal they are associated with.

Table 10: User LEDs

Reference Designator	Color	FPGA Signal
LED1	Green	LEDIN13
LED2	Green	LEDIN7
LED3	Green	LEDIN8
LED4	Green	LEDIN9
LED5	Green	LEDIN10
LED6	Green	LEDIN11

3.10 System LEDs

The XEVM642 4VSX35 Daughter Card has 3 system LEDs which reflect the status of programming the FPGA. These function of each LED is shown in the table below.

Table 11: System LEDs

Reference Designator	Color	LED Name
DS3	Green	LEDRSTAT
DS6	Green	LEDRDONE
DS7	Red	LEDERR

3.11 Switches

The XEVM642 4VSX35 Daughter Card has 3 types of switches; an 8 position DIP switch, 5 push button switches, and a rotary switch. The location of these switches on the board is indicated in figure 3-2. The following 3 sections describe these switches.

3.11.1 User DIP Switch

Switch SW1 is an 8 position DIP switch. Each position is connected directly to the FPGA. The signal each position is associated with is shown in the table below. programming the FPGA.

Table 12: User DIP Switch

SW1 Position	FPGA Signal
1	SW0
2	SW1
3	SW2
4	SW3
5	SW4
6	SW5
7	SW6
8	SW7

3.11.2 Push Button Switches

The XEVM642 4VSX35 Daughter Card has 5 push button momentary switches. Each switch is connected directly to the FPGA. The FPGA signal each switch is associated with is shown in the table below.

Table 13: Push Button Switches

Schematic Switch Name	Silkscreen Switch Name
SW8	PB1
SW9	PB2
SW10	PB3
SW11	PB4
ACE_RSTn	PB5

3.11.3 Rotary Switch

Rotary switch SW7 has 8 positions (marked 0-7) which are binary encoded into FPGA signals CFGA0, CFGA1, and CFGA2.

3.12 Test Points

The XEVM642 4VSX35 Daughter Card has thirteen (13) scope hook-probe test points. Their positions are shown in figure 3-7. The test points are shown in the table below along with the signals that are present on each test point.

Table 14: Test Points

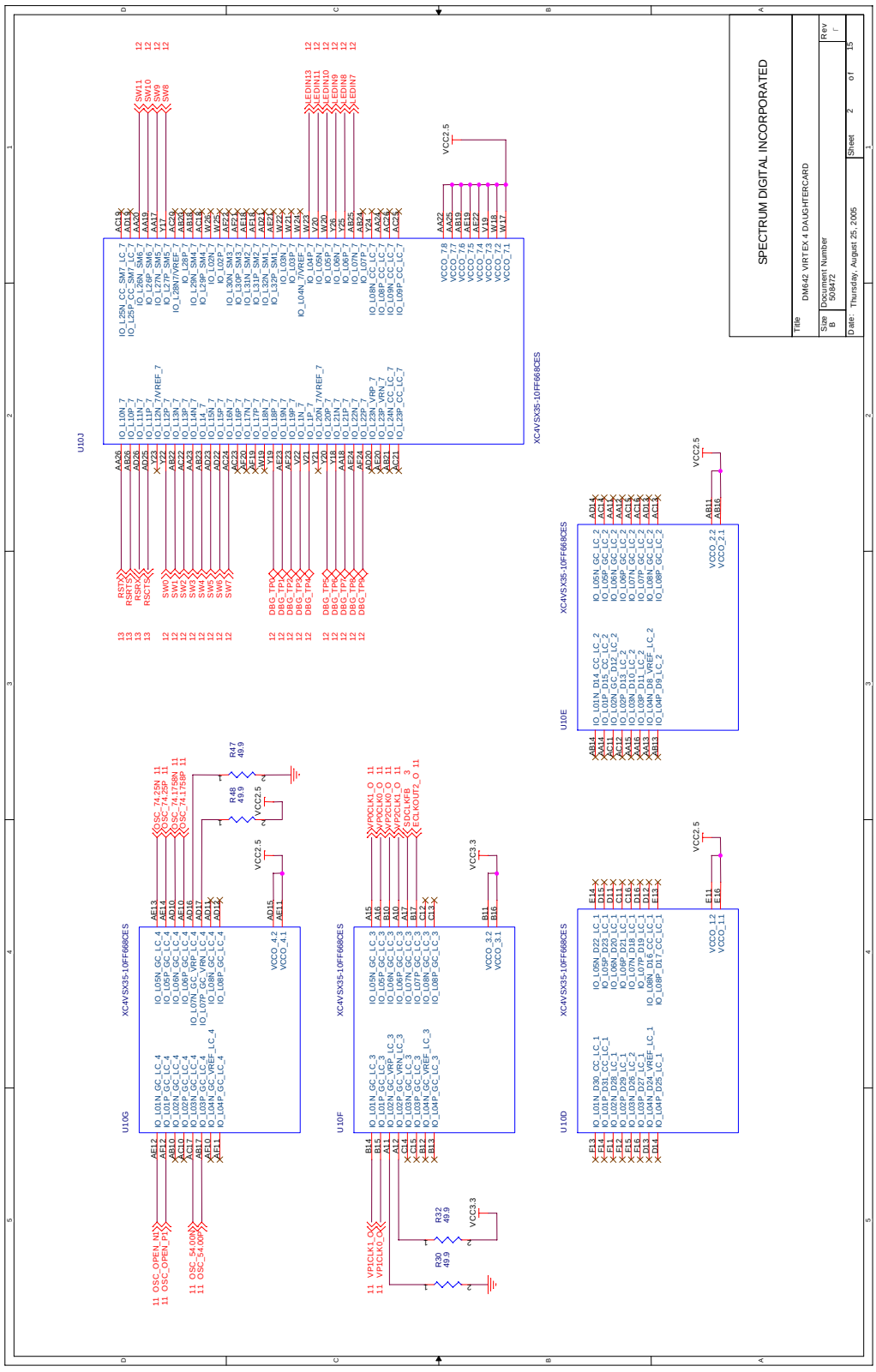
Test Point Name	Signal
J1	Vss
J8	Vss
J17	Vss
J10	Vss
J11	CCLK
J14	VBAT
J19	Vss
J20	RDY
J21	Vss
J22	POR_TEST
J23	+2.5V
J24	+1.5V
J25	+3.3V

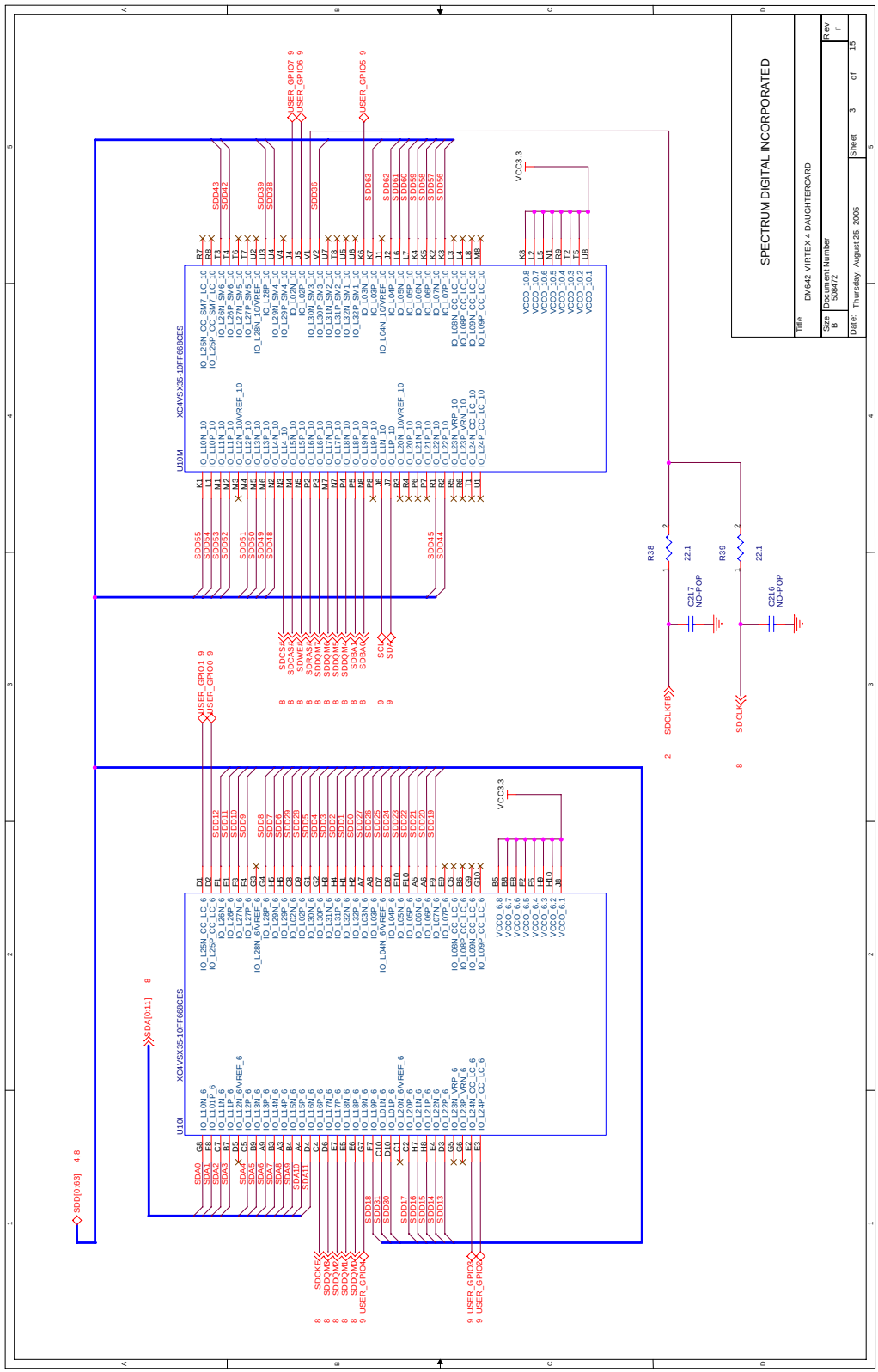
Appendix A

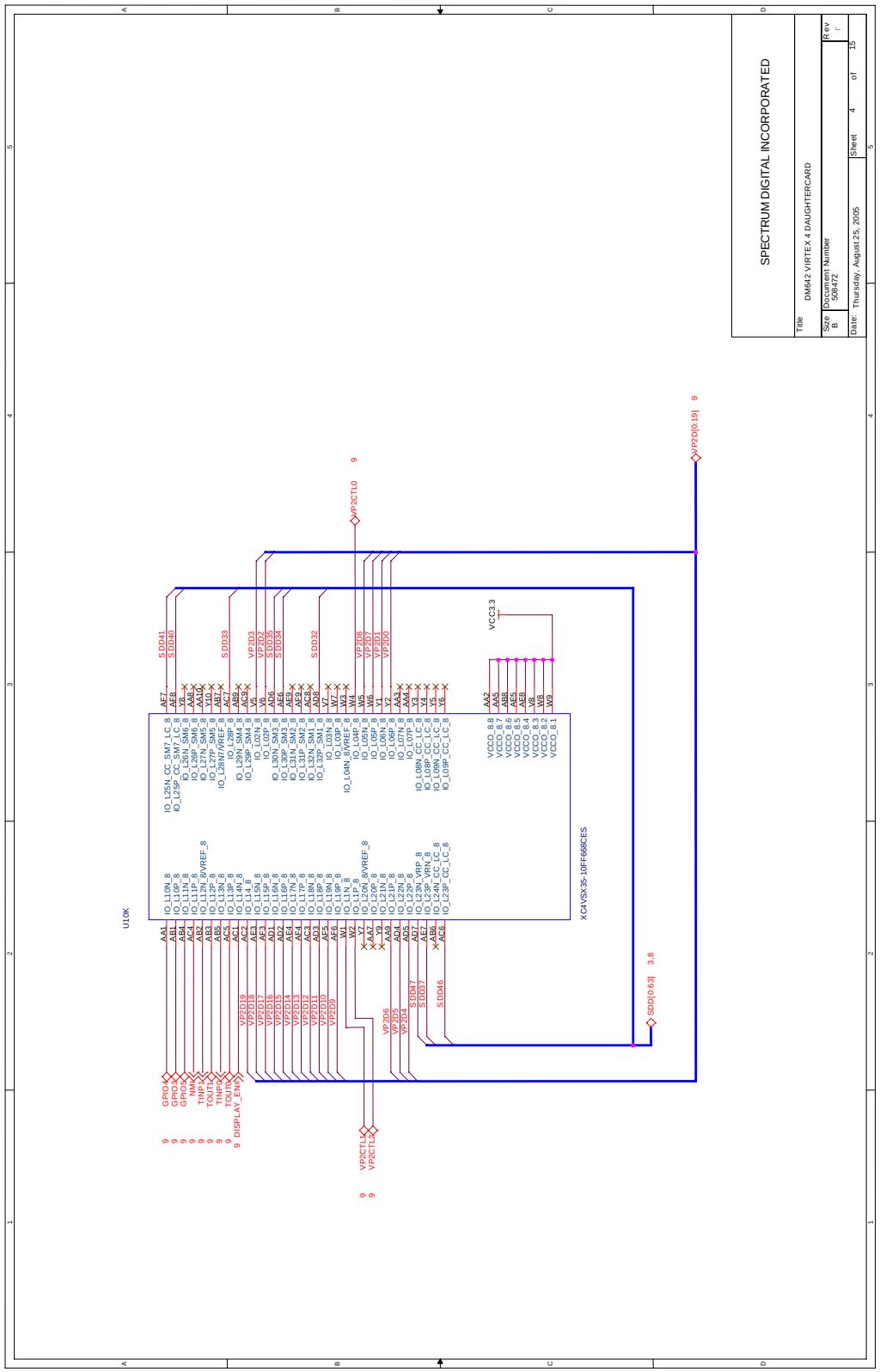
Schematics

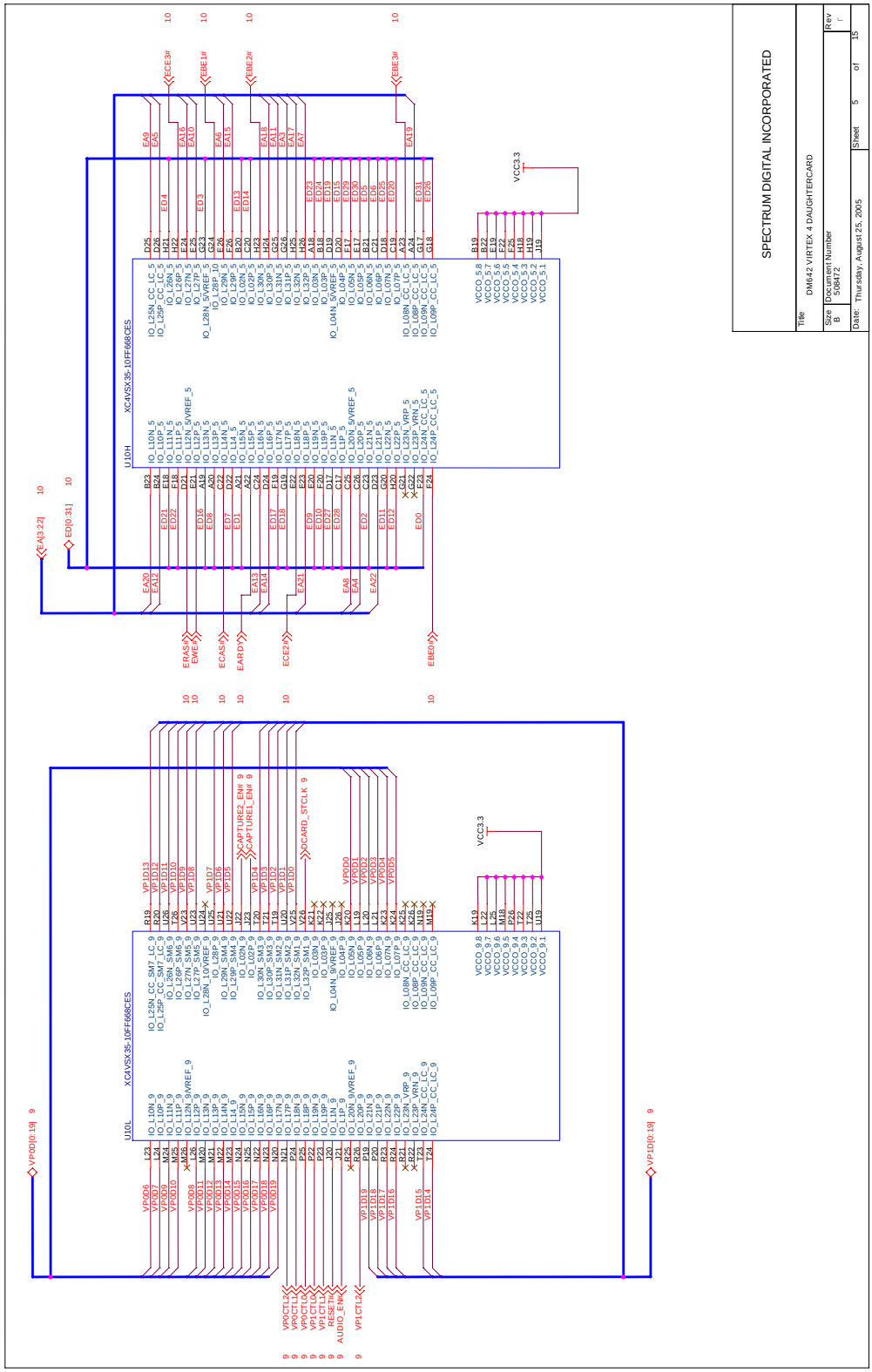
This appendix contains the schematics for the XEVM642 4VSX35 Daughter Card.

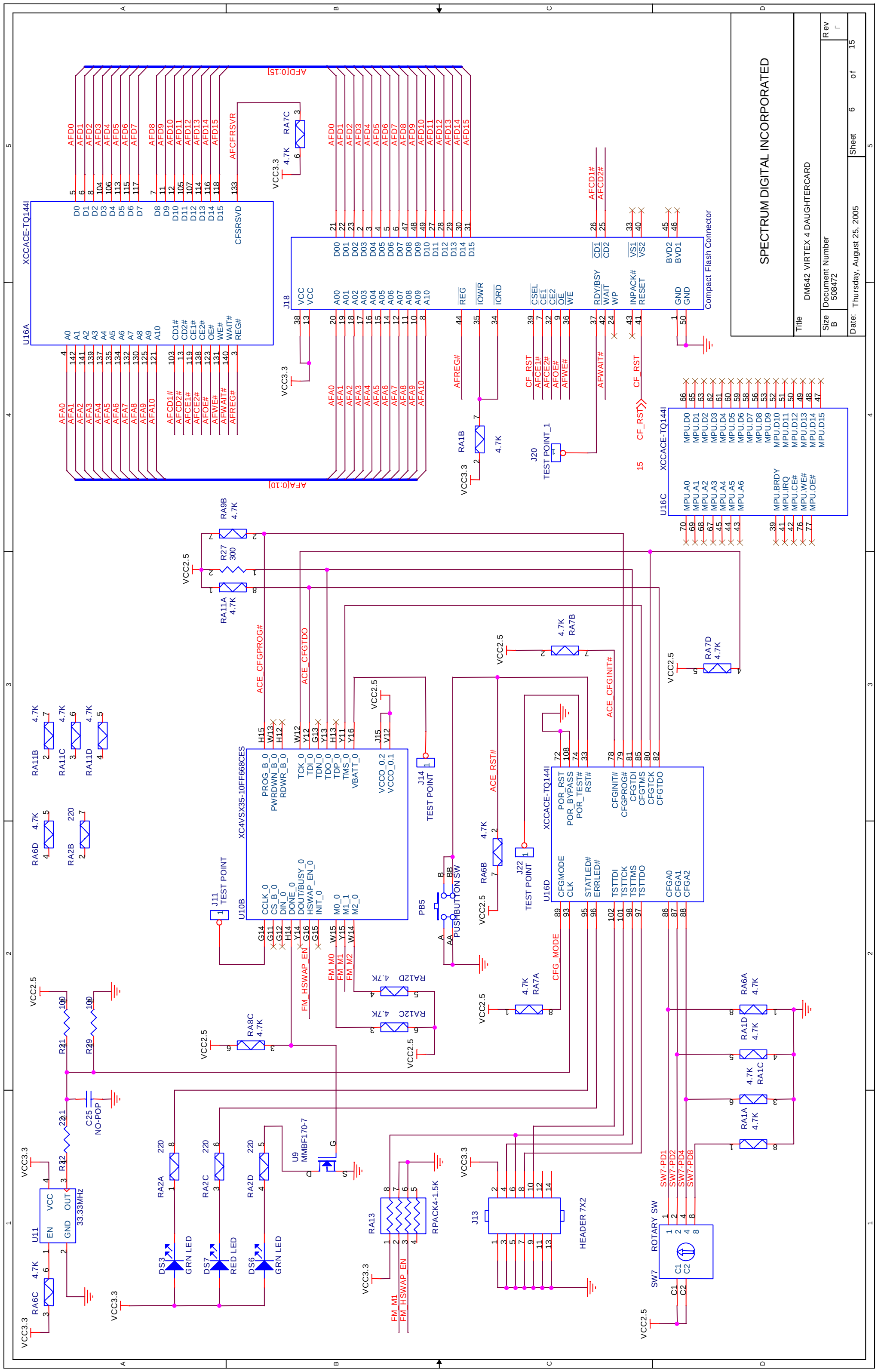
REV
DESCRIPTION
DATE
APPROVED
A
Initial schematic ready for layout.
04/01/05
RRP
NOTES, UNLESS OTHERWISE SPECIFIED:
1. RESISTANCE VALUES IN OHMS.
2. CAPACITANCE VALUES IN MICROFARADS.
3. ALL 0.1 uF AND 0.01uF CAPACITORS ARE DECOUPLING CAPS UNLESS OTHERWISE NOTED. THEY ARE SHOWN ON THE PAGE WITH THE INTEGRATED CIRCUITS THEY SHOULD BE PLACED NEAR.
SCHEMATIC INDEX
01 TITLE - Notes and Contents
02 FPGA 1
03 FPGA 2
04 FPGA 3
05 FPGA 4
06 FPGA CONFIG
07 FPGA POWER
08 SDRAM
09 DAUGHTERCARD CONNECTORS
10 EMIF DAUGHTERCARD CONNECTOR
11 USER SWITCHES LED
12 RS232 Buffers
13 CLOCKS
14 DECOUPLING CAPACITORS
15 POWER SUPPLY
REVISION STATUS OF SHEETS
DWN R. R. P. 04/01/2005
CHK T. W.K. 04/01/2005
ENGR R. R. P. 04/01/2005
ENGR MGR R. R. P. 04/01/2005
QA C. M.D. 04/01/2005
MFG R. R. P. 04/01/2005
APPROVALS R. R. P. 04/01/2005
NEXT ASSY USED ON
APPLICATION
SPECTRUM DIGITAL INCORPORATED
Title DM642 VIRTEX 4 DAUGHTERCARD
Size B
Document Number 508472
Rev F
Date: Thursday, August 25, 2005
Sheet 1 of 15

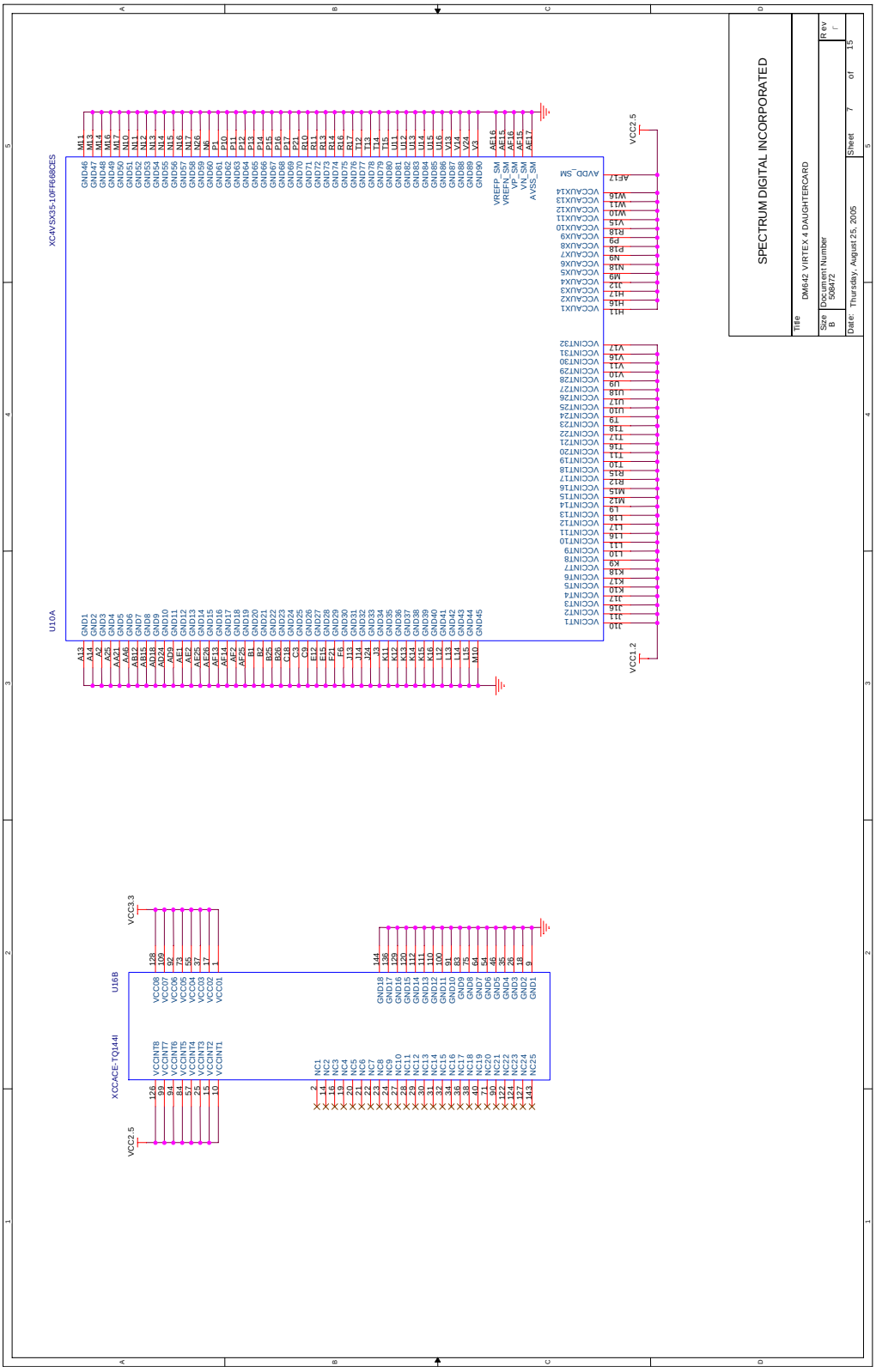

SPECTRUM DIGITAL INCORPORATED
Title
DM642 VIRTEX 4 DAUGHTERCARD
Size
B
Document Number
503472
Rev
F
Date: Thursday, August 25, 2005
Sheet 2 of 15
U10J
XC4VSX35-10FF668CES
U10G
U10F
U10E
U10D
VCC2.5
VCC3.3
R47 49.9
R48 49.9
R30 49.9
R32 49.9

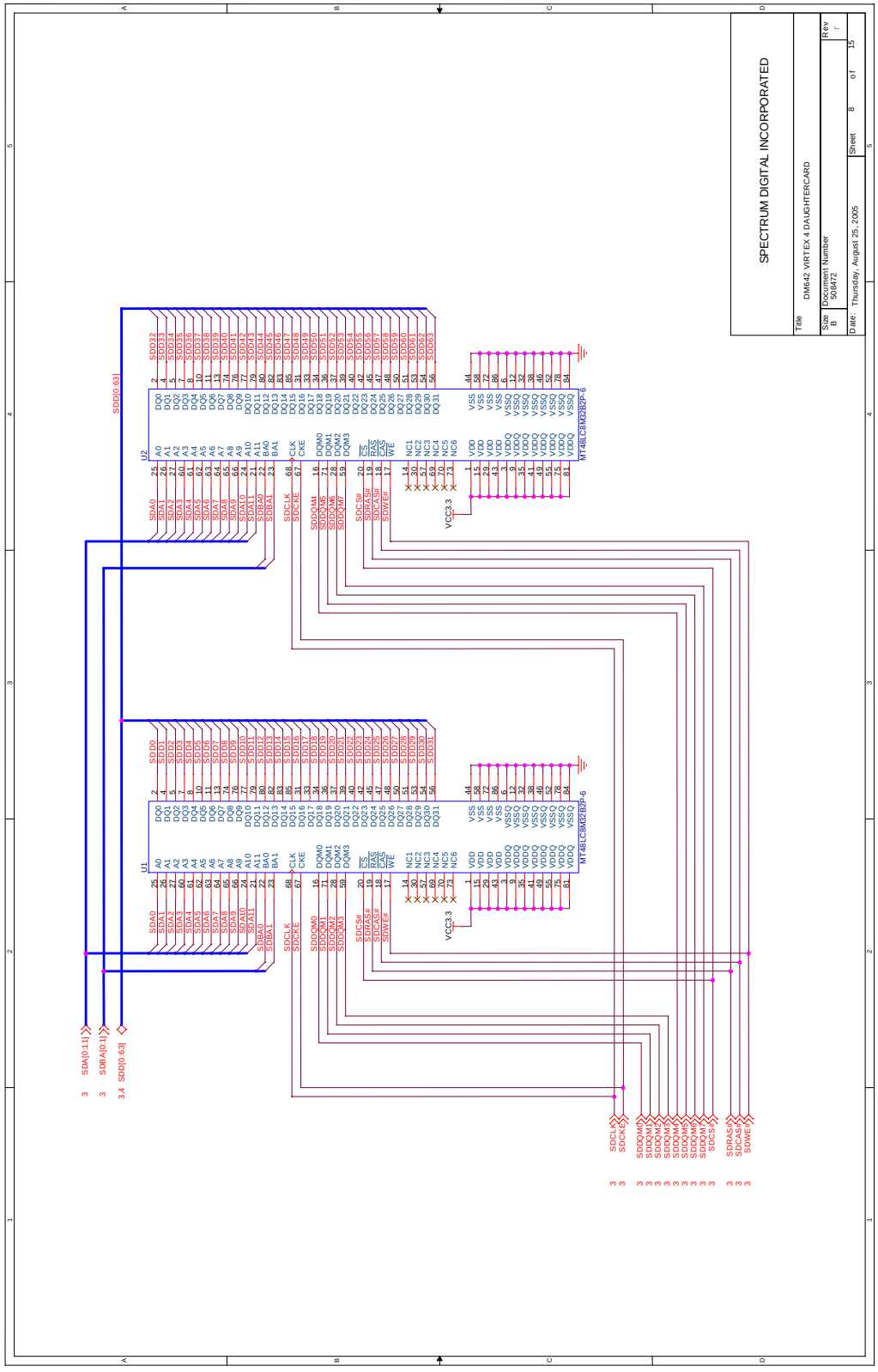

SPECTRUM DIGITAL INCORPORATED
Title DM642 VIRTEX 4 DAUGHTERCARD
Size B
Document Number 508472
Rev F
Date: Thursday, August 25, 2005
Sheet 3 of 15
U10M XC4VSX35-10FF668CES
U10I XC4VSX35-10FF668CES
R38 22.1
R39 22.1
C217 NO-POP
C216 NO-POP
VCC3.3
SDCLKFB
SDCLK

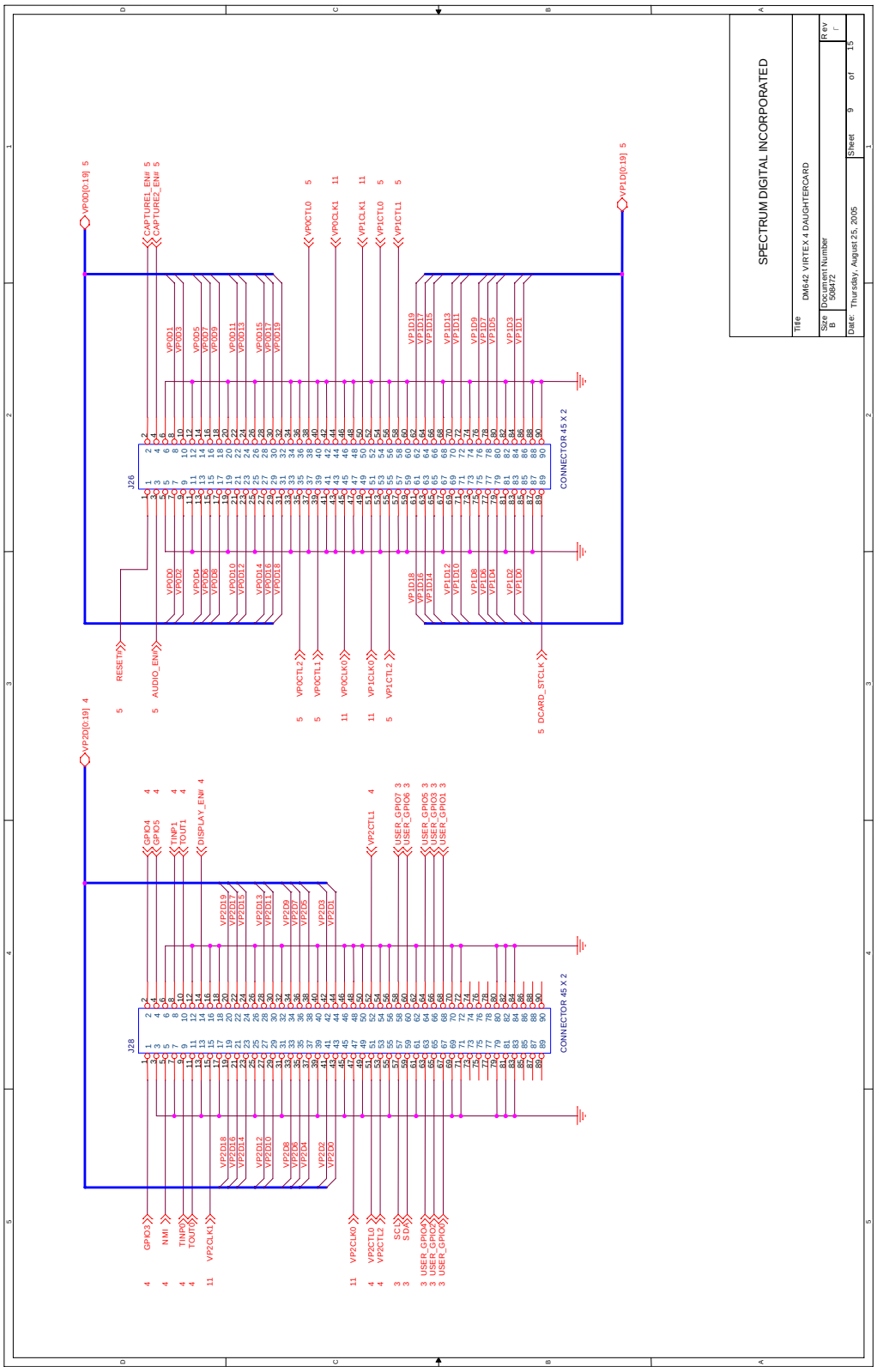

SPECTRUM DIGITAL INCORPORATED
Title
DM642 VIRTEX 4 DAUGHTERCARD
Size B
Document Number 508472
Rev F
Date: Thursday, August 25, 2005
Sheet 4 of 15
U10K
XC4VSX35-10FF668CES
VP2CTL0
VP2D[0:19]
SDD[0:63]
VCC3.3
DISPLAY_ENA
GPIO4
GPIO3
GPIO2
NMI
TINP1
TOUT1
TINP0
TOUT0
VP2CTL1
VP2CTL2

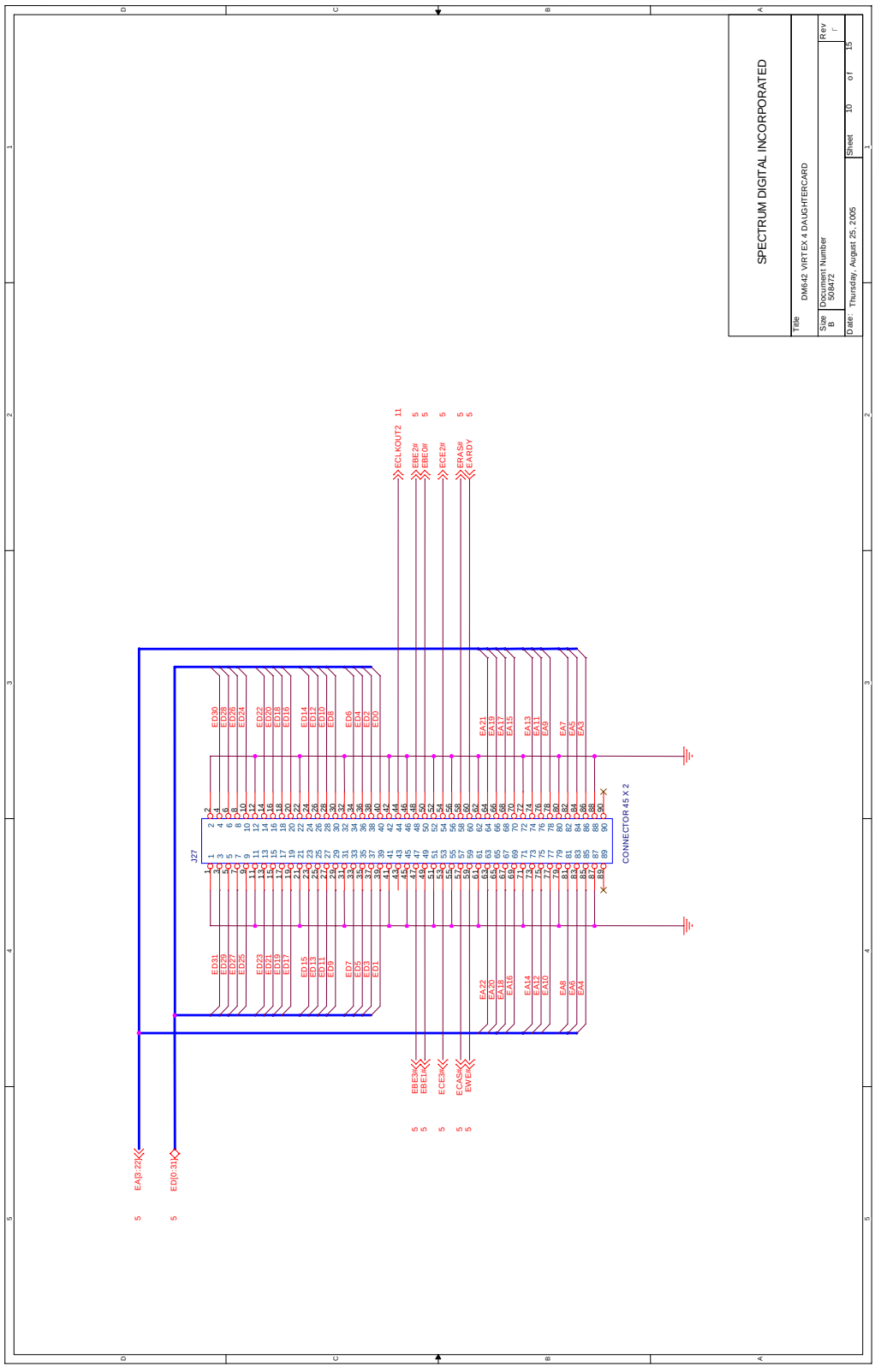

SPECTRUM DIGITAL INCORPORATED
Title
DM642 VIRTEX 4 DAUGHTERCARD
Size
B
Document Number
508472
Rev
Date: Thursday, August 25, 2005
Sheet 5 of 15
U10L XC4VSX35-10FF668CES
U10H XC4VSX35-10FF668CES
VP0D[0:19]
VP1D[0:19]
ED[0:31]
EA[3:22]
VCC3.3
ECE2#
EARD#
ECAS#
ERAS#
EWE#
EBE0#
EBE1#
EBE2#
EBE3#
ECE3#
CAPTURE2_EN# 9
CAPTURE1_EN# 9
XCARD_STCLK 9
VP0CTL2
VP0CTL1
VP0CTL0
VP1CTL2
VP1CTL1
VP1CTL0
RESET#
AUDIO_EN#
VP1CTL2

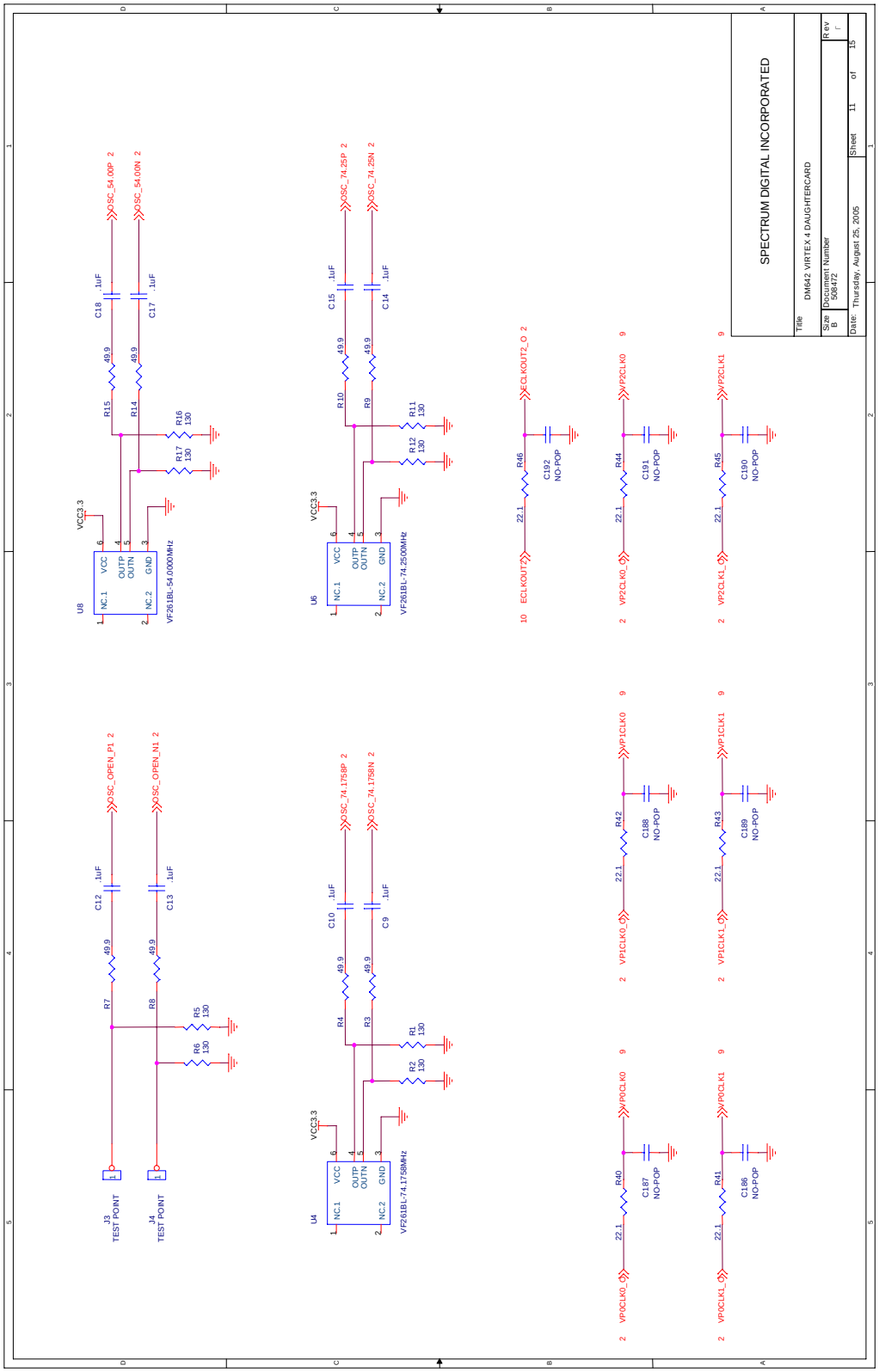

SPECTRUM DIGITAL INCORPORATED
Title
DM642 VIRTEX 4 DAUGHTERCARD
Size
B
Document Number
508472
Rev
F
Date: Thursday, August 25, 2005
Sheet 6 of 15

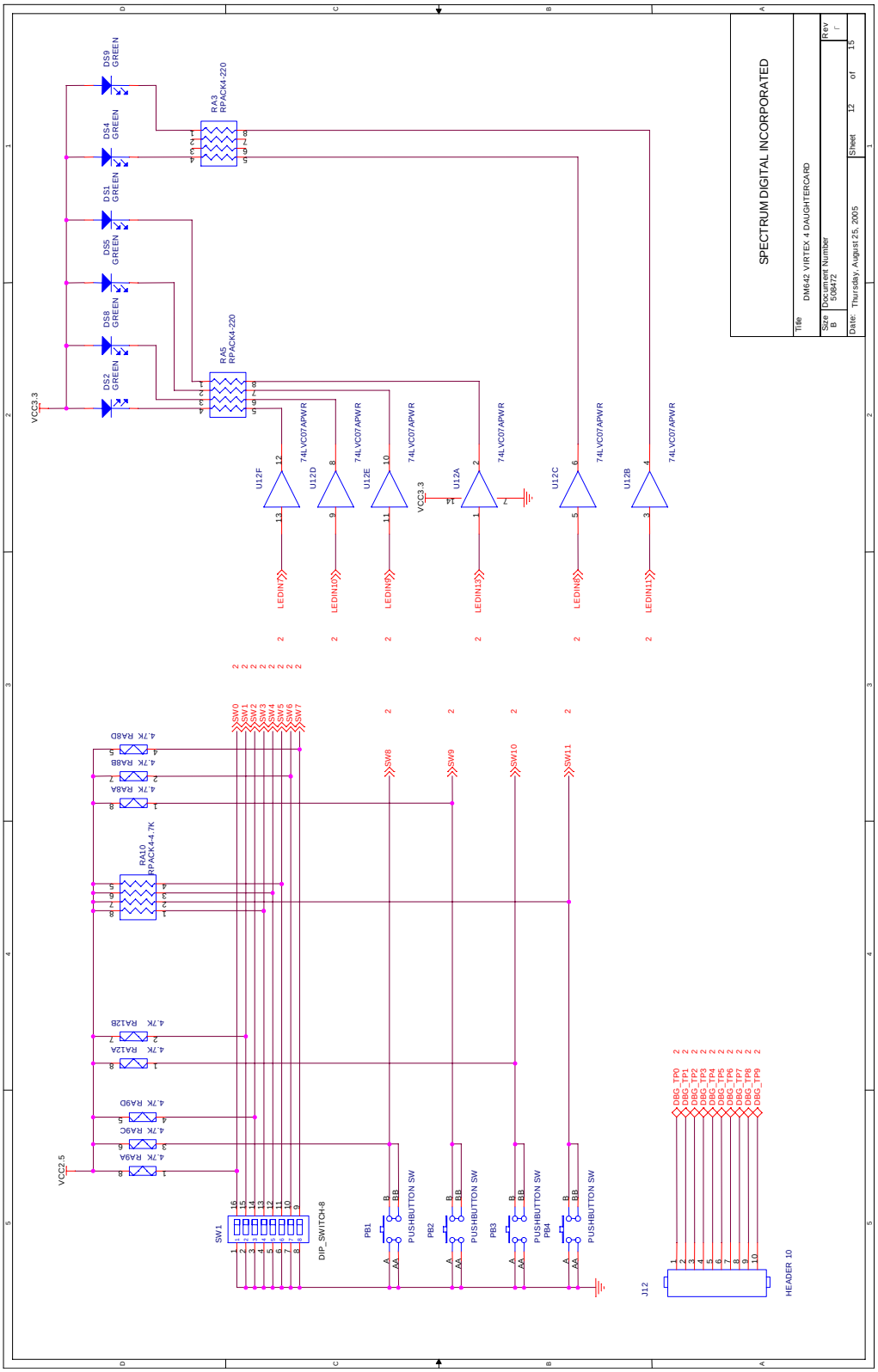

SPECTRUM DIGITAL INCORPORATED
Title
DM642 VIRTEX 4 DAUGHTERCARD
Size
B
Document Number
5084f72
Rev
F
Date: Thursday, August 25, 2005
Sheet
7
of
15
U10A
XC4VSX35-10FF668CES
U16B
XCCACE-TQ144I
VCC3.3
VCC2.5
VCC1.2

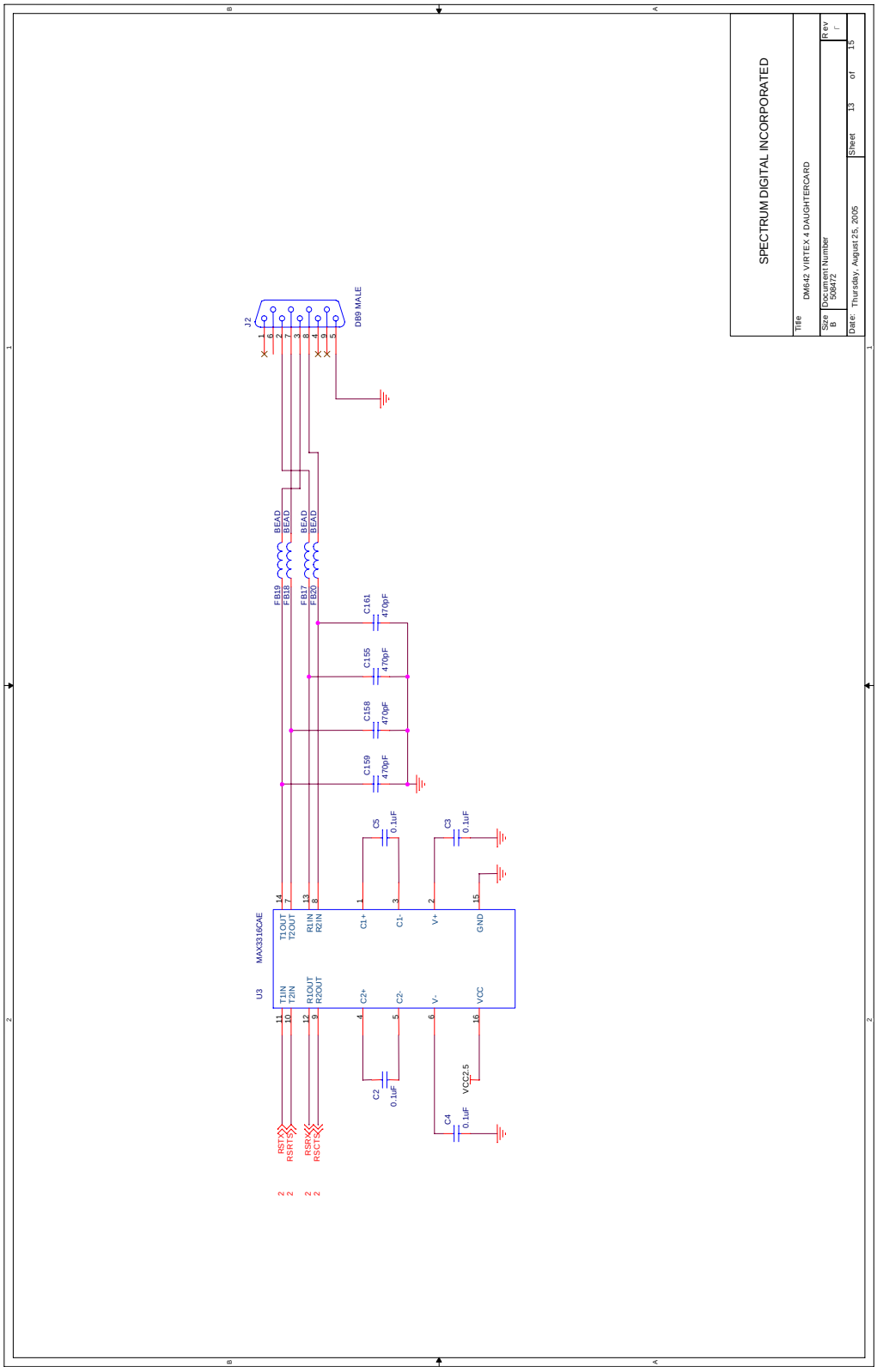

SPECTRUM DIGITAL INCORPORATED
Title
DM642 VIRTEX 4 DAUGHTERCARD
Size
B
Document Number
509472
Rev
F
Date:
Thursday, August 25, 2005
Sheet
8
of
15
SDD[0:63]
U1
U2
MT48LC8M32B2P-6
SDA[0:11]
SDBA[0:1]
SDD[0:63]
SDCLK
SDCKE
SDDQM0
SDDQM1
SDDQM2
SDDQM3
SDDQM4
SDDQM5
SDDQM6
SDDQM7
SDCS#
SDRAS#
SDCAS#
SDWE#

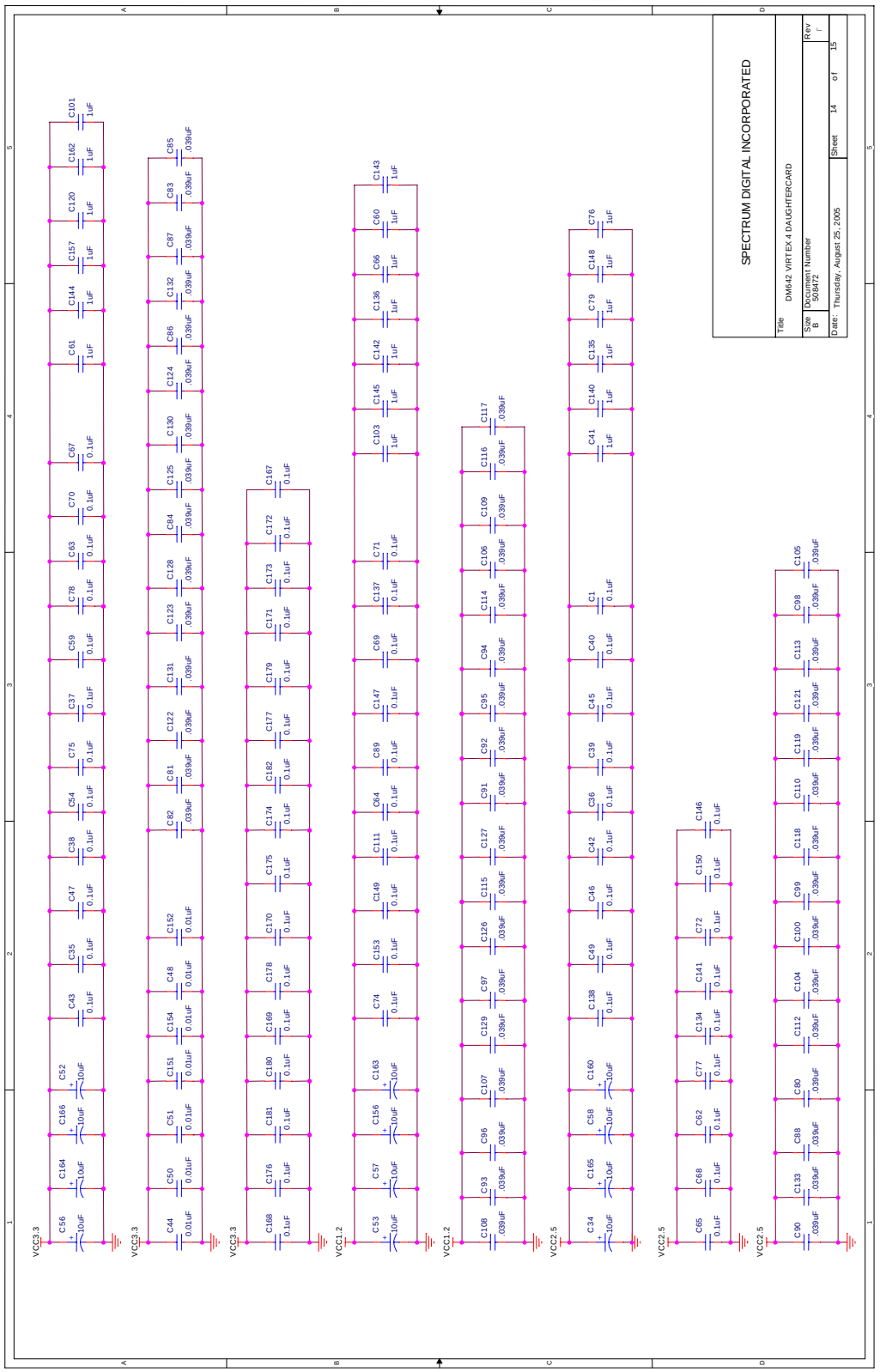

SPECTRUM DIGITAL INCORPORATED
Title
DM642 VIRTEX 4 DAUGHTERCARD
Size
B
Document Number
508472
Rev
F
Date:
Thursday, August 25, 2005
Sheet
9
of
15
CONNECTOR 45 X 2
CONNECTOR 45 X 2

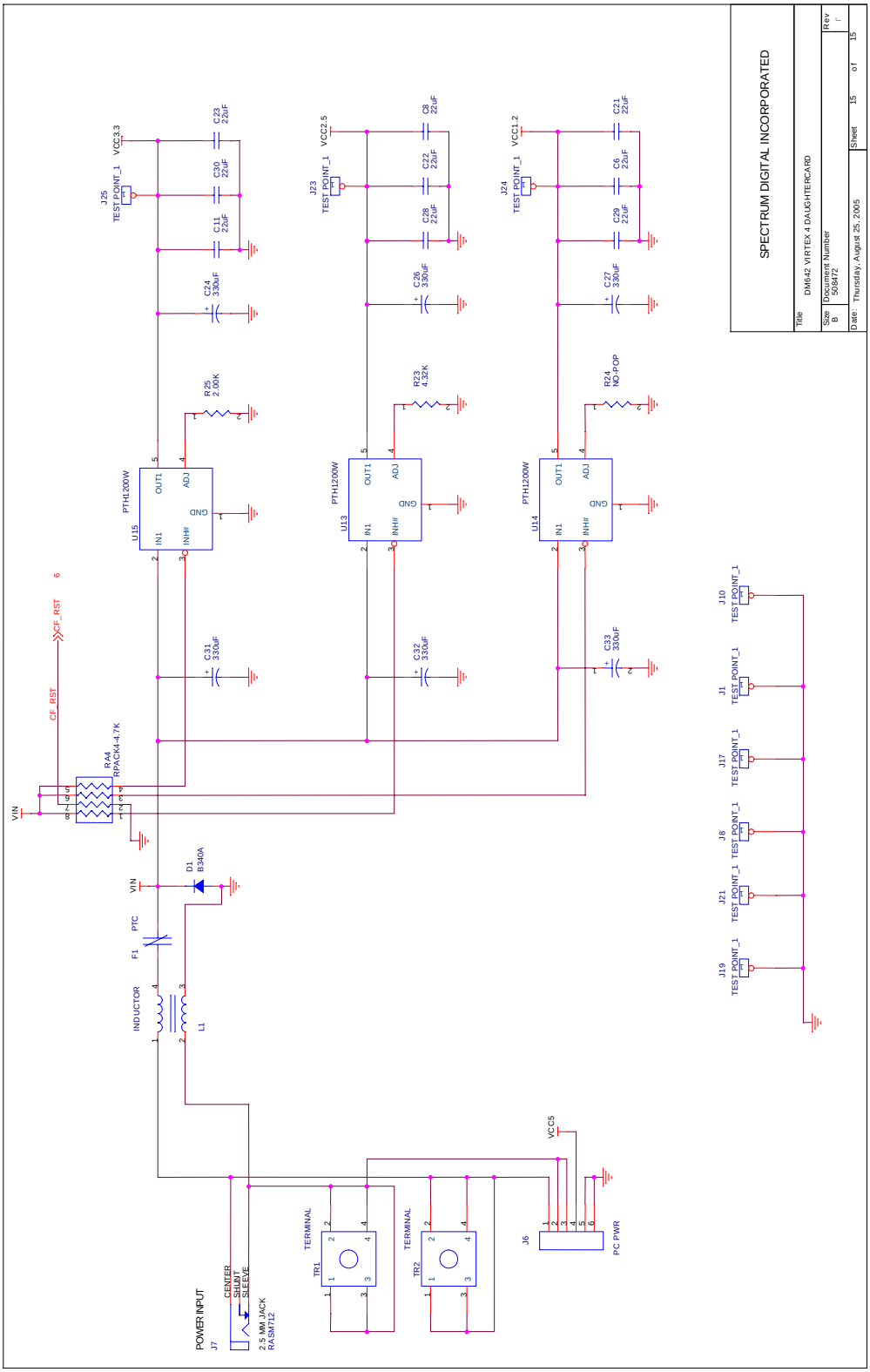

SPECTRUM DIGITAL INCORPORATED
Title
DM642 VIRTEX 4 DAUGHTERCARD
Size
B
Document Number
503472
Rev
F
Date: Thursday, August 25, 2005
Sheet
10
of
15
J27
CONNECTOR 45 X 2
ECLKOUT2
EBE2#
EBE0#
ECE2#
ERAS#
EARDY
EBE3#
EBE1#
ECE3#
ECAS#
EWE#
EAB:22
ED[0:31]


SPECTRUM DIGITAL INCORPORATED
Title
DM642 VIRTEX 4 DAUGHTERCARD
Size B
Document Number 508472
Rev F
Date: Thursday, August 25, 2005
Sheet 11 of 15
U8
VF261BL-54.0000MHz
U6
VF261BL-74.2500MHz
U4
VF261BL-74.1758MHz
OSC_54.00P
OSC_54.00N
OSC_74.25P
OSC_74.25N
OSC_74.1758P
OSC_74.1758N
OSC_OPEN_P1
OSC_OPEN_N1
ECLKOUT2_O
VP2CLK0
VP2CLK1
VP1CLK0
VP1CLK1
VP0CLK0
VP0CLK1
J3 TEST POINT
J4 TEST POINT
VCC3.3


SPECTRUM DIGITAL INCORPORATED
Title DM642 VIRTEX 4 DAUGHTERCARD
Size B
Document Number 508472
Rev F
Date: Thursday, August 25, 2005
Sheet 12 of 15
DS9 GREEN
DS4 GREEN
DS1 GREEN
DS5 GREEN
DS8 GREEN
DS2 GREEN
RA3 RPACK4-220
RA5 RPACK4-220
VCC3.3
74LVC07APWR
U12F
U12D
U12E
U12A
U12C
U12B
LEDIN7
LEDIN10
LEDIN9
LEDIN13
LEDIN8
LEDIN11
SW0
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
SW9
SW10
SW11
4.7K RA8D
4.7K RA8B
4.7K RA8A
RA10 RPACK4-4.7K
4.7K RA12B
4.7K RA12A
4.7K RA9D
4.7K RA9C
4.7K RA9A
VCC2.5
SW1
DIP_SWITCH-8
PB1
PB2
PB3
PB4
PUSHBUTTON SW
DBG_TP0
DBG_TP1
DBG_TP2
DBG_TP3
DBG_TP4
DBG_TP5
DBG_TP6
DBG_TP7
DBG_TP8
DBG_TP9
J12
HEADER 10


SPECTRUM DIGITAL INCORPORATED
Title DM642 VIRTEX 4 DAUGHTERCARD
Size B
Document Number 508472
Rev F
Date: Thursday, August 25, 2005
Sheet 13 of 15
J2
DB9 MALE
FB19
FB18
FB17
FB20
BEAD
C161 470pF
C155 470pF
C158 470pF
C159 470pF
C5 0.1uF
C3 0.1uF
U3
MAX3316CAE
T1IN
T2IN
R1OUT
R2OUT
T1OUT
T2OUT
R1IN
R2IN
C1+
C1-
V+
GND
C2+
C2-
V-
VCC
C2 0.1uF
C4 0.1uF
VCC2.5
RST
RSRTS
RSR
RSCTS

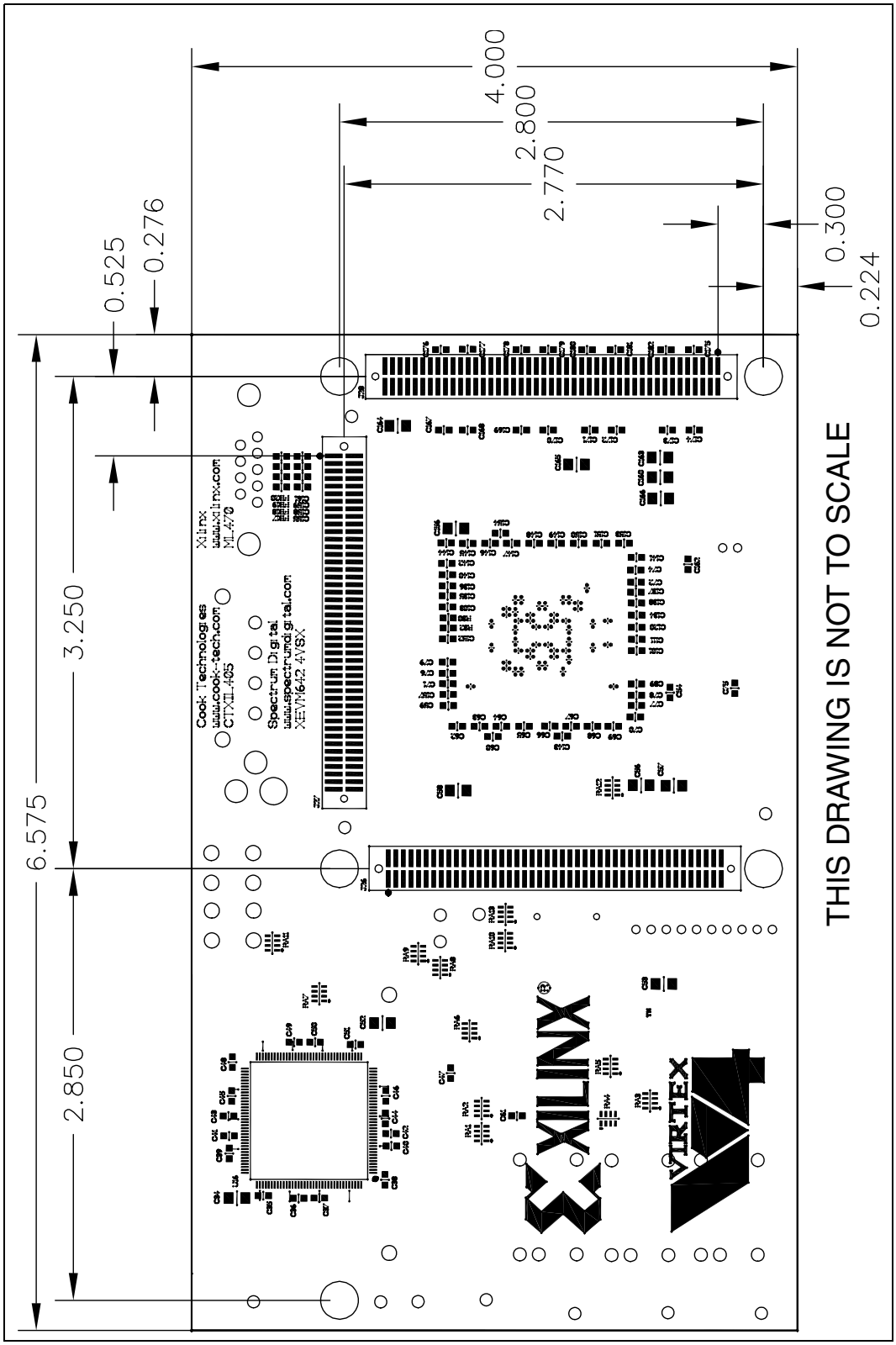

SPECTRUM DIGITAL INCORPORATED
Title
DM642 VIRTEX 4 DAUGHTERCARD
Size
B
Document Number
5/9/8472
Rev
Date: Thursday, August 25, 2005
Sheet 14 of 15
VCC3.3
VCC1.2
VCC2.5


SPECTRUM DIGITAL INCORPORATED
Title
DM642 VIRTEX 4 DAUGHTERCARD
Size B
Document Number
508472
Rev
Date: Thursday, August 25, 2005
Sheet 15 of 15
VCC3.3
VCC2.5
VCC1.2
VCC5
VIN
CF_RST
PTC
INDUCTOR
POWER INPUT
CENTER
SHUNT
SLEEVE
2.5 MM JACK
RASM712
TERMINAL
PC PWR
PTH1200W

Appendix B

Mechanical Information

This appendix contains the mechanical information about the XEVM642 4VSX35 Daughter Card.


4.000
2.800
2.770
0.300
0.224
0.525
0.276
3.250
6.575
2.850
THIS DRAWING IS NOT TO SCALE
Xilinx
www.xilinx.com
ML478
Cook Technologies
www.cook-tech.com
CTXXL405
Spectrum Digital
www.spectrumdigital.com
XEVM642 4VSX
XILINX
VIRTEX

[redacted]

SPECTRUM DIGITAL INCORPORATED

Printed in U.S.A., June 2006
508475-0001 Rev A