

# ***TMS320C6416 DSK***

*Technical  
Reference*

# TMS320C6416 DSK Technical Reference

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## About This Manual

This document describes the board level operations of the TMS320C6416 DSP Starter Kit (DSK) module. The DSK is based on the Texas Instruments TMS320C6416 Digital Signal Processor.

The TMS320C6416 DSK is a table top card to allow engineers and software developers to evaluate certain characteristics of the TMS320C6416 DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

## Notational Conventions

This document uses the following conventions.

The TMS320C6416 DSK will sometimes be referred to as the DSK.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

```
equations  
!rd = !strobe&rw;
```

## Information About Cautions

This book may contain cautions.

***This is an example of a caution statement.***

A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

## Related Documents

Texas Instruments TMS320C64xx DSP CPU Reference Guide  
Texas Instruments TMS320C64xx DSP Peripherals Reference Guide

**Table 1: Manual History**

Revision	History
A	Production Release
B	Updates for 720 Mhz. Support

# Chapter 1

## Introduction to the TMS320C6416 DSK

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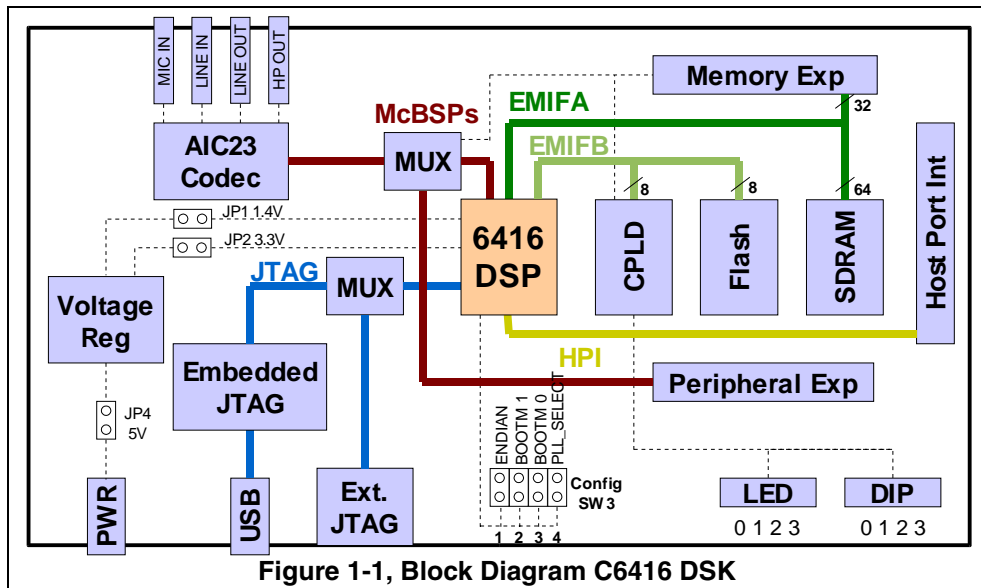
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Chapter One provides a description of the TMS320C6416 DSK along with the key features and a block diagram of the circuit board.

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### 1.1 Key Features

The C6416 DSK is a low-cost standalone development platform that enables users to evaluate and develop applications for the TI C64xx DSP family. The DSK also serves as a hardware reference design for the TMS320C6416 DSP. Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.



The DSK comes with a full compliment of on-board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments TMS320C6416 DSP operating at 600 or 720 MHz.
- An AIC23 stereo codec
- 16 Mbytes of synchronous DRAM
- 512 Kbytes of non-volatile Flash memory
- 4 user accessible LEDs and DIP switches
- Software board configuration through registers implemented in CPLD
- Configurable boot options and clock input selection
- Standard expansion connectors for daughter card use
- JTAG emulation through on-board JTAG emulator with USB host interface or external emulator
- Single voltage power supply (+5V)

## **1.2 Functional Overview of the TMS320C6416 DSK**

The DSP on the 6416 DSK interfaces to on-board peripherals through one of two busses, the 64-bit wide EMIFA and the 8-bit wide EMIFB. The SDRAM, Flash and CPLD are each connected to one of the busses. EMIFA is also connected to the daughtercard expansion connectors which is used for third party add-in boards.

An on-board AIC23 codec allows the DSP to transmit and receive analog signals. McBSP1 is used for the codec control interface and McBSP2 is used for data. Analog I/O is done through four 3.5mm audio jacks that correspond to microphone input, line input, line output and headphone output. The codec can select the microphone or the line input as the active input. The analog output is driven to both the line out (fixed gain) and headphone (adjustable gain) connectors. McBSP1 and McBSP2 can be re-routed to the expansion connectors in software.

A programmable logic device called a CPLD is used to implement glue logic that ties the board components together. The CPLD also has a register based user interface that lets the user configure the board by reading and writing to the CPLD registers.

The DSK includes 4 LEDs and 4 position DIP switch as a simple way to provide the user with interactive feedback. Both are accessed by reading and writing to the CPLD registers.

An included 5V external power supply is used to power the board. On-board switching voltage regulators provide the 1.4V DSP core voltage and 3.3V I/O supplies. The board is held in reset until these supplies are within operating specifications. A separate regulator powers the 3.3V lines on the expansion interface.

Code Composer communicates with the DSK through an embedded JTAG emulator with a USB host interface. The DSK can also be used with an external emulator through the external JTAG connector.

### **1.3 Basic Operation**

The DSK is designed to work with TI's Code Composer Studio development environment and ships with a version specifically tailored to work with the board. Code Composer communicates with the board through the on-board JTAG emulator. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

After the install is complete, follow these steps to run Code Composer. The DSK must be fully connected to launch the DSK version of Code Composer.

- 1) Connect the included power supply to the DSK.
- 2) Connect the DSK to your PC with a standard USB cable (also included).
- 3) Launch Code Composer from its icon on your desktop.

Detailed information about the DSK including a tutorial, examples and reference material is available in the DSK's help file. You can access the help file through Code Composer's help menu. It can also be launched directly by double-clicking on the file `c6416dsk.hlp` in Code Composer's `docs\hlp` subdirectory.

## 1.4 Memory Map

The C64xx family of DSPs has a large byte addressable address space. Program code and data can be placed anywhere in the unified address space. Addresses are always 32-bits wide.

The memory map shows the address space of a generic 6416 processor on the left with specific details of how each region is used on the right. By default, the internal memory sits at the beginning of the address space. Portions of memory can be remapped in software as L2 cache rather than fixed RAM.

Each EMIF (External Memory Interface) has 4 separate addressable regions called chip enable spaces (CE0-CE3). The SDRAM occupies CE0 of EMIFA while the CPLD and Flash are mapped to CE0 and CE1 of EMIFB respectively. Daughtercards use CE2 and CE3 of EMIFA.

Address	Generic 6416 Address Space	6416 DSK
0x00000000	Internal Memory	Internal Memory
0x00100000	Reserved Space or Peripheral Regs	Reserved or Peripheral
0x60000000	EMIFB CE0	CPLD
0x64000000	EMIFB CE1	Flash
0x68000000	EMIFB CE2	
0x6C000000	EMIFB CE3	
0x80000000	EMIFA CE0	SDRAM
0x90000000	EMIFA CE1	
0xA0000000	EMIFA CE2	
0xB0000000	EMIFA CE3	Daughter Card

**Figure 1-2, Memory Map, C6416 DSK**

### 1.5 Configuration Switch Settings

The DSK has 3 configuration switches that allows users to control the operational state of the DSP when it is released from reset. The configuration switch block is labeled SW3 on the DSK board, next to the reset switch.

Configuration switch 1 controls the endianness of the DSP while switches 2 and 3 configure the boot mode that will be used when the DSP starts executing. By default all switches are off which corresponds to EMIFB boot (out of 8-bit Flash) in little endian mode. The figure below shows these settings.

**Table 1: Configuration Switch Settings**

Switch 4	Switch 3	Switch 2	Switch 1	Configuration Description
Off				720 Mhz operation (60 Mhz input clock)
On				600 Mhz operation (50 Mhz input clock)
	Off	Off		EMIF boot from 8-bit Flash
	Off	On		No Boot
	On	Off		Reserved
	On	On		HPI boot
			Off	Little endian
			On	Big endian

### 1.6 Power Supply

The DSK operates from a single +5V external power supply connected to the main power input (J5). Internally, the +5V input is converted into +1.4V and +3.3V using a dual voltage regulator. The +1.4V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and all other chips on the board. The power connector is a 2.5mm barrel-type plug.

There are three power test points on the DSK at JP1, JP2 and JP4. All 6416 I/O current passes through JP2 while all core current passes through JP1. All system current passes through JP4. Normally these jumpers are closed. To measure the current passing through remove the jumpers and connect the pins with a current measuring device such as a multimeter or current probe.

The DSK provides +3.3V, up to 1A for the daughter card. The +3.3V supply is derived from the +5V power source via the main +3.3 volt regulator. It is also possible to provide the daughter card with +12V and -12V when the external power connector (J6) is used.

## Chapter 2

# Board Components

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This chapter describes the operation of the major board components on the TMS320C6416 DSK.

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## **2.1 CPLD (Programmable Logic)**

The C6416 DSK uses an Altera EPM3128TC100-10 Complex Programmable Logic Device (CPLD) device to implement:

- 4 Memory-mapped control/status registers that allow software control of various board features.
- Address decode and memory access logic.
- Control of the daughter card interface and signals.
- Assorted "glue" logic that ties the board components together.

### **2.1.1 CPLD Overview**

The CPLD logic is used to implement functionality specific to the DSK. Your own hardware designs will likely implement a completely different set of functions or take advantage of the DSPs high level of integration for system design and avoid the use of external logic completely.

The CPLD implements simple random logic functions that eliminate the need for additional discrete devices. In particular, the CPLD aggregates the various reset signals coming from the reset button and power supervisors and generates a global reset.

The EPM3128TC100-10 is a 3.3V (5V tolerant), 100-pin QFP device that provides 128 macrocells, 80 I/O pins, and a 10 ns pin-to-pin delay. The device is EEPROM-based and is in-system programmable via a dedicated JTAG interface (a 10-pin header on the DSK). The CPLD source files are written in the industry standard VHDL (Hardware Design Language) and included with the DSK.

## 2.1.2 CPLD Registers

The 4 CPLD memory-mapped registers allows users to control CPLD functions in software. On the 6416 DSK the registers are primarily used to access the LEDs and DIP switches and control the daughter card interface. The registers are mapped into EMIFB data space at address 0x60000000. They appear as 8-bit registers with a simple asynchronous memory interface. The following table gives a high level overview of the CPLD registers and their bit fields:

The table below shows the bit definitions for the 4 registers in CPLD.

**Table 1: CPLD Register Definitions**

Offset	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	USER_REG	USR_SW3 R	USR_SW2 R	USR_SW1 R	USR_SW0 R	USR_LED3 R/W 0(Off)	USR_LED2 R/W 0(Off)	USR_LED1 R/W 0(Off)	USR_LED0 R/W 0(Off)
1	DC_REG	DC_DET R	0	DC_STAT1 R	DC_STAT0 R	DC_RST R 0(No reset)	0	DC_CNTL1 R/W 0(low)	DC_CNTL0 R/W 0(low)
4	VERSION	CPLD_VER[3:0] R				0	BOARD_VERSION[2:0] R		
6	MISC	McBSP2_EN R (MCBSP2 enabled)	SCR_4 R/W 0	SCR_3 R/W 0	DSPPLL_ SELECT R 1	DSPPLL_ ENABLE R 1	FLASH_PAGE R/W 0 (A19=0)	McBSP2 ON/OFF Board R/W 0 (Onboard)	McBSP1 ON/OFF Board R/W 0 (Onboard)

## 2.1.3 USER\_REG Register

USER\_REG is used to read the state of the 4 DIP switches and turn the 4 LEDs on or off to allow the user to interact with the DSK. The DIP switches are read by reading the top 4 bits of the register and the LEDs are set by writing to the low 4 bits.

**Table 2: CPLD USER\_REG Register**

Bit	Name	R/W	Description
7	USER_SW3	R	User DIP Switch 3(1 = Off, 0 = On)
6	USER_SW2	R	User DIP Switch 2(1 = Off, 0 = On)
5	USER_SW1	R	User DIP Switch 1(1 = Off, 0 = On)
4	USER_SW0	R	User DIP Switch 0(1 = Off, 0 = On)
3	USER_LED3	R/W	User-defined LED 3 Control (0 = Off, 1 = On)
2	USER_LED2	R/W	User-defined LED 2 Control (0 = Off, 1 = On)
1	USER_LED1	R/W	User-defined LED 1 Control (0 = Off, 1 = On)
0	USER_LED0	R/W	User-defined LED 0 Control (0 = Off, 1 = On)

### 2.1.4 DC\_REG Register

DC\_REG is used to monitor and control the daughter card interface. DC\_DET detects the presence of a daughter card. DC\_STAT and DC\_CNTL provide simple communications with the daughter card through readable status lines and writable control lines.

The daughter card is released from reset when the DSP is released from reset. DC\_RST can be used to put the card back in reset.

**Table 3: DC\_REG Register**

Bit	Name	R/W	Description
7	DC_DET	R	Daughter Card Detect (1= Board detected)
6	0	R	Always 0
5	DC_STAT1	R	Daughter Card Status 1 (0=Low, 1 = High)
4	DC_STAT0	R	Daughter Card Status 0 (0=Low, 1 = High)
3	DC_RST	R/W	Daughter Card Reset (0=No Reset, 1 = Reset)
2	0	R	Always zero
1	DC_CNTL1	R/W	Daughter Card Control 1(0 = Low, 1 = High)
0	DC_CNTL0	R/W	Daughter Card Control 0(0 = Low, 1 = High)

### 2.1.5 VERSION Register

The VERSION register contains two read only fields that indicate the BOARD and CPLD versions. This register will allow your software to differentiate between production releases of the DSK and account for any variances. This register is not expected to change often, if at all.

**Table 4: Version Register Bit Definitions**

Bit #	Name	R/W	Description
7	CPLD_VER3	R	Most Significant CPLD Version Bit
6	CPLD_VER2	R	CPLD Version Bit
5	CPLD_VER1	R	CPLD Version Bit
4	CPLD_VER0	R	Least Significant CPLD Version Bit
3	0	R	Always 0
2	DSK_VER2	R	Most Significant DSK Board Version Bit
1	DSK_VER1	R	DSK Board Version Bit
0	DSK_VER0	R	Least Significant DSK Board Version Bit

### 2.1.6 MISC Register

The MISC register is used to provide software control for miscellaneous board functions. On the 6416 DSK, the MISC register controls how auxiliary signals are brought out to the daughter-card connectors.

McBSP1 and McBSP2 are usually used as the control and data ports of the on-board AIC23 codec. The power-on state of these bits (both 0s) represents that configuration. Set MCBSP1SEL or MCBSP2SEL to route the McBSPs to the daughtercard connectors rather than the codec.

The Flash and CPLD share CE1 which means that the highest address bit (A21) is used to differentiate between the two. In this configuration 512Kbytes of 8-bit Flash are visible at the beginning of CE1 which matches the chip on the production board. If the Flash is replaced with a 1Mbyte chip, only 512Kbytes of Flash will still be visible but FLASH\_PAGE can be used to select between the top and bottom halves. FLASH\_PAGE replaces the address bit (A21) that is lost sharing CE1 with the CPLD.

An on-board PLL is used to generate the DSP's input clock frequency. The DSPPLL\_SELECT and DSPPLL\_ENABLE bits are read-only versions of the PLL configuration signals. DSPPLL\_ENABLE will read 1 if the PLL is enabled. DSPPLL\_SELECT (set by configuration switch #4) switches between a 50 Mhz and 60 Mhz input clock.

The 6416's PCI interface and McBSP2 share some pins. The McBSP2\_EN signal is used to disable McBSP2 when the PCI interface is active. McBSP2\_EN is generated on the board when an appropriate daughtercard that uses PCI is plugged in, it can be read through this CPLD bit.

The scratch bits are unused. They can be set to any value.

**Table 5: MISC Register**

Bit	Name	R/W	Description
7	McBSP2_EN	R	Value of McBSP2_EN from PCI header
6	SCRATCH_4	R/W	Scratch bit 4
5	SCRATCH_3	R/W	Scratch bit 3
4	DSPPLL_SELECT	R	PLL select (0 = 50/600 Mhz, 1 = 60/720 Mhz)
3	DSPPLL_ENABLE	R	PLL enable (0 = off, 1 = on)
2	FLASH_PAGE	R/W	Flash address bit 19
1	MCBSP2SEL	R/W	McBSP2 on/off board (0 = on-board, 1 = off-board)
0	MCBSP1SEL	R/W	McBSP1 on/off board (0 = on-board, 1 = off-board)

2.2 AIC23 Codec

The DSK uses a Texas Instruments AIC23 (part #TLV320AIC23) stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line and headphone outputs so the user can hear the output.

The codec communicates using two serial channels, one to control the codec’s internal configuration registers and one to send and receive digital audio samples. McBSP1 is used as the unidirectional control channel. It should be programmed to send a 16-bit control word to the AIC23 in SPI format. The top 7 bits of the control word should specify the register to be modified and the lower 9 should contain the register value. The control channel is only used when configuring the codec, it is generally idle when audio data is being transmitted,

McBSP2 is used as the bi-directional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The DSK examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the DSP side. The preferred serial format is DSP mode which is designed specifically to operate with the McBSP ports on TI DSPs.

The codec has a 12MHz system clock. The 12MHz system clock corresponds to USB sample rate mode, named because many USB systems use a 12MHz clock and can use the same clock for both the codec and USB controller. The internal sample rate generate subdivides the 12MHz clock to generate common frequencies such as 48KHz, 44.1KHz and 8KHz. The sample rate is set by the codec’s SAMPLERATE register. The figure below shows the codec interface on the C6416 DSK.

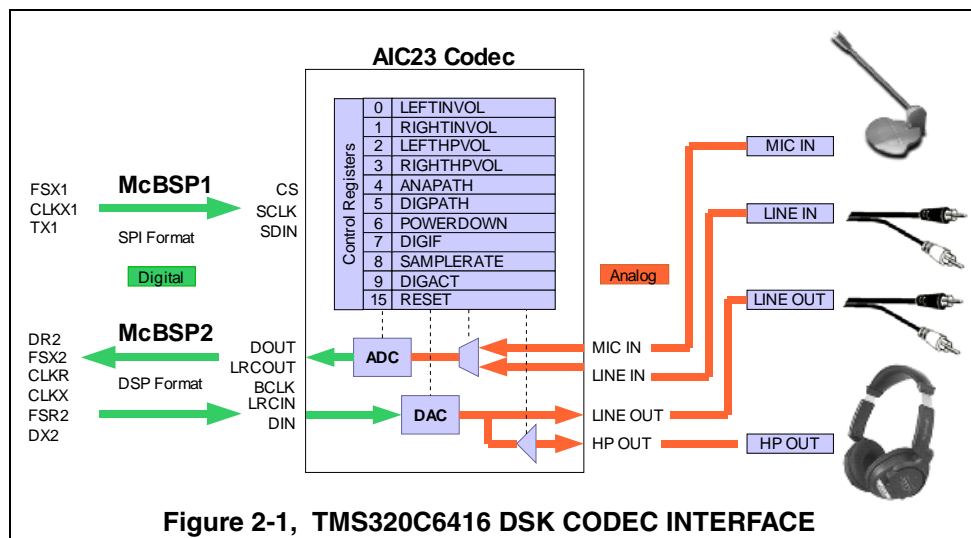


Figure 2-1, TMS320C6416 DSK CODEC INTERFACE

### **2.3 Synchronous DRAM**

The DSK uses a pair of industry standard 64 megabit SDRAMs in CE0 of EMIFA. The two devices are used in parallel to create a 64-bit wide interface. Total available memory is 16 megabytes.

The DSK uses an EMIFA clock of 120 MHz. The integrated SDRAM controller is started by configuring the EMIF in software. Timings can be found in the SDRAM datasheet and the DSK help file. When using the SDRAM, note that one row of the memory array must be refreshed at least every 15.6 microseconds to maintain the integrity of its contents.

### **2.4 Flash Memory**

The DSK uses a 512Kbyte external Flash as a boot option. It is connected to CE1 of EMIFB with an 8-bit interface. Flash is a type of memory which does not lose its contents when the power is turned off. When read it looks like a simple asynchronous read-only memory (ROM). Flash can be erased in large blocks commonly referred to as sectors or pages. Once a block has been erased each word can be programmed once through a special command sequence. After that the entire block must be erased again to change the contents.

The Flash requires 70ns for both reads and writes. The general settings used with the DSK use 8 cycles for both read and write strobes (80ns) to leave a little extra margin.

### **2.5 LEDs and DIP Switches**

The DSK includes 4 software accessible LEDs (D7-D10) and DIP switches (SW1) that provide the user a simple form of input/output. Both are accessed through the CPLD USER\_REG register.

## **2.6 Daughter Card Interface**

The DSK provides three expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their DSK platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are for memory, peripherals, and the Host Port Interface (HPI)

The memory connector provides access to the DSP's asynchronous EMIF signals to interface with memories and memory mapped devices. It supports byte addressing on 32 bit boundaries. The peripheral connector brings out the DSP's peripheral signals like McBSPs, timers, and clocks. Both connectors provide power and ground to the daughter card

The HPI is a high speed interface that can be used to allow multiple DSPs to communicate and cooperate on a given task. The HPI connector brings out the HPI specific control signals as well as McBSP2.

Most of the expansion connector signals are buffered so that the daughter card cannot directly influence the operation of the DSK board. The use of TI low voltage, 5V tolerant buffers, and CBT interface devices allows the use of either +5V or +3.3V devices to be used on the daughter card.

Other than the buffering, most daughter card signals are not modified on the board. However, a few daughter card specific control signals like DC\_RESET and DC\_DET exist and are accessible through the CPLD DC\_REG register. The DSK also multiplexes the McBSP1 and McBSP2 of on-board or external use. This function is controlled through the CPLD MISC register.

# Chapter 3

## Physical Description

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This chapter describes the physical layout of the TMS320C6416 DSK and its connectors.

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### 3.1 Board Layout

The C6416 DSK is a 8.75 x 4.5 inch (210 x 115 mm.) multi-layer board which is powered by an external +5 volt only power supply. Figure 3-1 shows the layout of the C6416 DSK.

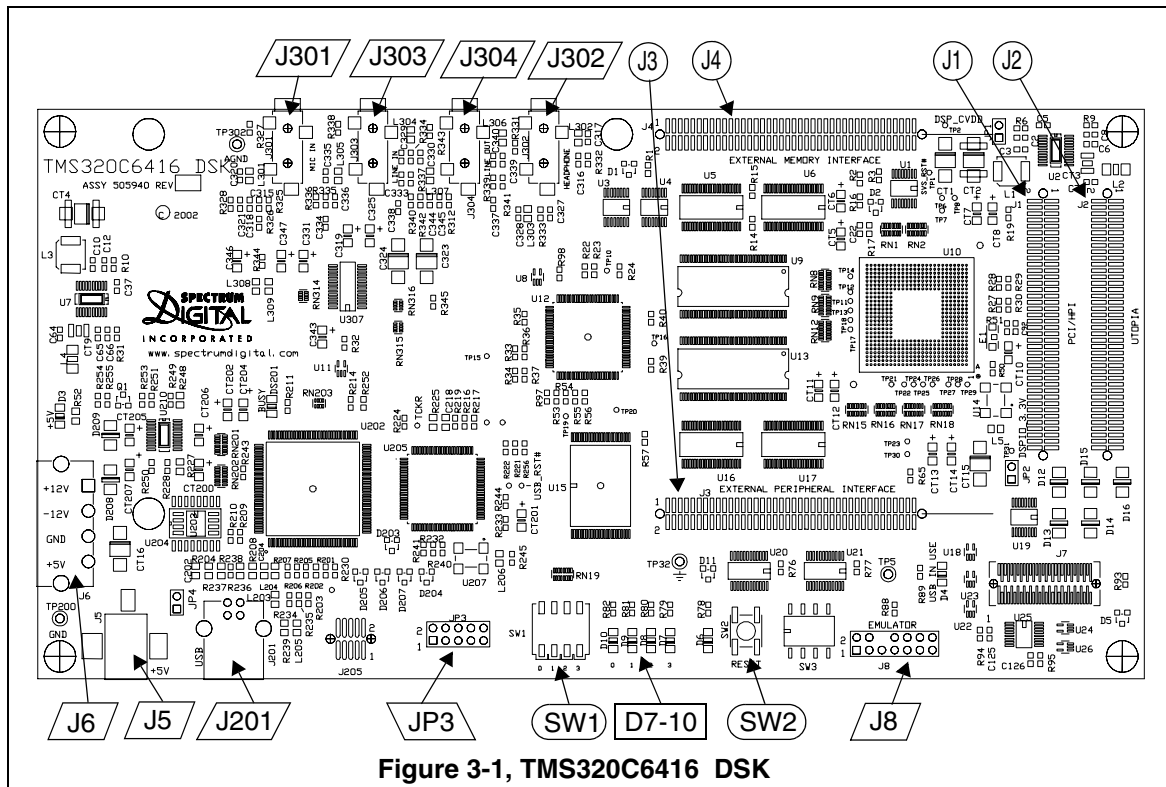


Figure 3-1, TMS320C6416 DSK

### 3.2 Connector Index

The TMS320C6416 DSK has many connectors which provide the user access to the various signals on the DSK.

**Table 1: TMS320C6416 DSK Connectors**

Connector	# Pins	Function
J4	80	Memory
J3	80	Peripheral
J1	80	HPI
J301	3	Microphone
J303	3	Line In
J304	3	Line Out
J303	3	Headphone
J5	2	+5 Volt
J6 *	4	Optional Power Connector
J8	14	External JTAG
J201	5	USB Port
JP3	10	CPLD Programming
SW3	8	DSP Configuration Jumper

**Note:** "\*" Not populated

### 3.3 Expansion Connectors

The TMS320C6416 DSK supports three expansion connectors that follow the Texas Instruments interconnection guidelines. The expansion connector pinouts are described in the following three sections.

The three expansion connectors are all 80 pin 0.050 x 0.050 inches low profile connectors from Samtec or AMP. The Samtec SFM Series (surface mount) connectors are designed for high speed interconnections because they have low propagation delay, capacitance, and cross talk. The connectors present a small foot print on the DSK. Each connector includes multiple ground, +5V, and +3.3V power signals so that the daughter card can obtain power directly from the DSK. The peripheral expansion connector additionally provides both +12V and -12V to the daughter card. The recommended mating connector, whose part number is TFM-140-32-S-D-LC, is a surface mount connector that provides a 0.465" mated height.

**Note:** I is on an Input pin  
 O is on an Output pin  
 Z is on a High Impedance pin

## 3.3.1 J4, Memory Expansion Connector

Table 2: J4, Memory Expansion Connector

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	5V	Vcc	5V voltage supply pin	2	5V	Vcc	5V voltage supply pin
3	AEA21	O	EMIF address pin 21	4	AEA20	O	EMIF address pin 20
5	AEA19	O	EMIF address pin 19	6	AEA18	O	EMIF address pin 18
7	AEA17	O	EMIF address pin 17	8	AEA16	O	EMIF address pin 16
9	AEA15	O	EMIF address pin 15	10	AEA14	O	EMIF address pin 14
11	GND	Vss	System ground	12	GND	Vss	System ground
13	AEA13	O	EMIF address pin 13	14	AEA12	O	EMIF address pin 12
15	AEA11	O	EMIF address pin 11	16	AEA10	O	EMIF address pin 10
17	AEA9	O	EMIF address pin 9	18	AEA8	O	EMIF address pin 8
19	AEA7	O	EMIF address pin 7	20	AEA6	O	EMIF address pin 6
21	5V	Vcc	5V voltage supply pin	22	5V	Vcc	5V voltage supply pin
23	AEA5	O	EMIF address pin 5	24	AEA4	O	EMIF address pin 4
25	AEA3	O	EMIF address pin 3	26	AEA2	O	EMIF address pin 2
27	ABE3#	O	EMIF byte enable 3	28	ABE2#	O	EMIF byte enable 2
29	ABE1#	O	EMIF byte enable 1	30	ABE0#	O	EMIF byte enable 0
31	GND	Vss	System ground	32	GND	Vss	System ground
33	AED31	I/O	EMIF data pin 31	34	AED30	I/O	EMIF data pin 30
35	AED29	I/O	EMIF data pin 29	36	AED28	I/O	EMIF data pin 28
37	AED27	I/O	EMIF data pin 27	38	AED26	I/O	EMIF data pin 26
39	AED25	I/O	EMIF data pin 25	40	AED24	I/O	EMIF data pin 24
41	3.3V	Vcc	3.3V voltage supply pin	42	3.3V	Vcc	3.3V voltage supply pin
43	AED23	I/O	EMIF data pin 23	44	AED22	I/O	EMIF data pin 22
45	AED21	I/O	EMIF data pin 21	46	AED20	I/O	EMIF data pin 20
47	AED19	I/O	EMIF data pin 19	48	AED18	I/O	EMIF data pin 18
49	AED17	I/O	EMIF data pin 17	50	AED16	I/O	EMIF data pin 16
51	GND	Vss	System ground	52	GND	Vss	System ground
53	AED15	I/O	EMIF data pin 15	54	AED14	I/O	EMIF data pin 14
55	AED13	I/O	EMIF data pin 13	56	AED12	I/O	EMIF data pin 12
57	AED11	I/O	EMIF data pin 11	58	AED10	I/O	EMIF data pin 10
59	AED9	I/O	EMIF data pin 9	60	AED8	I/O	EMIF data pin 8
61	GND	Vss	System ground	62	GND	Vss	System ground
63	AED7	I/O	EMIF data pin 7	64	AED6	I/O	EMIF data pin 6
65	AED5	I/O	EMIF data pin 5	66	AED4	I/O	EMIF data pin 4
67	AED3	I/O	EMIF data pin 3	68	AED2	I/O	EMIF data pin 2
69	AED1	I/O	EMIF data pin 1	70	AED0	I/O	EMIF data pin 0
71	GND	Vss	System ground	72	GND	Vss	System ground
73	AARE#	O	EMIF async read enable	74	AWE#	O	EMIF async write enable
75	AAOE#	O	EMIF async output enable	76	AARDY	I	EMIF asynchronous ready
77	ACE3#	O	Chip enable 3	78	ACE2#	O	Chip enable 2
79	GND	Vss	System ground	80	GND	Vss	System ground

## 3.3.2 J3, Peripheral Expansion Connector

Table 3: J3, Peripheral Expansion Connector

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	12V	Vcc	12V voltage supply pin	2	-12V	Vcc	-12V voltage supply pin
3	GND	Vss	System ground	4	GND	Vss	System ground
5	5V	Vcc	5V voltage supply pin	6	5V	Vcc	5V voltage supply pin
7	GND	Vss	System ground	8	GND	Vss	System ground
9	5V	Vcc	5V voltage supply pin	10	5V	Vcc	5V voltage supply pin
11	N/C	-	No connect	12	N/C	-	No connect
13	N/C	-	No connect	14	N/C	-	No connect
15	N/C	-	No connect	16	N/C	-	No connect
17	N/C	-	No connect	18	N/C	-	No connect
19	3.3V	Vcc	3.3V voltage supply pin	20	3.3V	Vcc	3.3V voltage supply pin
21	CLKX0	I/O	McBSP0 transmit clock	22	CLKS0	I	McBSP0 clock source
23	FSX0	I/O	McBSP0 transmit frame sync	24	DX0	O	McBSP0 transmit data
25	GND	Vss	System ground	26	GND	Vss	System ground
27	CLKR0	I/O	McBSP0 receive clock	28	N/C	-	No connect
29	FSR0	I/O	McBSP0 receive frame sync	30	DR0	I	McBSP0 receive data
31	GND	Vss	System ground	32	GND	Vss	System ground
33	CLKX2	I/O	McBSP2 transmit clock	34	CLKS2	I	McBSP2 clock source
35	FSX2	I/O	McBSP2 transmit frame sync	36	DX2	O	McBSP2 transmit data
37	GND	Vss	System ground	38	GND	Vss	System ground
39	CLKR2	I/O	McBSP2 receive clock	40	N/C	-	No connect
41	FSR2	I/O	McBSP2 receive frame sync	42	DR2	I	McBSP2 receive data
43	GND	Vss	System ground	44	GND	Vss	System ground
45	TOUT0	O	Timer 0 output	46	TINP0	I	Timer 0 input
47	N/C	-	No connect	48	EXT_INT5	I	External interrupt 5
49	TOUT1	O	Timer 1 output	50	TINP1	I	Timer 1 input
51	GND	Vss	System ground	52	GND	Vss	System ground
53	EXT_INT4	I	External interrupt 4	54	N/C	-	No connect
55	N/C	-	No connect	56	N/C	-	No connect
57	N/C	-	No connect	58	N/C	-	No connect
59	RESET	O	System reset	60	N/C	-	No connect
61	GND	Vss	System ground	62	GND	Vss	System ground
63	CNTL1	O	Daughtercard control 1	64	CNTL0	O	Daughtercard control
65	STAT1	I	Daughtercard status 1	66	STAT0	I	Daughtercard status
67	EXT_INT6	I	External interrupt 6	68	EXT_INT7	I	External interrupt 7
69	ACE3#	O	Chip enable 3	70	N/C	-	No connect
71	N/C	-	No connect	72	N/C	-	No connect
73	N/C	-	No connect	74	N/C	-	No connect
75	DC_DET#	Vss	System ground	76	GND	Vss	System ground
77	GND	Vss	System ground	78	ECL KOUT	O	EMIF Clock
79	GND	Vss	System ground	80	GND	Vss	System ground

## 3.3.3 J1, HPI Expansion Connector

Table 4: J1, HPI Expansion Connector

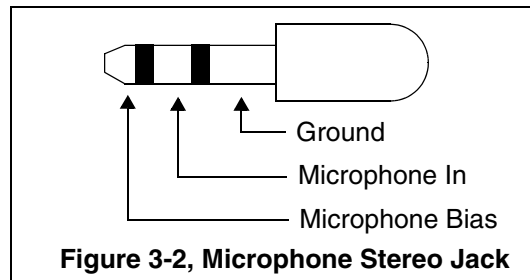
Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	PCI_EN	I	PCI enable	2	BSP2_EN	I	MCBSP2_EN
3	GND	Vss	System ground	4	HPI_RS#	I	HPI reset
5	XSP_CS	O	PCI serial	6	BEA13	I	PCI EEPROM auto-init
7	GND	Vss	System ground	8	GND	Vss	System ground
9	AD1	I/O	PCI address/data 1	10	PCBE0#	I/O	PCI command/byte ena 0
11	AD3	I/O	PCI address/data 3	12	AD0	I/O	PCI address/data 0
13	AD5	I/O	PCI address/data 5	14	AD2	I/O	PCI address/data 2
15	AD7	I/O	PCI address/data 7	16	AD4	I/O	PCI address/data 4
17	GND		System ground	18	AD6	I/O	PCI address/data 6
19	AD8	I/O	PCI address/data 8	20	GND	Vss	System ground
21	AD10	I/O	PCI address/data 10	22	AD9	I/O	PCI address/data 9
23	AD12	I/O	PCI address/data 12	24	AD11	I/O	PCI address/data 11
25	AD14	I/O	PCI address/data 14	26	AD13	I/O	PCI address/data 13
27	GND	Vss	System ground	28	AD15	I/O	PCI address/data 15
29	PCBE1#	I/O	PCI command/byte ena 1	30	GND	Vss	System ground
31	GND	Vss	System ground	32	PPAR	I/O	PCI parity
33	PSERR#	I/O	PCI system error	34	GND	Vss	System ground
35	GND	Vss	System ground	36	PSTOP#	I/O	PCI stop
37	PPERR#	I/O	PCI parity error	38	GND	Vss	System ground
39	GND	Vss	System ground	40	PTRDY#	I/O	PCI target ready
41	PDEVSEL#	I/O	PCI device select	42	GND	Vss	System ground
43	GND	Vss	System ground	44	PFRAME#	I/O	PCI Frame
45	PIRDY#	I/O	PCI initiator ready	46	GND	Vss	System ground
47	GND	Vss	System ground	48	AD16	I/O	PCI address/data 16
49	PCBE2#	I/O	PCI command/byte ena 2	50	AD18	I/O	PCI address/data 18
51	AD17	I/O	PCI address/data 17	52	AD20	I/O	PCI address/data 20
53	AD19	I/O	PCI address/data 19	54	AD22	I/O	PCI address/data 22
55	AD21	I/O	PCI address/data 21	56	GND	Vss	System ground
57	AD23	I/O	PCI address/data 23	58	PIDSEL	I	PCI init device select
59	PCBE3#	I/O	PCI command/byte ena 3	60	AD24	I/O	PCI address/data 24
61	GND	Vss	System ground	62	AD26	I/O	PCI address/data 26
63	AD25	I/O	PCI address/data 25	64	AD28	I/O	PCI address/data 28
65	AD27	I/O	PCI address/data 27	66	AD30	I/O	PCI address/data 30
67	AD29	I/O	PCI address/data 29	68	PGNT#	I	PCI bus grant
69	AD31	I/O	PCI address/data 31	70	GND	Vss	System ground
71	GND	Vss	System ground	72	PRST#	I	PCI reset
73	PREQ#	O	PCI bus request	74	GND	Vss	System ground
75	GND	Vss	System ground	76	PINTA#	O	PCI interrupt A
77	PCLK	I	PCI Clock	78	GND	Vss	System ground
79	GND	Vss	System ground	80	N/C	-	No connect

### 3.4 Audio Connectors

The C6416 DSK has 4 audio connectors. They are described in the following sections.

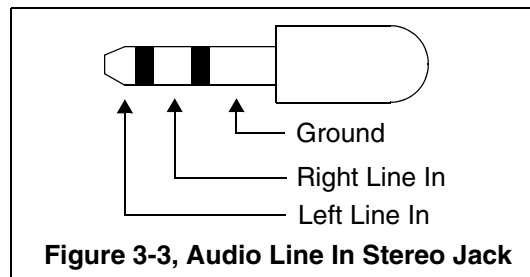
#### 3.4.1 J301, Microphone Connector

The input is a 3.5 mm. stereo jack. Both inputs are connected to the microphone so it is monaural. The signals on the plug are shown in the figure below.



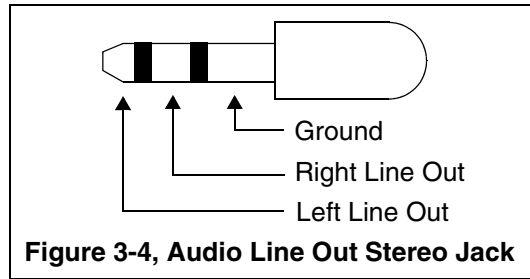
#### 3.4.2 J303, Audio Line In Connector

The audio line in is a stereo input. The input connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.



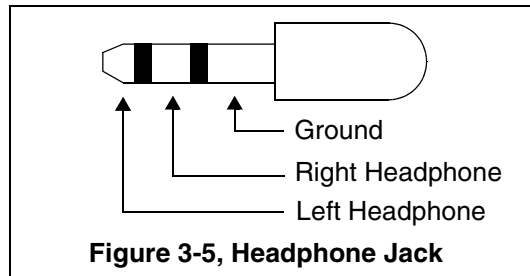
### 3.4.3 J304, Audio Line Out Connector

The audio line out is a stereo output. The output connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.



### 3.4.4 J303, Headphone Connector

Connector J4 is a headphone/speaker jack. It can drive standard headphones or a high impedance speaker directly. The standard 3.5 mm jack is shown in the figure below

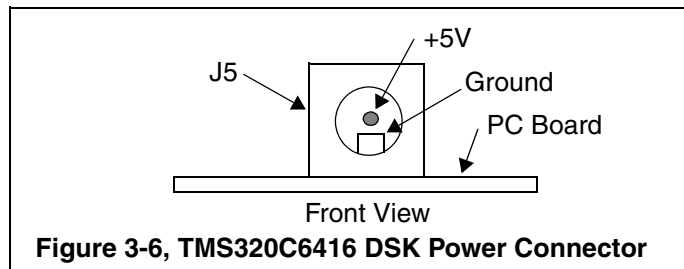


### 3.5 Power Connectors

The C6416 DSK has 2 power connectors. They are described in the following sections.

#### 3.5.1 J5, +5 Volt Connector

Power (+5 volts) is brought onto the TMS320C6416 DSK via connector J5. The connector has an outside diameter of 5.5 mm. and an inside diameter of 2.5 mm. The A diagram of J5 is shown below.



#### 3.5.2 J6, Optional Power Connector

Connector J6 is an optional power connector. It will operate with the standard personal computer power supply. To populate this connector use a Molex #15-24-4041. The table below shows the voltages on the respective pins.

**Table 5: J6, Optional Power Connector**

Pin #	Voltage Level
1	+12 Volts
2	-12 Volts
3	Ground
4	+5 Volts

**WARNING !**

Do not plug into J5 and J6 at the same time.

### 3.6 Miscellaneous Connectors

The C6416 DSK has 3 additional connectors to aid the user in developing with this product. They are described in the following sections.

#### 3.6.1 J201, USB Connector

Connector J201 provides a Universal Serial Bus (USB) Interface to the embedded JTAG emulation logic on the DSK. This allows for code development and debug without the use of an external emulator. The signals on this connector are shown in the below.

**Table 6: J201, USB Connector**

Pin #	USB Signal Name
1	USBVdd
2	D+
3	D-
4	USB Vss
5	Shield
6	Shield

#### 3.6.2 J8, External JTAG Connector

The TMS320C6416 DSK is supplied with a 14 pin header interface, J8. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown figure 3-6 below.

TMS	1	2	TRST-	Header Dimensions Pin-to-Pin spacing, 0.100 in. (X,Y) Pin width, 0.025-in. square post Pin length, 0.235-in. nominal
TDI	3	4	GND	
PD (+3.3V)	5	6	<b>no pin (key)</b>	
TDO	7	8	GND	
TCK-RET	9	10	GND	
TCK	11	12	GND	
EMU0	13	14	EMU1	

**Figure 3-7, JTAG INTERFACE**

The signal names for each pin are shown in the table below.

**Table 7: J8, JTAG Interface**

Pin #	Signal Name
1	TMS
2	TRST-
3	TDI
4	GND
5	PD
6	no pin
7	TDO
8	GND
9	TCK-RET
10	GND
11	TCK
12	GND
13	EMU0
14	EMU1

### 3.6.3 JP3, PLD Programming Connector

This connector interfaces to the Altera CPLD, U12. It is used in the in the factory for the programming of the CPLD. This connector is not intended to be used outside the factory.

### 3.7 System LEDs

The TMS320C6416 DSK has four system light emitting diodes (LEDs). These LEDs indicate various conditions on the DSK. These function of each LED is shown in the table below.

**Table 8: System LEDs**

Reference Designator	Color	Function	On Signal State
D4	Green	USB Emulation in use. When External JTAG Emulator is used this LED is off.	1
D3	Green	+5 Volt present	1
D6	Orange	RESET Active	1
DS201	Green	USB Active, Blinks during USB data transfer	1

### **3.8 Reset Switch**

There are three resets on the TMS320C6416 DSK. The first reset is the power on reset. This circuit waits until power is within the specified range before releasing the power on reset pin to the TMS320C6416.

External sources which control the reset are push button SW2, and the on board embedded USB JTAG emulator.

# Appendix A

## Schematics

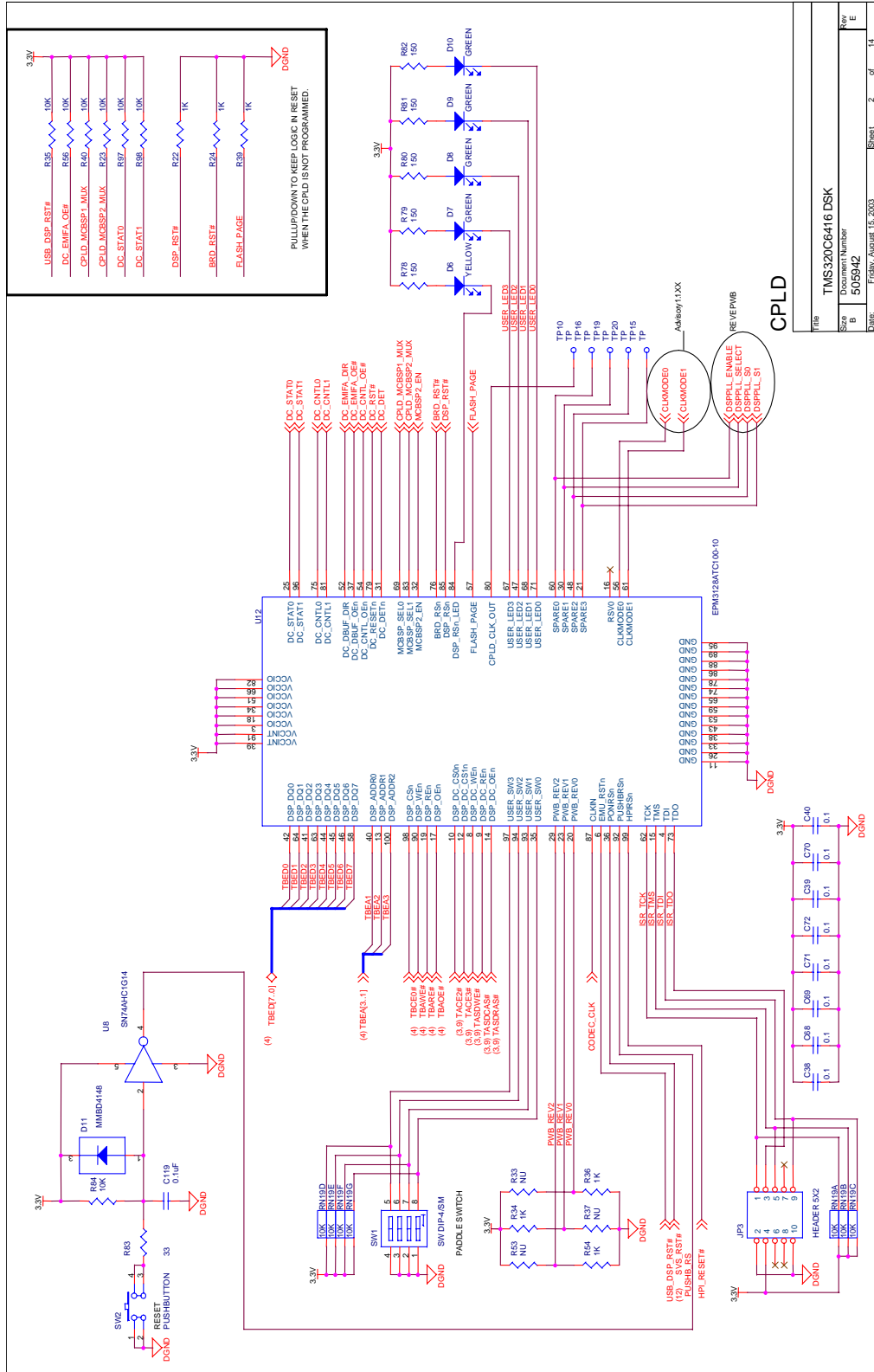
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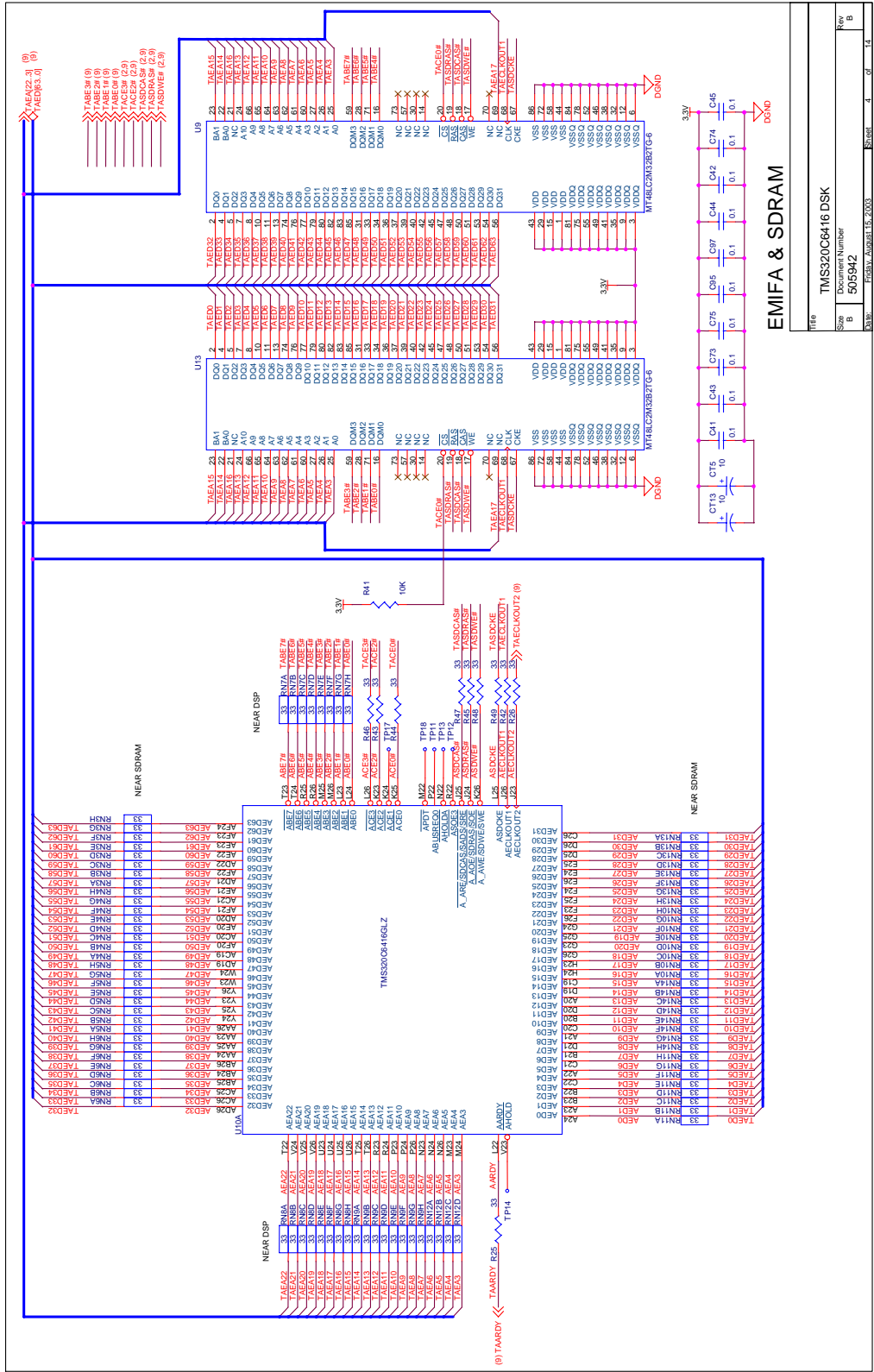
This appendix contains the schematics for the TMS320C6416 DSK. Board components with designators between 200 and 299 (e.g. DS201, R211) are part of Spectrum Digital's embedded JTAG emulator and are not included in these schematics.

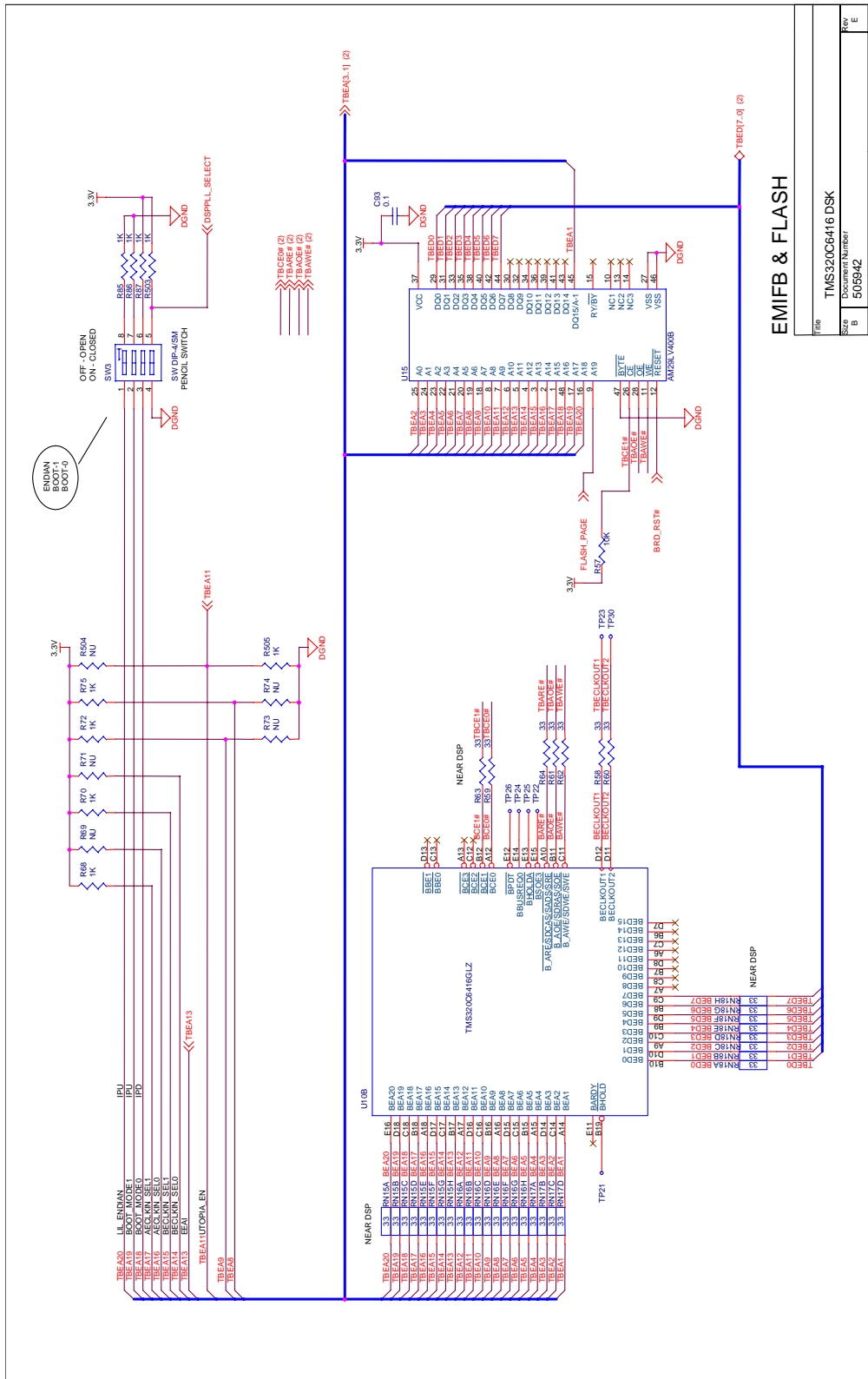


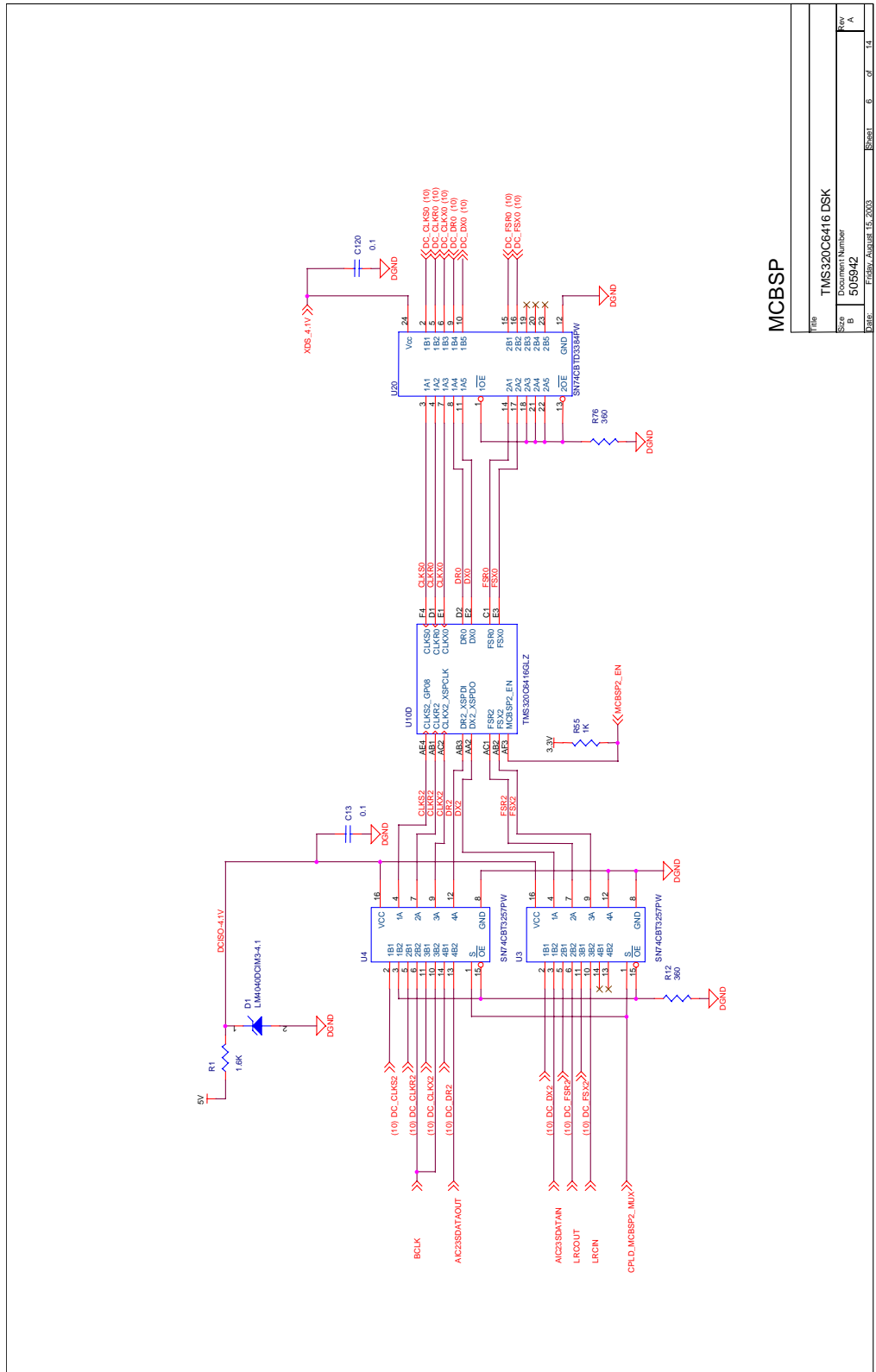


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Rev	E





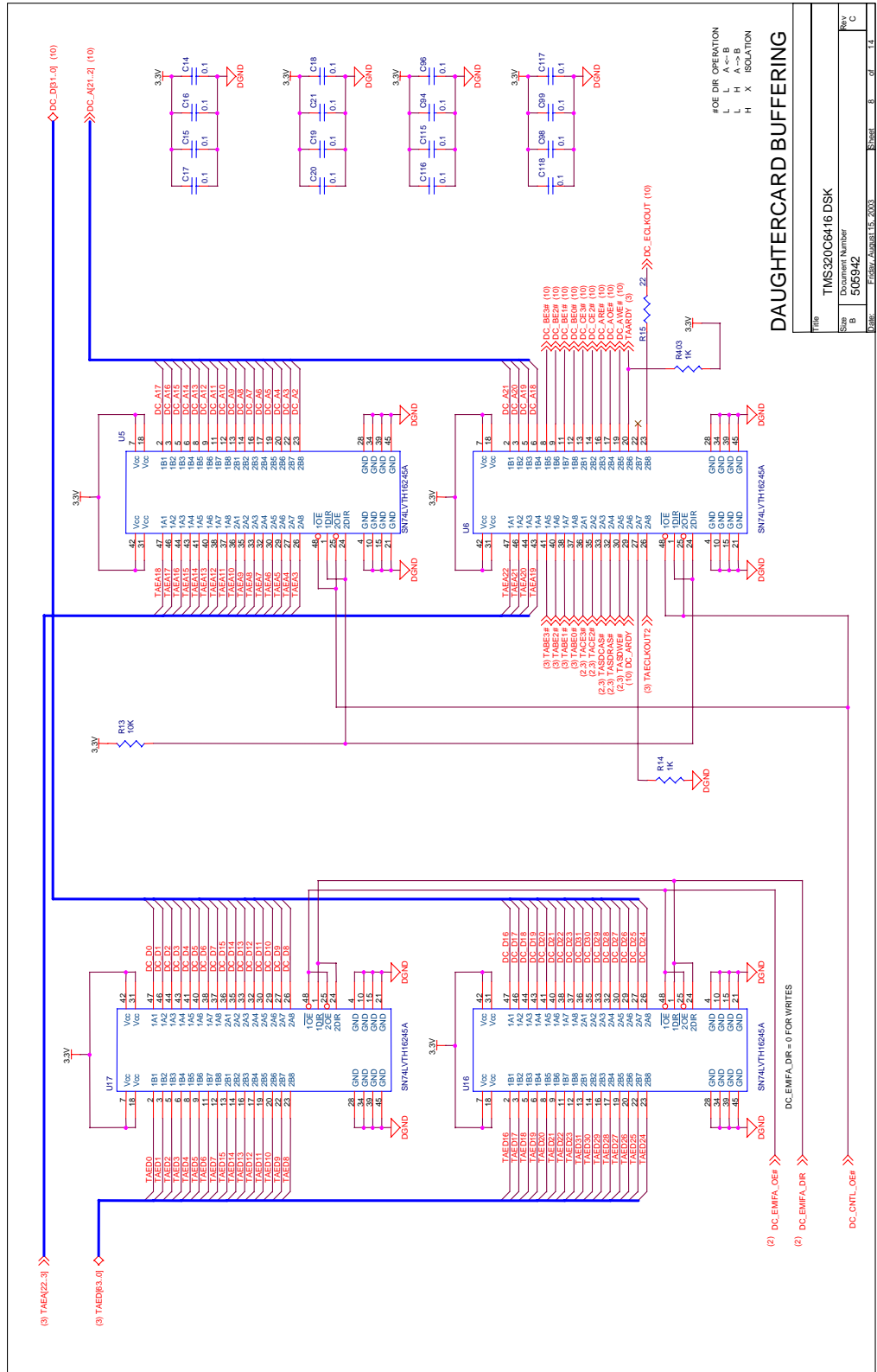


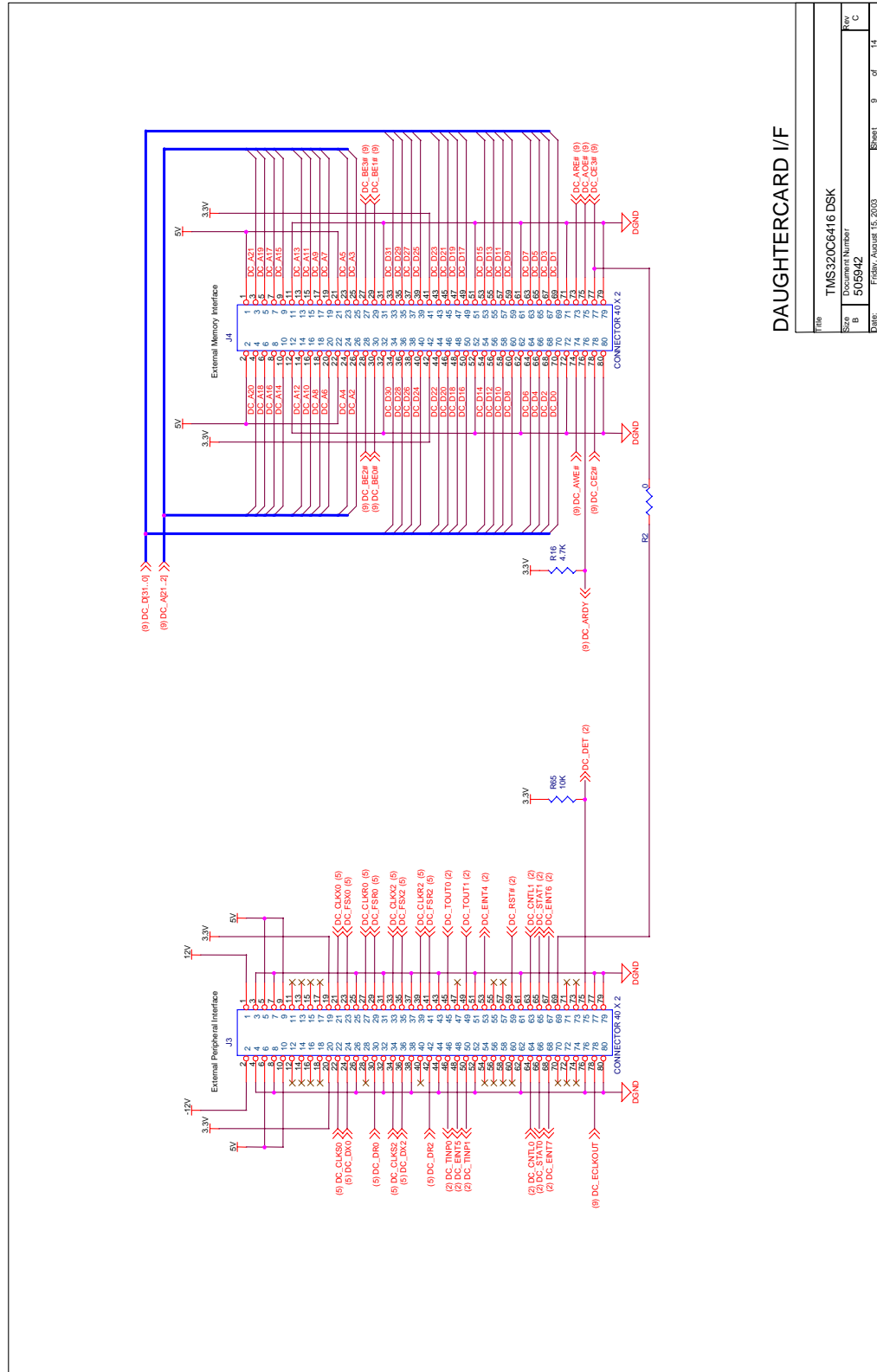


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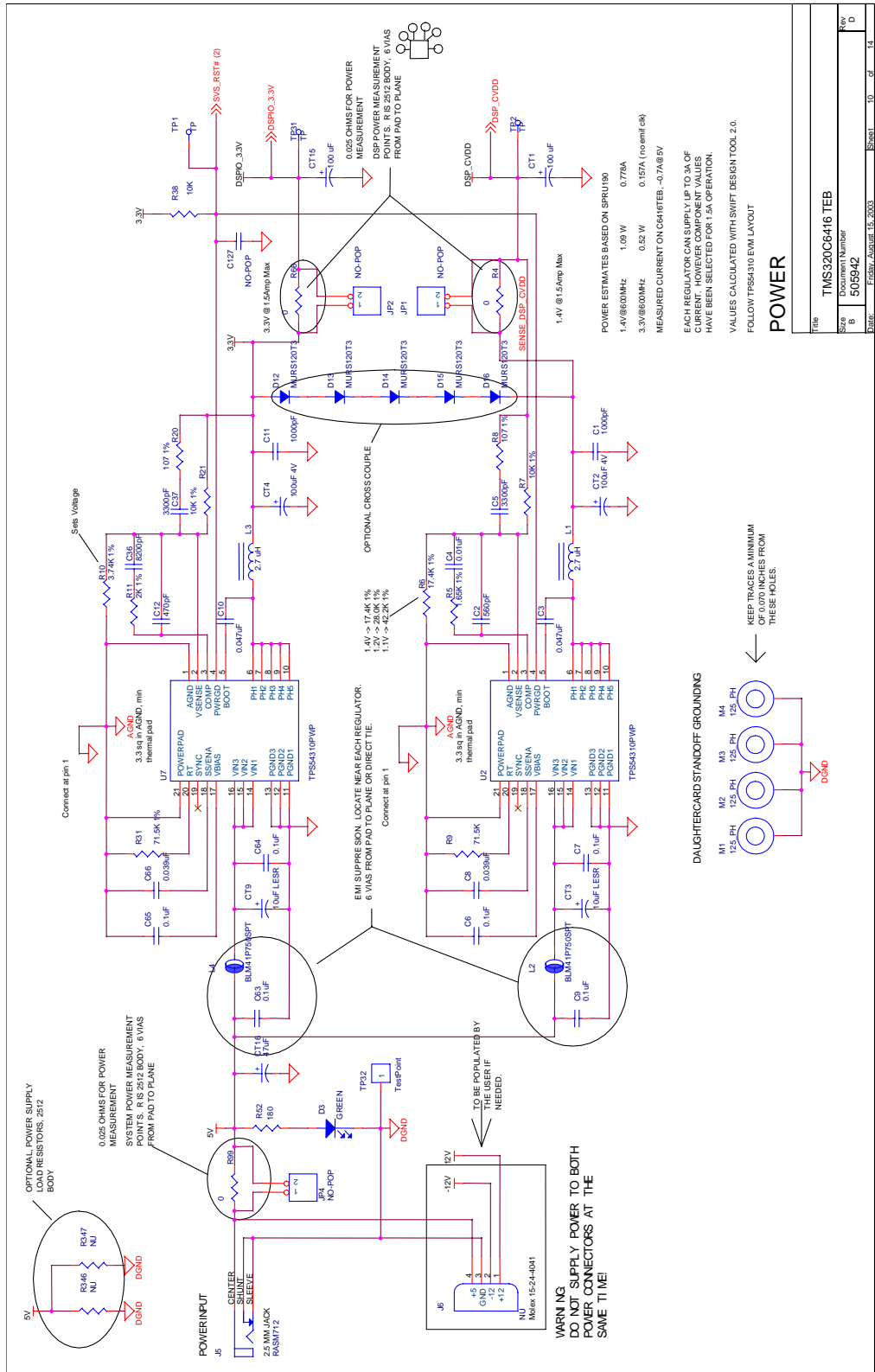






DAUGHTERCARD I/F

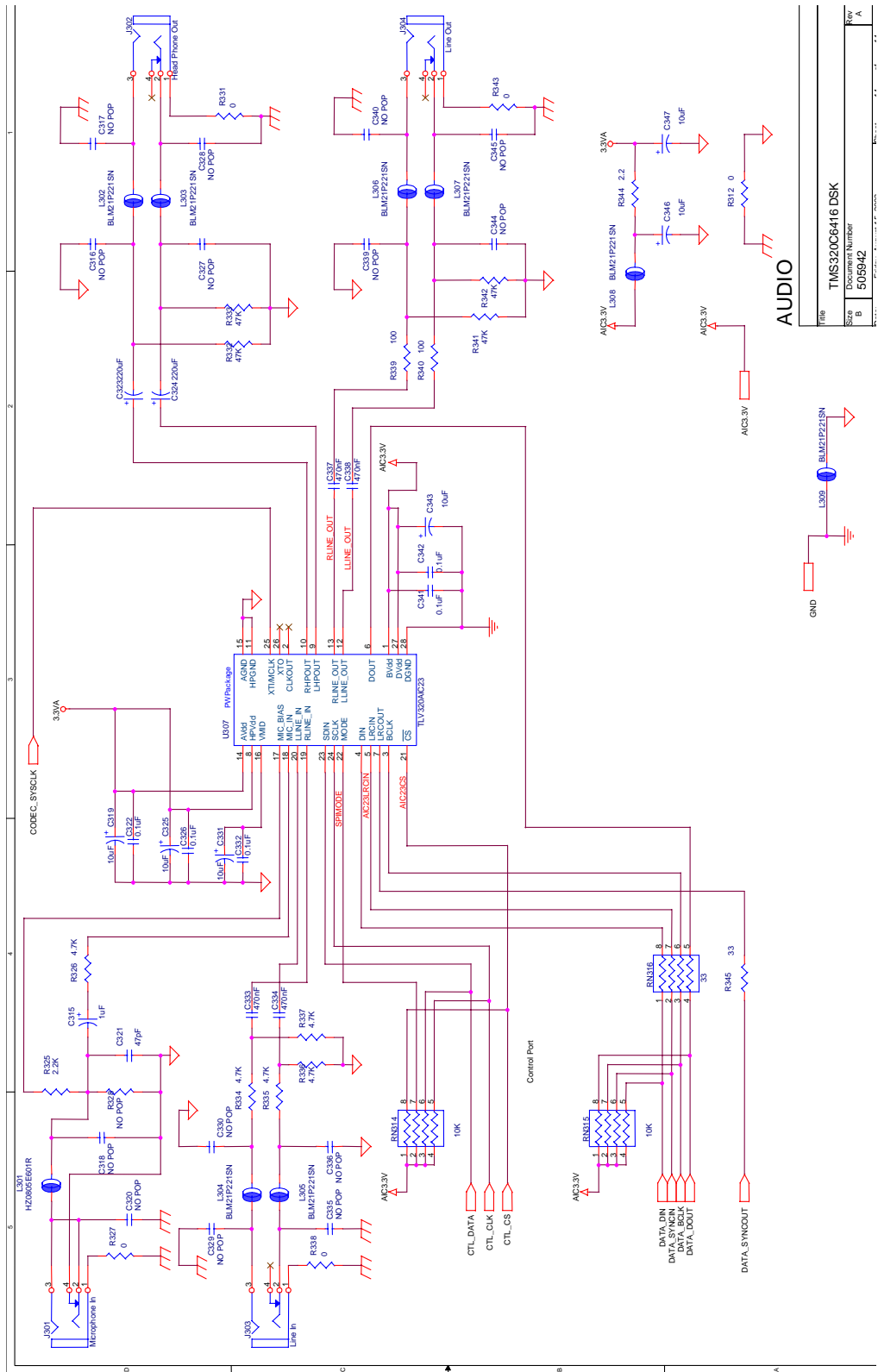
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AUDIO

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# Appendix B

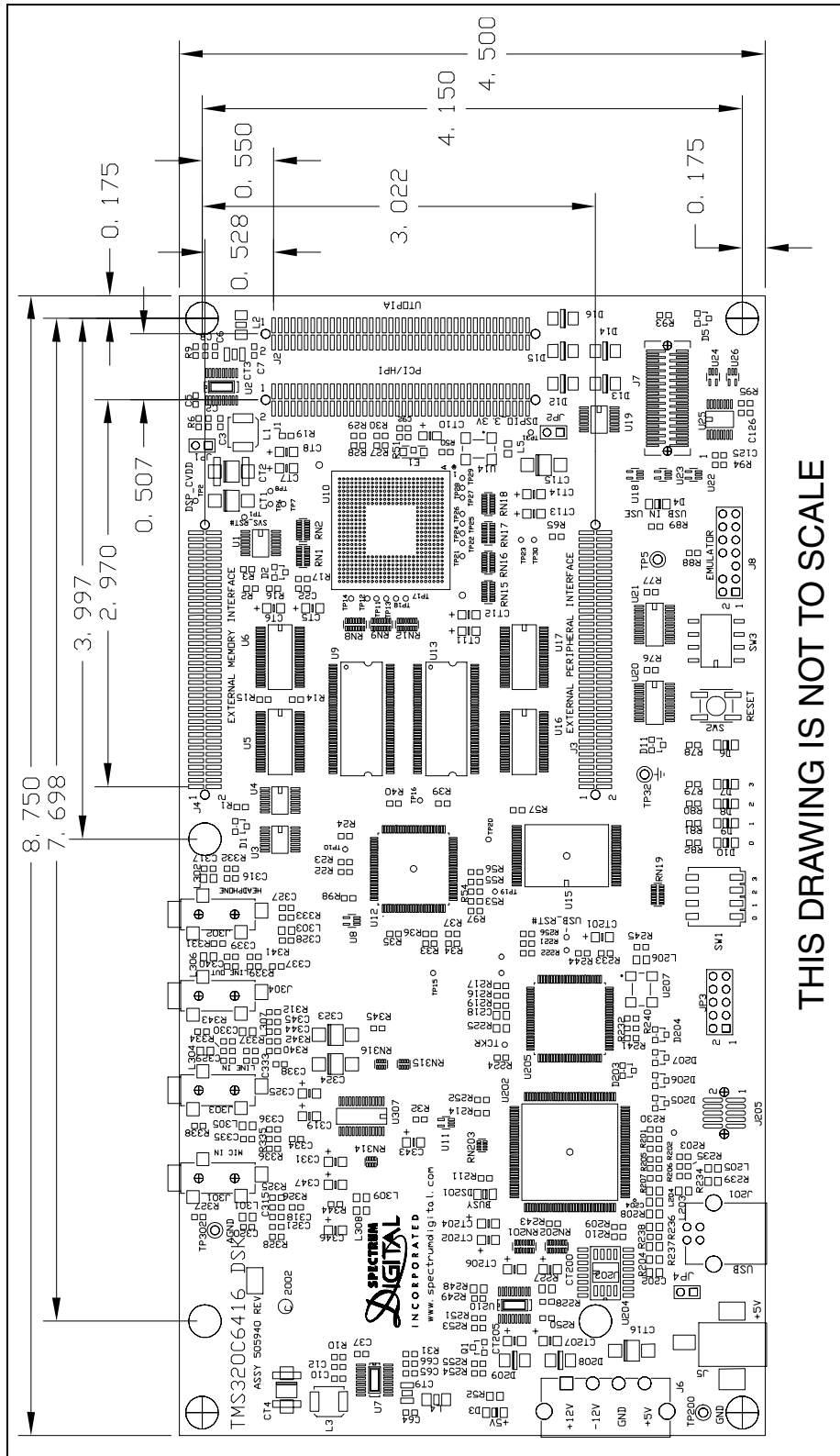
## Mechanical Information

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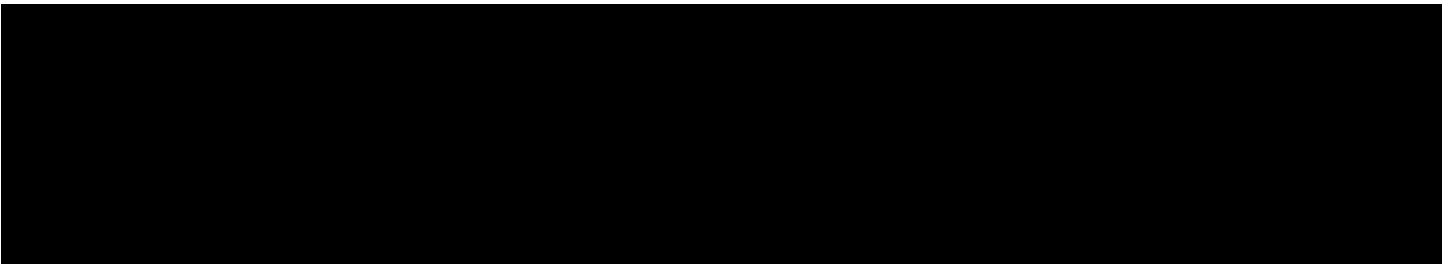
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This appendix contains the mechanical information about the TMS320C6416 DSK produced by Spectrum Digital.



THIS DRAWING IS NOT TO SCALE





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505945-0001 Rev. B