

TMS320C6455 ***Evaluation Module***

*Technical
Reference*

**TMS320C6455
Evaluation Module
Technical Reference**

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About This Manual

This document describes the board level operations of the TMS320C6455 DSP Evaluation Module (EVM). The EVM is based on the Texas Instruments TMS320C6455 Digital Signal Processor.

The TMS320C6455 EVM is a table top card to allow engineers and software developers to evaluate certain characteristics of the TMS320C6455 DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The TMS320C6455 Evaluation Module will sometimes be referred to as the EVM, C6455 EVM, or TMS320C6455 EVM.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

```
equations  
!rd = !strobe&rw;
```

Information About Cautions

This book may contain cautions.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320C64xx DSP CPU Reference Guide
Texas Instruments TMS320C64xx DSP Peripherals Reference Guide

Table 1: Manual History

Revision	History
A	Initial Release
B	Changed CLKIN to 50 Mhz. for DSK and Mezzanine boards Fixed swizzle on daughter card interrupts
C	Corrected DSK connector documentation Replaced sheets 4,5 in DSK schematics

Chapter 1

Overview of the TMS320C6455 Evaluation Module

Chapter One provides an overview description of the TMS320C6455 Evaluation Module along with the key features and a block diagram of the evaluation platform.

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1.1 Key Features

The C6455 Evaluation Module (EVM) is a high performance standalone development platform that enables users to evaluate and develop applications for the TI C64xx DSP family. The EVM also serves as a hardware reference design for the TMS320C6455 DSP. The EVM is made up of two circuit boards; the C6455 DSK base board with the Mezzanine connector populated, and a C6455 AMCC type Mezzanine board.

Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.

This Technical Reference Manual discusses both boards separately. Chapters 2-4 and appendices A,B provide information on the DSK C6455 board. Chapters 5,6 and appendices C,D have information on the C6455 Mezzanine card.

The figure below shows the two boards joined together to make up the EVM platform.

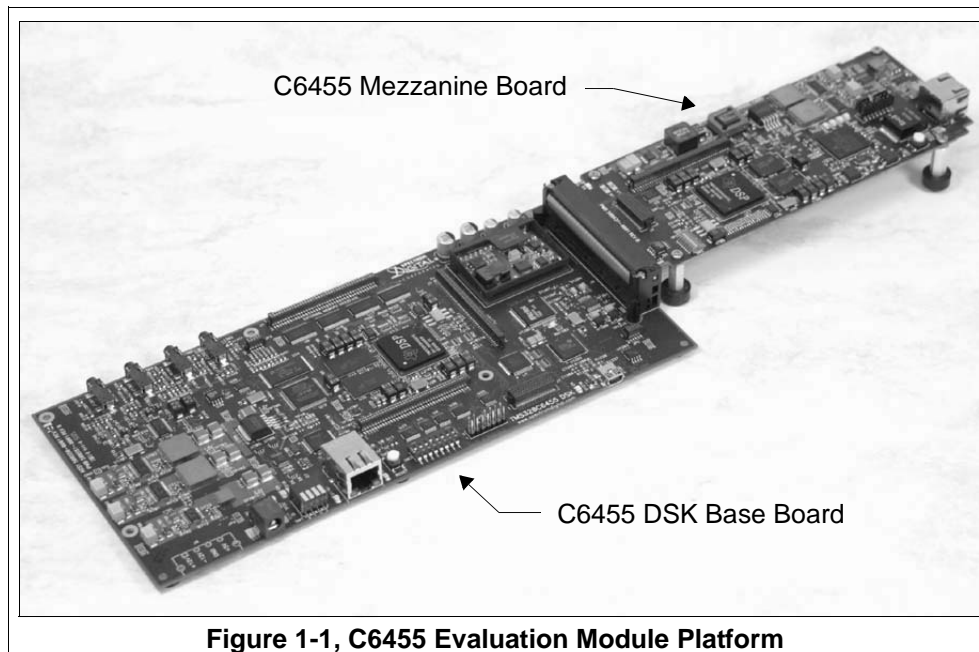
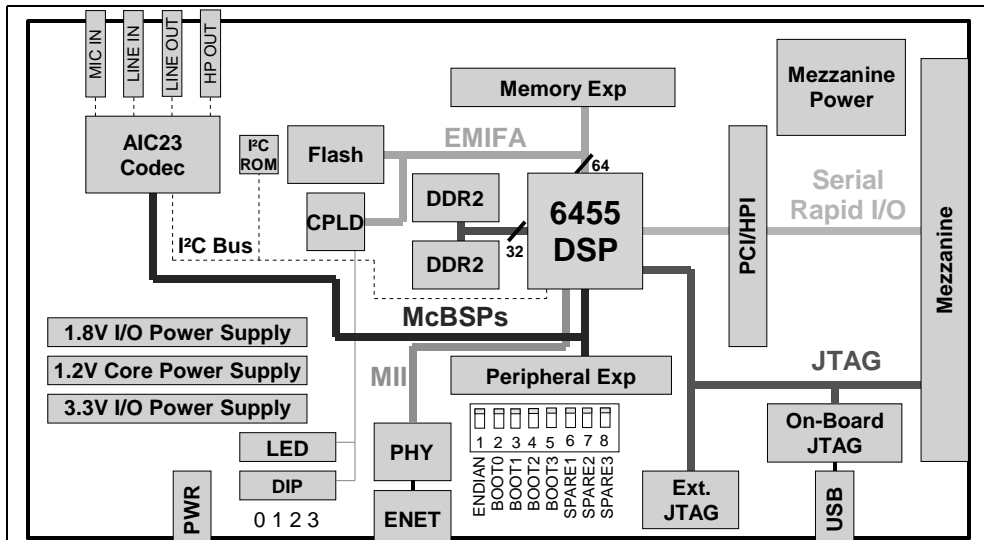
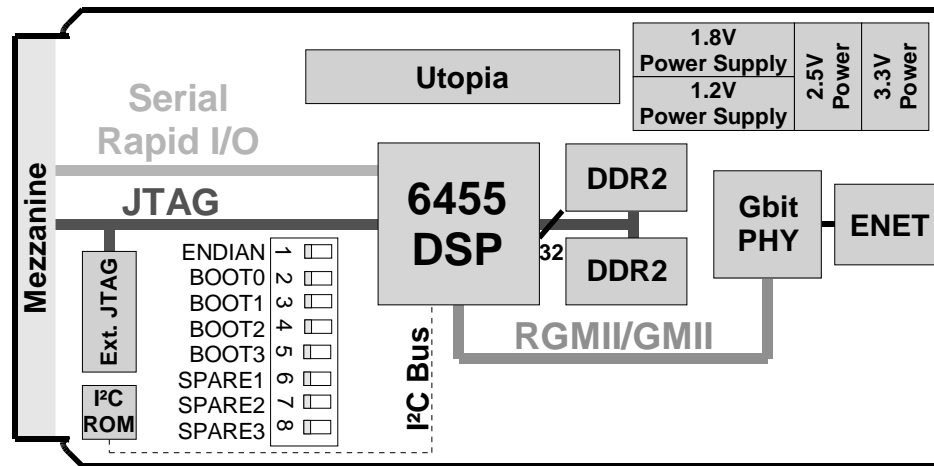


Figure 1-1, C6455 Evaluation Module Platform

The figures below provide block diagrams of the DSK portion and Mezzanine portion of the C6455 EVM platform.



Block Diagram of DSK Portion of C6455 EVM Platform



Block Diagram of Mezzanine Portion of C6455 EVM Platform

Figure 1-2, Block Diagrams of C6455 EVM Platform

The key features of the of the EVM platform include:

- A DSP Starter Kit (DSK) board (Mezzanine connector populated) with the following features:
 - A Texas Instruments TMS320C6455 DSP operating at 1 Gigahertz.
 - An AIC23 stereo codec
 - 128 Mbytes of DDR2 memory
 - 4M bytes of non-volatile Flash memory
 - 10/100 MBPs ethernet interface
 - I²C Serial ROM
 - 4 user accessible LEDs and DIP switches
 - Software board configuration through registers implemented in CPLD
 - Configured boot options and clock input selection
 - Standard expansion connectors for daughter card use
 - JTAG emulation through on-board JTAG emulator with USB host interface or external emulator
 - Single voltage power supply (+5V)

- A Mezzanine board with the following features:
 - A Texas Instruments TMS320C6455 DSP operating at 1 Gigahertz.
 - 128 Mbytes of DDR2 memory
 - 10/100 MBPs ethernet interface
 - I²C Serial ROM
 - Configurable boot options and clock input selection

1.2 Functional Overview of the TMS320C6455 EVM Platform

The EVM Platform is made up of two printed circuit boards (DSK and Mezzanine) connected to each other via a Serial Rapid I/O (SRIO) connector. Each board has a Texas Instruments C6455 DSP running at 1 Ghz.

The functional overviews of the DSK and mezzanine boards are in chapters 2 and 5 respectively.

1.3 Basic Operation

The EVM Platform is designed to work with TI's Code Composer Studio development environment and ships with a version specifically tailored to work with the board. Code Composer communicates with the board through the on-board JTAG emulator. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

After the install is complete, follow these steps to run Code Composer. Make sure the Mezzanine board is plugged into the DSK board. The DSK board must be fully connected to launch the EVM version of Code Composer.

- 1) Connect the included power supply to the DSK board.
- 2) Connect the DSK to your PC with a standard USB cable (also included).
- 3) Launch Code Composer from its icon on your desktop.

Detailed information about the EVM including a tutorial, examples and reference material is available in the EVM's help file.

1.4 Memory Maps

Each processor in the EVM platform has its own memory map. For the DSK board's memory map please refer to chapter 2. The Mezzanine board's memory map is discussed in chapter 5.

1.5 Configuration Switch Settings

The configuration switch settings for the EVM platform are discussed in chapter 2. The DSK has 8 configuration switches that allows users to control the operational state of the DSP when it is released from reset. The configuration switch block is labeled SW3 on the DSK board, next to the reset switch.

1.6 Bootmode Configurations

The bootmode configurations for each processor in the EVM platform are described in chapters 2 and 5.

1.7 Power Supply

The DSK operates from a single +5V external power supply connected to the main power input (J5). Internally, the +5V input is converted into +1.5, +1.8V and +3.3V using multiple voltage regulators. The +1.2V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and all other chips on the board. The +1.8 volt supply is used to support DDR2 memories. The power connector is a 2.5mm barrel-type plug.

The DSK provides +3.3V, up to 1A for the daughter card. The +3.3V supply is derived from the +5V power source via the main +3.3 volt regulator. It is also possible to provide the daughter card with +12V and -12V when the external power connector (J6) is used.

Chapter 2

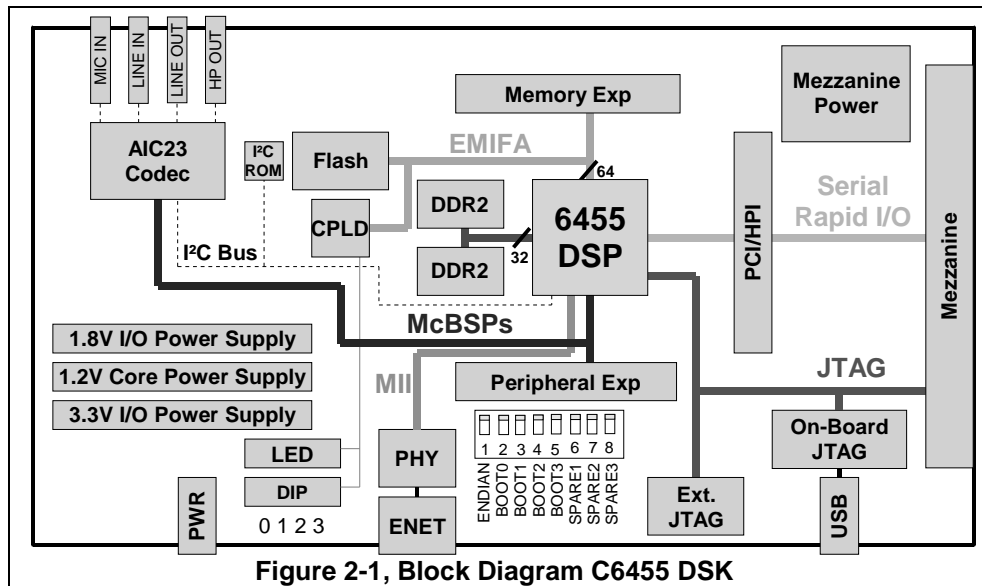
Introduction to the TMS320C6455 DSK

Chapter two provides a description of the TMS320C6455 DSK along with the key features and a block diagram of the circuit board.

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2.1 Key Features

The C6455 DSK is a high performance standalone development platform that enables users to evaluate and develop applications for the TI C64xx DSP family. The DSK also serves as a hardware reference design for the TMS320C6455 DSP. Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.



The DSK comes with a full compliment of on-board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments TMS320C6455 DSP operating at 1 Gigahertz.
- An AIC23 stereo codec
- 128 Mbytes of DDR2 memory
- 4M bytes of non-volatile Flash memory
- 10/100 MBPs ethernet interface
- I²C Serial ROM
- 4 user accessible LEDs and DIP switches
- Software board configuration through registers implemented in CPLD
- Configured boot options and clock input selection
- Standard expansion connectors for daughter card use

- JTAG emulation through on-board JTAG emulator with USB host interface or external emulator
- Single voltage power supply (+5V)

2.2 Functional Overview of the TMS320C6455 DSK

The DSP on the C6455 DSK interfaces to on-board peripherals through the 64-bit wide EMIFA configured for 32 bit accesses. The CPLD and daughter card expansion connectors are connected to EMIFA. The DDR2 memory is on its own dedicated EMIF.

An on-board AIC23 codec allows the DSP to transmit and receive analog signals. I²C is used for the codec control interface and McBSP1 is used for data. Analog I/O is done through four 3.5mm audio jacks that correspond to microphone input, line input, line output and headphone output. The codec can select the microphone or the line input as the active input. The analog output is driven to both the line out (fixed gain) and headphone (adjustable gain) connectors. McBSP0 and McBSP1 can be re-routed to the expansion connectors in software.

A programmable logic device called a CPLD is used to implement glue logic that ties the board components together. The CPLD also has a register based user interface that lets the user configure the board by reading and writing to the CPLD registers.

A Flash memory is mapped into CE3 space. The Flash contains power on self test as shipped, or can be programmed for user programs.

The DSK has a 10/100 mbit Phy which is connected to the DSP's on board EMAC.

The DSK includes 4 LEDs and 4 position DIP switch as a simple way to provide the user with interactive feedback. Both are accessed by reading and writing to the CPLD registers.

An included 5V external power supply is used to power the board. On-board switching voltage regulators provide the 1.2V DSP core voltage, 1.8V for DDR, and 3.3V I/O supplies. The board is held in reset until these supplies are within operating specifications.

Code Composer communicates with the DSK through an embedded JTAG emulator with a USB host interface. The DSK can also be used with an external emulator through the external 60 pin and 14 pin JTAG connectors.

2.3 Basic Operation

The DSK is designed to work with TI's Code Composer Studio development environment and ships with a version specifically tailored to work with the board. Code Composer communicates with the board through the on-board JTAG emulator. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

After the install is complete, follow these steps to run Code Composer. The DSK must be fully connected to launch the DSK version of Code Composer.

- 1) Connect the included power supply to the DSK.
- 2) Connect the DSK to your PC with a standard USB cable (also included).
- 3) Launch Code Composer from its icon on your desktop.

Detailed information about the DSK including a tutorial, examples and reference material is available in the DSK's help file.

2.4 Memory Map

The C64xx family of DSPs has a large byte addressable address space. Program code and data can be placed anywhere in the unified address space. Addresses are always 32-bits wide.

The memory map shows the address space of a generic 6455 processor on the left with specific details of how each region is used on the right. By default, the internal memory sits at the beginning of the address space. Portions of memory can be remapped in software as L2 cache rather than fixed RAM.

EMIFA (External Memory Interface A) has 4 separate addressable regions called chip enable spaces (CE2-CE5). The DDR2 occupies CE0 of DDR2 Memory bus. The CPLD and Flash are mapped to CE2 and CE3 of EMIFA respectively. Daughter cards use CE4 and CE5 of EMIFA.

Address	Generic 6455 Address Space	6455 DSK
0x00000000	Internal Memory	Internal Memory
0x00100000	Reserved Space or Peripheral Regs	Reserved or Peripheral
0xA0000000	EMIFA CE2	CPLD
0xB0000000	EMIFA CE3	Flash
0xC0000000	EMIFA CE4	Daughter Card
0xD0000000	EMIFA CE5	
0xE0000000	DDR2 CE0	DDR2 Memory

Figure 2-2, Memory Map, C6455 DSK

2.5 Configuration Switch Settings

The DSK has 8 configuration switches that allows users to control the operational state of the DSP when it is released from reset. The configuration switch block is labeled SW3 on the DSK board, next to the reset switch.

Configuration switch 1 controls the endianness of the DSP. The factory default is little endian. The settings of switch 1 are shown in the table below.

Table 1: Endian Configuration Switch Settings

SW3-1	Configuration Description
Off	Little endian *
On	Big endian

* Default

Switches 2-5 configure the boot mode that will be used when the DSP starts executing. These boot modes are shown in the table below. The default boot mode is EMIFA 8 bit ROM Boot.

Table 2: Boot Load Configuration Switch Settings

SW3-5 AE19	SW3-4 * AE18	SW3-3 AE17	SW3-2 AE16	Configuration Description
Off	Off	Off	Off	No Boot
Off	Off	Off	On	Host Boot HPI
Off	Off	On	Off	Reserved
Off	Off	On	On	Reserved
Off	On	Off	Off	EMIFA 8 bit ROM Boot *
Off	On	Off	On	I ² C Boot Master
Off	On	On	Off	I ² C slave
Off	On	On	On	Host Boot PCI
On	x	x	x	Serial Rapid I/O Boot see DSP data sheet for more details

** Default

On revision "C" and newer boards the switch positions 6-8 are spare switches. The CLKIN frequency is now set to a fixed 50 Mhz. oscillator.

2.6 Bootmode Configurations

The C6455 uses the address lines to configure the device configuration at RESET. Although many of these configurations can be changed in software via internal DSP configuration registers, the defaults for the DSK are shown in the table below.

Table 3: Bootmode Configurations

Config Pin Name	Function	Controlled By
AE19	Boot Mode 3	SW3-5
AE18	Boot Mode 2	SW3-4
AE17	Boot Mode 1	SW3-3
AE16	Boot Mode 0	SW3-2
AE15	AECLKIN Selected	Resistor Strap
AE14	HPI 32 bit Mode Selected	Resistor Strap
AE13	Endian Mode	SW3-1
AE12	Ethernet MAC Enabled	Resistor Strap
AE11	Reserved	Resistor Strap
AE10	EMAC MDIO/MII Mode	Resistor Strap
AE9	EMAC MDIO/MII Mode	Resistor Strap
AE8	PCI I ² C ROM Enable	Resistor Strap
AE7	Reserved	Resistor Strap
AE6	PCI 33 Mhz.	Resistor Strap
AE5	McBSP1 Enabled	Resistor Strap
AE4	SYSCLK4 Output	Resistor Strap
AE3	Reserved	Resistor Strap
AE2	CFGGP2	Resistor Strap
AE1	CFGGP1	Resistor Strap
AE0	CFGGP0	Resistor Strap
ABA1	EMIFA Enabled	Resistor Strap
ABA0	DDR Enabled	Resistor Strap

2.7 Power Supply

The DSK operates from a single +5V external power supply connected to the main power input (J5). Internally, the +5V input is converted into +1.5, +1.8V and +3.3V using multiple voltage regulators. The +1.2V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and all other chips on the board. The +1.8 volt supply is used to support DDR2 memories. The power connector is a 2.5mm barrel-type plug.

The DSK provides +3.3V, up to 1A for the daughter card. The +3.3V supply is derived from the +5V power source via the main +3.3 volt regulator. It is also possible to provide the daughter card with +12V and -12V when the external power connector (J6) is used.

The DSK also supplies +12 volts to the AMCC connector. This is the voltage supply to the Mezzanine Board. The +12 volts is created by a +5V to +12V converter, PWR1.

Chapter 3

Board Components

This chapter describes the operation of the major board components on the TMS320C6455 DSK.

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3.1 CPLD (Programmable Logic)

The C6455 DSK uses an Altera EPM3128TC100-10 Complex Programmable Logic Device (CPLD) device to implement:

- 5 Memory-mapped control/status registers that allow software control of various board features.
- Address decode and memory access logic.
- Control of the daughter card interface and signals.
- Assorted "glue" logic that ties the board components together.

3.1.1 CPLD Overview

The CPLD logic is used to implement functionality specific to the DSK. Your own hardware designs will likely implement a completely different set of functions or take advantage of the DSPs high level of integration for system design and avoid the use of external logic completely.

The CPLD implements simple random logic functions that eliminate the need for additional discrete devices. In particular, the CPLD aggregates the various reset signals coming from the reset button and power supervisors and generates a global reset.

The EPM3128TC100-10 is a 3.3V (5V tolerant), 100-pin QFP device that provides 128 macrocells, 80 I/O pins, and a 10 ns pin-to-pin delay. The device is EEPROM-based and is in-system programmable via a dedicated JTAG interface (a 10-pin header on the DSK). The CPLD source files are written in the industry standard VHDL (Hardware Design Language) and included with the DSK.

3.1.2 CPLD Registers

The 5 CPLD memory-mapped registers allows users to control CPLD functions in software. On the C6455 DSK the registers are primarily used to access the LEDs and DIP switches and control the daughter card interface. The registers are mapped into CE2 data space at address 0xA000000. They appear as 8-bit registers with a simple asynchronous memory interface. The following table gives a high level overview of the CPLD registers and their bit fields:

The table below shows the bit definitions for the 5 registers in CPLD.

Table 1: CPLD Register Definitions

Offset	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	USER_REG	USR_SW3 R	USR_SW2 R	USR_SW1 R	USR_SW0 R	USR_LED3 R/W 0(Off)	USR_LED2 R/W 0(Off)	USR_LED1 R/W 0(Off)	USR_LED0 R/W 0(Off)
1	DC_REG	DC_DET R	0	DC_STAT1 R	DC_STAT0 R	DC_RST R 0(No reset)	0	DC_CNTL1 R/W 0(low)	DC_CNTL0 R/W 0(low)
4	VERSION	CPLD_VER[3:0] R				0	BOARD_VERSION[2:0] R		
6	MISC	McBSP2_EN R (MCBSP2 enabled)	Spare3	Spare2	Spare1	Spare1	Resv 0	Resv 0	McBSP1 ON/OFF Board R/W 0 (Onboard)
7	MISC2	DSPA RSTST (Reset Status)	Resv 0	Resv 0	Resv 0	HUR RST EN	Ethernet PHY RST	CPUB Enable	CPUB PRSNT

3.1.3 USER_REG Register

USER_REG is used to read the state of the 4 DIP switches and turn the 4 LEDs on or off to allow the user to interact with the DSK. The DIP switches are read by reading the top 4 bits of the register and the LEDs are set by writing to the low 4 bits.

Table 2: CPLD USER_REG Register

Bit	Name	R/W	Description
7	USER_SW3	R	User DIP Switch 3(1 = Off, 0 = On)
6	USER_SW2	R	User DIP Switch 2(1 = Off, 0 = On)
5	USER_SW1	R	User DIP Switch 1(1 = Off, 0 = On)
4	USER_SW0	R	User DIP Switch 0(1 = Off, 0 = On)
3	USER_LED3	R/W	User-defined LED 3 Control (0 = Off, 1 = On)
2	USER_LED2	R/W	User-defined LED 2 Control (0 = Off, 1 = On)
1	USER_LED1	R/W	User-defined LED 1 Control (0 = Off, 1 = On)
0	USER_LED0	R/W	User-defined LED 0 Control (0 = Off, 1 = On)

3.1.4 DC_REG Register

DC_REG is used to monitor and control the daughter card interface. DC_DET detects the presence of a daughter card. DC_STAT and DC_CNTL provide simple communications with the daughter card through readable status lines and writable control lines.

The daughter card is released from reset when the DSP is released from reset. DC_RST can be used to put the card back in reset.

Table 3: DC_REG Register

Bit	Name	R/W	Description
7	DC_DET	R	Daughter Card Detect (1= Board detected)
6	0	R	Always 0
5	DC_STAT1	R	Daughter Card Status 1 (0=Low, 1 = High)
4	DC_STAT0	R	Daughter Card Status 0 (0=Low, 1 = High)
3	DC_RST	R/W	Daughter Card Reset (0=No Reset, 1 = Reset)
2	0	R	Always zero
1	DC_CNTL1	R/W	Daughter Card Control 1(0 = Low, 1 = High)
0	DC_CNTL0	R/W	Daughter Card Control 0(0 = Low, 1 = High)

3.1.5 VERSION Register

The VERSION register contains two read only fields that indicate the BOARD and CPLD versions. This register will allow your software to differentiate between production releases of the DSK and account for any variances. This register is not expected to change often, if at all.

Table 4: Version Register Bit Definitions

Bit #	Name	R/W	Description
7	CPLD_VER3	R	Most Significant CPLD Version Bit
6	CPLD_VER2	R	CPLD Version Bit
5	CPLD_VER1	R	CPLD Version Bit
4	CPLD_VER0	R	Least Significant CPLD Version Bit
3	0	R	Always 0
2	DSK_VER2	R	Most Significant DSK Board Version Bit
1	DSK_VER1	R	DSK Board Version Bit
0	DSK_VER0	R	Least Significant DSK Board Version Bit

3.1.6 MISC Register

The MISC register is used to provide software control for miscellaneous board functions. On the C6455 DSK, the MISC register controls how auxiliary signals are brought out to the daughter-card connectors.

McBSP1 is usually used as the control and data port of the on-board AIC23 codec. The power-on state of this bit (0) represents that configuration. Set MCBSP0SEL to route the McBSP1 to the daughter card connectors rather than the codec.

The scratch bits are unused. They can be set to any value.

Table 5: MISC Register

Bit	Name	R/W	Description
7	Reserved	R	
6	Spare3	R	Spare switch
5	Spare2	R	Spare switch
4	Spare1	R	Spare switch
3	Spare0	R	Spare switch
2	Reserved	R	
1	Reserved	R	
0	MCBSP1SEL	R/W	McBSP1 on/off board (0 = on-board, 1 = off-board)

3.1.7 MISC2 Register

MISC2 register is used for factory test and EVM functions when a C64xx AMCC mezzanine card is used.

This register also contains a bit for resetting the on board PHY.

Bits 0 and 1 are used for EVM configurations. Bit 0 is used to detect that a mezzanine card is plugged into the AMCC slot which is not populated on a DSK. Bit 1 enables the AMCC mezzanine card. When driven to a zero the AMCC card is enabled.

Bit 3 provides a mechanism to reset the ethernet PHY. Writing as 1 resets the on board ethernet PHY.

Bits 4 and 7 are used for factory tests, and the remaining bits are reserved for future use.

Table 6: MISC2 Register

Bit	Name	R/W	Description
7	DSPA RSTST	W	DSP A Reset Status (0 = Not in reset, 1 = In Reset), Factory Test
6	Reserved	R	Not Used
5	Reserved	R	Not Used
4	Reserved	R	Not Used
3	Reserved	R	User-defined LED 3 Control (0 = Off, 1 = On)
2	Ethernet PHY RST	R/W	Ethernet PHY reset Enable (0 = Not Reset, 1 = Reset)
1	CPUB Enable	W	CPU B Reset (0 = Not Reset, 1 = Reset)
0	CPUB PRSNT	R	CPU B Present (0 = Not present, 1 = Present)

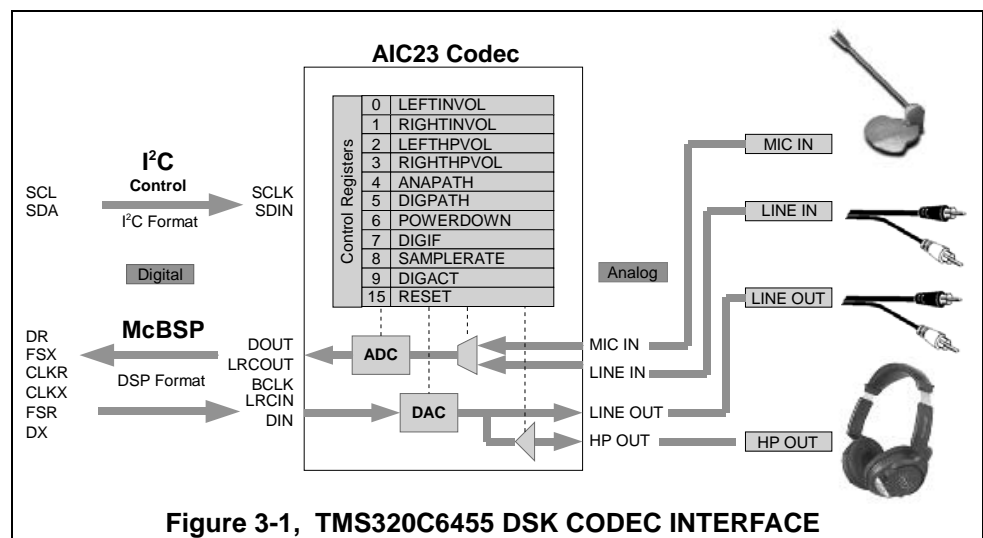
3.2 AIC23 Codec

The DSK uses a Texas Instruments AIC23 (part #TLV320AIC23) stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line and headphone outputs so the user can hear the output.

The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. The C6455's I²C interface is used as the unidirectional control channel. The control channel is only used when configuring the codec, it is generally idle when audio data is being transmitted,

McBSP1 is used as the bi-directional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The DSK examples generally use a 55-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the DSP side. The preferred serial format is DSP mode which is designed specifically to operate with the McBSP ports on TI DSPs.

The codec has a 12MHz system clock. The 12MHz system clock corresponds to USB sample rate mode, named because many USB systems use a 12MHz clock and can use the same clock for both the codec and USB controller. The internal sample rate generate subdivides the 12MHz clock to generate common frequencies such as 48KHz, 44.1KHz and 8KHz. The sample rate is set by the codec's SAMPLERATE register. The figure below shows the codec interface on the C6455 DSK.



3.3 DDR2 Memory

The DSK uses a pair of industry standard 512 megabit DDR2 in CE0. The two devices are used in parallel to create a 32-bit wide interface. Total available memory is 128 megabytes, and is accessible from addresses 0xE0000 0000 to 0xE800 0000.

The DSK uses a factory setting DDR2 clock at 250 MHz. The integrated DDR2 controller is started by configuring the EMIF in software. Timings can be found in the DDR2 data sheet and the DSK help file.

3.4 Flash Memory

The DSK uses a 4 Mbyte external Flash as a boot option. It is connected to CE3 of EMIFA with an 8-bit interface, and is accessible from addresses 0xB0000 0000 to 0xB01F FFFF. Flash is a type of memory which does not lose its contents when the power is turned off. When read it looks like a simple asynchronous read-only memory (ROM). Flash can be erased in large blocks commonly referred to as sectors or pages. Once a block has been erased each word can be programmed once through a special command sequence. After that the entire block must be erased again to change the contents.

3.5 LEDs and DIP Switches

The DSK includes 4 software accessible LEDs (D7-D10) and DIP switches (SW1) that provide the user a simple form of input/output. Both are accessed through the CPLD USER_REG register.

3.6 Ethernet Interface

An Intel LTX971ACE 10/100 Mbps PHY is connected to the DSP's internal EMAC controller. There are 2 status LEDs which detail the status of the ethernet link.

3.7 I²C ROM

The DSK incorporates a 1 Mbit I²C ROM. The ROM can be used for general storage or configured as a boot device for the DSP.

3.8 Daughter Card Interface

The DSK provides three expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their DSK platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are for memory, peripherals, and the Host Port Interface (HPI)

The memory connector provides access to the DSP's asynchronous EMIF signals to interface with memories and memory mapped devices. It supports byte addressing on 32 bit boundaries. The peripheral connector brings out the DSP's peripheral signals like McBSPs, timers, and clocks. Both connectors provide power and ground to the daughter card.

The HPI is a high speed interface that can be used to allow multiple DSPs to communicate and cooperate on a given task. The HPI connector brings out the HPI specific control signals as well as a PCI multiplexed interface.

Most of the expansion connector signals are buffered so that the daughter card cannot directly influence the operation of the DSK board. The use of TI low voltage, 5V tolerant buffers, and CBT interface devices allows the use of either +5V or +3.3V devices to be used on the daughter card.

Other than the buffering, most daughter card signals are not modified on the board. However, a few daughter card specific control signals like DC_RESET and DC_DET exist and are accessible through the CPLD DC_REG register. The DSK also multiplexes the McBSP1 for on board or external use. This function is controlled through the CPLD MISC register.

3.9 DSP and EMIFA Clock Generation

The C6455 DSK uses the internal DSP dividers to select the user PLL frequency, and multiple oscillators. This allows the DSK to support 600, 725, 850, 1000, and 1200 megahertz CPU clocks. However, the default configuration is 1 gigahertz and the software shipped with the DSK assumes the default configuration.

3.10 JTAG Interfaces

The DSK supports embedded emulation controller as its primary debug channel. However it has an option to support 14 pin and 60 pin TI style JTAG connections for external emulators. When either the 14 pin or 60 pin interface is plugged into the DSK the on board embedded emulator is disabled. The 60 pin interface also supports trace functions when used with the appropriate trace emulation platform.

Chapter 4

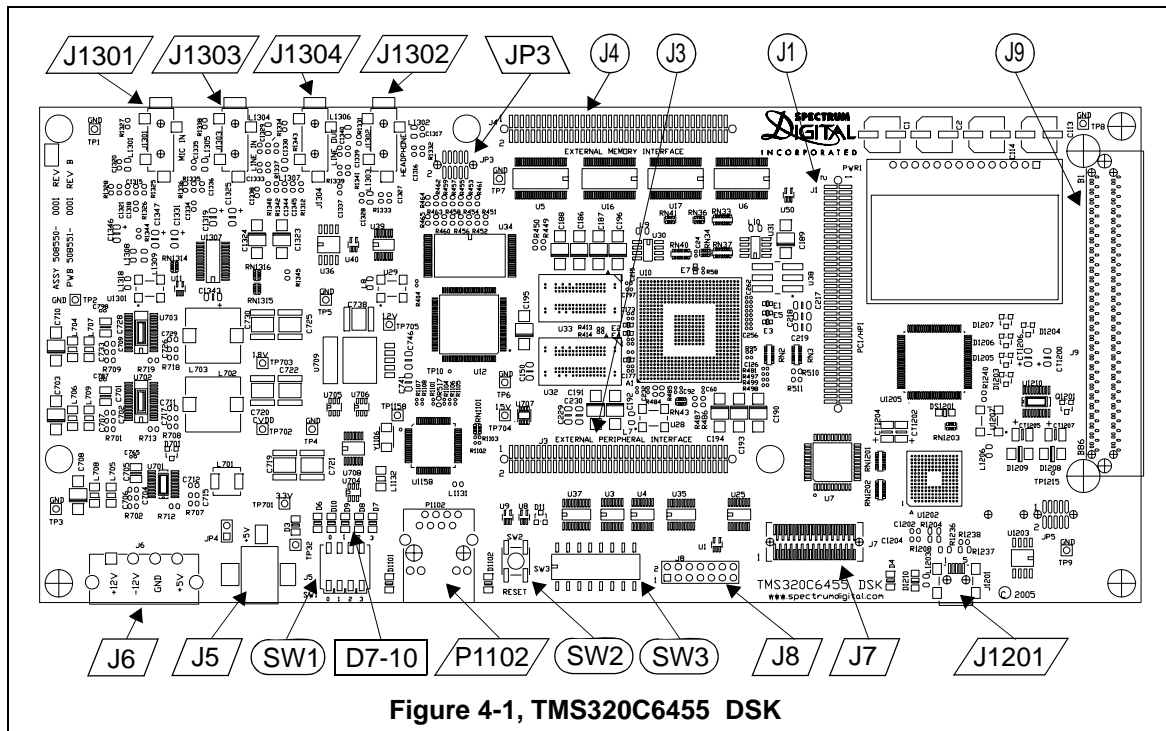
Physical Description

This chapter describes the physical layout of the TMS320C6455 DSK and its connectors.

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4.1 Board Layout

The C6455 DSK is a 10.0 x 4.5 inch (254 x 115 mm.) multi-layer board which is powered by an external +5 volt only power supply. Figure 4-1 shows the layout of the C6455 DSK.



4.2 Connector Index

The TMS320C6455 DSK has many connectors which provide the user access to the various signals on the DSK.

Table 1: TMS320C6455 DSK Connectors

Connector	# Pins	Function
J4	80	Memory
J3	80	Peripheral
J1	80	HPI
J1301	3	Microphone
J1303	3	Line In
J1304	3	Line Out
J1302	3	Headphone
J5	2	+5 Volt
J6 *	4	Optional Power Connector
J7	80	Enhanced JTAG Connector
J8	14	External JTAG
J1201	5	USB Port
JP3	4	CPLD Programming
P1102	8	Ethernet
SW3	8	DSP Configuration Switch

Note: "*" Not populated

4.3 Expansion Connectors

The TMS320C6455 DSK supports three expansion connectors that follow the Texas Instruments interconnection guidelines. The expansion connector pinouts are described in the following three sections.

The three expansion connectors are all 80 pin 0.050 x 0.050 inches low profile connectors from Samtec or AMP. The Samtec SFM Series (surface mount) connectors are designed for high speed interconnections because they have low propagation delay, capacitance, and cross talk. The connectors present a small foot print on the DSK. Each connector includes multiple ground, +5V, and +3.3V power signals so that the daughter card can obtain power directly from the DSK. The peripheral expansion connector additionally provides both +12V and -12V to the daughter card. The recommended mating connector, whose part number is TFM-140-32-S-D-LC, is a surface mount connector that provides a 0.465" mated height.

Note: I is on an Input pin
 O is on an Output pin
 Z is on a High Impedance pin

4.3.1 J4, Memory Expansion Connector

Table 2: J4, Memory Expansion Connector

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	5V	Vcc	5V voltage supply pin	2	5V	Vcc	5V voltage supply pin
3	AEA19	O	EMIF address pin 21	4	AEA18	O	EMIF address pin 20
5	AEA17	O	EMIF address pin 19	6	AEA16	O	EMIF address pin 18
7	AEA15	O	EMIF address pin 17	8	AEA14	O	EMIF address pin 16
9	AEA13	O	EMIF address pin 15	10	AEA12	O	EMIF address pin 14
11	GND	Vss	System ground	12	GND	Vss	System ground
13	AEA11	O	EMIF address pin 13	14	AEA10	O	EMIF address pin 12
15	AEA9	O	EMIF address pin 11	16	AEA8	O	EMIF address pin 10
17	AEA7	O	EMIF address pin 9	18	AEA6	O	EMIF address pin 8
19	AEA5	O	EMIF address pin 7	20	AEA4	O	EMIF address pin 6
21	5V	Vcc	5V voltage supply pin	22	5V	Vcc	5V voltage supply pin
23	AEA3	O	EMIF address pin 5	24	AEA2	O	EMIF address pin 4
25	AEA1	O	EMIF address pin 3	26	AEA0	O	EMIF address pin 2
27	ABE3#	O	EMIF byte enable 3	28	ABE2#	O	EMIF byte enable 2
29	ABE1#	O	EMIF byte enable 1	30	ABE0#	O	EMIF byte enable 0
31	GND	Vss	System ground	32	GND	Vss	System ground
33	AED31	I/O	EMIF data pin 31	34	AED30	I/O	EMIF data pin 30
35	AED29	I/O	EMIF data pin 29	36	AED28	I/O	EMIF data pin 28
37	AED27	I/O	EMIF data pin 27	38	AED26	I/O	EMIF data pin 26
39	AED25	I/O	EMIF data pin 25	40	AED24	I/O	EMIF data pin 24
41	3.3V	Vcc	3.3V voltage supply pin	42	3.3V	Vcc	3.3V voltage supply pin
43	AED23	I/O	EMIF data pin 23	44	AED22	I/O	EMIF data pin 22
45	AED21	I/O	EMIF data pin 21	46	AED20	I/O	EMIF data pin 20
47	AED19	I/O	EMIF data pin 19	48	AED18	I/O	EMIF data pin 18
49	AED17	I/O	EMIF data pin 17	50	AED16	I/O	EMIF data pin 16
51	GND	Vss	System ground	52	GND	Vss	System ground
53	AED15	I/O	EMIF data pin 15	54	AED14	I/O	EMIF data pin 14
55	AED13	I/O	EMIF data pin 13	56	AED12	I/O	EMIF data pin 12
57	AED11	I/O	EMIF data pin 11	58	AED10	I/O	EMIF data pin 10
59	AED9	I/O	EMIF data pin 9	60	AED8	I/O	EMIF data pin 8
61	GND	Vss	System ground	62	GND	Vss	System ground
63	AED7	I/O	EMIF data pin 7	64	AED6	I/O	EMIF data pin 6
65	AED5	I/O	EMIF data pin 5	66	AED4	I/O	EMIF data pin 4
67	AED3	I/O	EMIF data pin 3	68	AED2	I/O	EMIF data pin 2
69	AED1	I/O	EMIF data pin 1	70	AED0	I/O	EMIF data pin 0
71	GND	Vss	System ground	72	GND	Vss	System ground
73	AARE#	O	EMIF async read enable	74	AAWE#	O	EMIF async write enable
75	AAOE#	O	EMIF async output enable	76	AARDY	I	EMIF asynchronous ready
77	ACE3#	O	Chip enable 3	78	ACE2#	O	Chip enable 2
79	GND	Vss	System ground	80	GND	Vss	System ground

4.3.2 J3, Peripheral Expansion Connector

Table 3: J3, Peripheral Expansion Connector

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	12V	Vcc	12V voltage supply pin	2	-12V	Vcc	-12V voltage supply pin
3	GND	Vss	System ground	4	GND	Vss	System ground
5	5V	Vcc	5V voltage supply pin	6	5V	Vcc	5V voltage supply pin
7	GND	Vss	System ground	8	GND	Vss	System ground
9	5V	Vcc	5V voltage supply pin	10	5V	Vcc	5V voltage supply pin
11	N/C	-	No connect	12	N/C	-	No connect
13	N/C	-	No connect	14	N/C	-	No connect
15	N/C	-	No connect	16	N/C	-	No connect
17	N/C	-	No connect	18	N/C	-	No connect
19	3.3V	Vcc	3.3V voltage supply pin	20	3.3V	Vcc	3.3V voltage supply pin
21	CLKX0	I/O	McBSP0 transmit clock	22	CLKS0	I	McBSP0 clock source
23	FSX0	I/O	McBSP0 transmit frame sync	24	DX0	O	McBSP0 transmit data
25	GND	Vss	System ground	26	GND	Vss	System ground
27	CLKR0	I/O	McBSP0 receive clock	28	N/C	-	No connect
29	FSR0	I/O	McBSP0 receive frame sync	30	DR0	I	McBSP0 receive data
31	GND	Vss	System ground	32	GND	Vss	System ground
33	CLKX2	I/O	McBSP2 transmit clock	34	CLKS2	I	McBSP2 clock source
35	FSX2	I/O	McBSP2 transmit frame sync	36	DX2	O	McBSP2 transmit data
37	GND	Vss	System ground	38	GND	Vss	System ground
39	CLKR2	I/O	McBSP2 receive clock	40	N/C	-	No connect
41	FSR2	I/O	McBSP2 receive frame sync	42	DR2	I	McBSP2 receive data
43	GND	Vss	System ground	44	GND	Vss	System ground
45	TOUT0	O	Timer 0 output	46	TINP0	I	Timer 0 input
47	N/C	-	No connect	48	EXT_INT5	I	External interrupt 5
49	TOUT1	O	Timer 1 output	50	TINP1	I	Timer 1 input
51	GND	Vss	System ground	52	GND	Vss	System ground
53	EXT_INT4	I	External interrupt 4	54	N/C	-	No connect
55	N/C	-	No connect	56	N/C	-	No connect
57	N/C	-	No connect	58	N/C	-	No connect
59	RESET	O	System reset	60	N/C	-	No connect
61	GND	Vss	System ground	62	GND	Vss	System ground
63	CNTL1	O	Daughtercard control 1	64	CNTL0	O	Daughtercard control
65	STAT1	I	Daughtercard status 1	66	STAT0	I	Daughtercard status
67	EXT_INT6	I	External interrupt 6	68	EXT_INT7	I	External interrupt 7
69	ACE3#	O	Chip enable 3	70	N/C	-	No connect
71	N/C	-	No connect	72	N/C	-	No connect
73	N/C	-	No connect	74	N/C	-	No connect
75	DC_DET#	Vss	System ground	76	GND	Vss	System ground
77	GND	Vss	System ground	78	ECL KOUT	O	EMIF Clock
79	GND	Vss	System ground	80	GND	Vss	System ground

4.3.3 J1, PCI Expansion Connector

Table 4: J1, PCI Expansion Connector

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	PCI_EN	I	PCI enable	2	Resv	N/C	Resv
3	GND	Vss	System ground	4	HPI_RS#	I	HPI reset
5	Resv	N/C	Resv	6	Resv	N/C	Resv
7	GND	Vss	System ground	8	GND	Vss	System ground
9	AD1	I/O	PCI address/data 1	10	GP[2]	I/O	General purpose I/O
11	AD3	I/O	PCI address/data 3	12	AD0	I/O	PCI address/data 0
13	AD5	I/O	PCI address/data 5	14	AD2	I/O	PCI address/data 2
15	AD7	I/O	PCI address/data 7	16	AD4	I/O	PCI address/data 4
17	GND		System ground	18	AD6	I/O	PCI address/data 6
19	AD8	I/O	PCI address/data 8	20	GND	Vss	System ground
21	AD10	I/O	PCI address/data 10	22	AD9	I/O	PCI address/data 9
23	AD12	I/O	PCI address/data 12	24	AD11	I/O	PCI address/data 11
25	AD14	I/O	PCI address/data 14	26	AD13	I/O	PCI address/data 13
27	GND	Vss	System ground	28	AD15	I/O	PCI address/data 15
29	PCBE1#	I/O	PCI command/byte ena 1	30	GND	Vss	System ground
31	GND	Vss	System ground	32	PPAR	I/O	PCI parity
33	PSERR#	I/O	PCI system error	34	GND	Vss	System ground
35	GND	Vss	System ground	36	PSTOP#	I/O	PCI stop
37	PPERR#	I/O	PCI parity error	38	GND	Vss	System ground
39	GND	Vss	System ground	40	Resv		None
41	PDEVSEL#	I/O	PCI device select	42	GND	Vss	System ground
43	GND	Vss	System ground	44	PFRAME#	I/O	PCI Frame
45	PIRDY#	I/O	PCI initiator ready	46	GND	Vss	System ground
47	GND	Vss	System ground	48	AD16	I/O	PCI address/data 16
49	PCBE2#	I/O	PCI command/byte ena 2	50	AD18	I/O	PCI address/data 18
51	AD17	I/O	PCI address/data 17	52	AD20	I/O	PCI address/data 20
53	AD19	I/O	PCI address/data 19	54	AD22	I/O	PCI address/data 22
55	AD21	I/O	PCI address/data 21	56	GND	Vss	System ground
57	AD23	I/O	PCI address/data 23	58	Resv		None
59	Resv		None	60	AD24	I/O	PCI address/data 24
61	GND	Vss	System ground	62	AD26	I/O	PCI address/data 26
63	AD25	I/O	PCI address/data 25	64	AD28	I/O	PCI address/data 28
65	AD27	I/O	PCI address/data 27	66	AD30	I/O	PCI address/data 30
67	AD29	I/O	PCI address/data 29	68	GP[12]	I/O	General purpose I/O
69	AD31	I/O	PCI address/data 31	70	GND	Vss	System ground
71	GND	Vss	System ground	72	GP[13]	I/O	General purpose I/O
73	GP[15]	I/O	General purpose I/O	74	GND	Vss	System ground
75	GND	Vss	System ground	76	GP[14]	I/O	General purpose I/O
77	PCLK	I	PCI Clock	78	GND	Vss	System ground
79	GND	Vss	System ground	80	N/C	-	No connect

4.3.4 J1, Used As HPI Expansion Connector

Table 5: J1, Used as HPI Expansion Connector

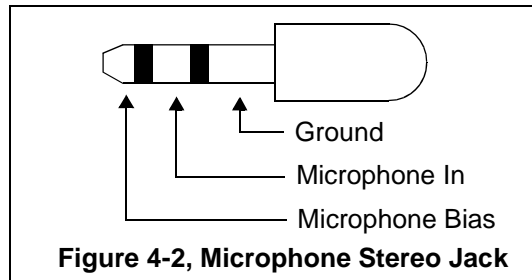
Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	PCI_EN	I	PCI enable	2	Resv	N/C	Resv
3	GND	Vss	System ground	4	HPI_RS#	I	HPI reset
5	Resv	N/C	Resv	6	Resv	N/C	Resv
7	GND	Vss	System ground	8	GND	Vss	System ground
9	HD1	I/O	Host data 1	10	PCBE0#	I/O	PCI command/byte ena 0
11	HD3	I/O	Host data 3	12	HD0	I/O	Host data 0
13	HD5	I/O	Host data 5	14	HD2	I/O	Host data 2
15	HD7	I/O	Host data 7	16	HD4	I/O	Host data 4
17	GND		System ground	18	HD6	I/O	Host data 6
19	HD8	I/O	Host data 8	20	GND	Vss	System ground
21	HD10	I/O	Host data 10	22	HD9	I/O	Host data 9
23	HD12	I/O	Host data 12	24	HD11	I/O	Host data 11
25	HD14	I/O	Host data 14	26	HD13	I/O	Host data 13
27	GND	Vss	System ground	28	HD15	I/O	Host data 15
29	HDS2#	I/O	Host data strobe 2	30	GND	Vss	System ground
31	GND	Vss	System ground	32	HAS#	I/O	Host address strobe
33	HDS1#	I/O	Host data strobe 1	34	GND	Vss	System ground
35	GND	Vss	System ground	36	HCNTL0	I/O	Host Control 0
37	HCS#	I/O	Host chip select	38	GND	Vss	System ground
39	GND	Vss	System ground	40	PTRDY#	I/O	PCI target ready
41	HCNTL1	I/O	Host Control 1	42	GND	Vss	System ground
43	GND	Vss	System ground	44	HINT#	I/O	Host Interrupt
45	HRDY#	I/O	Host ready	46	GND	Vss	System ground
47	GND	Vss	System ground	48	HD16	I/O	Host data 16
49	HR/W#	I/O	Host Read/Write	50	HD18	I/O	Host data 18
51	HD17	I/O	Host data 17	52	HD20	I/O	Host data 20
53	HD19	I/O	Host data 19	54	HD22	I/O	Host data 22
55	HD21	I/O	Host data 21	56	GND	Vss	System ground
57	HD23	I/O	Host data 23	58	Resv		Resv
59	Resv		Resv	60	HD24	I/O	Host data 24
61	GND	Vss	System ground	62	HD26	I/O	Host data 26
63	HD25	I/O	Host data 25	64	HD28	I/O	Host data 28
65	HD27	I/O	Host data 27	66	HD30	I/O	Host data 30
67	HD29	I/O	Host data 29	68	PGNT#	I	PCI bus grant
69	HD31	I/O	Host data 31	70	GND	Vss	System ground
71	GND	Vss	System ground	72	Resv		Resv
73	Resv		Resv	74	GND	Vss	System ground
75	GND	Vss	System ground	76	Resv		Resv
77	Resv		Resv	78	GND	Vss	System ground
79	GND	Vss	System ground	80	N/C	-	No connect

4.4 Audio Connectors

The C6455 DSK has 4 audio connectors. They are described in the following sections.

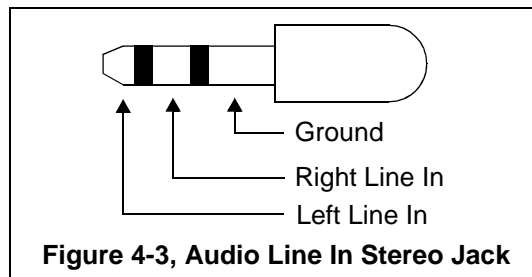
4.4.1 J1301, Microphone Connector

The input is a 3.5 mm. stereo jack. Both inputs are connected to the microphone so it is monaural. The signals on the plug are shown in the figure below.



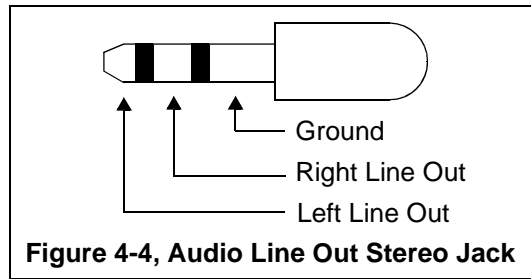
4.4.2 J1303, Audio Line In Connector

The audio line in is a stereo input. The input connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.



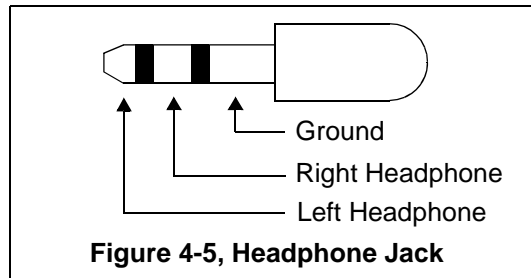
4.4.3 J1304, Audio Line Out Connector

The audio line out is a stereo output. The output connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.



4.4.4 J1302, Headphone Connector

Connector J1302 is a headphone/speaker jack. It can drive standard headphones or a high impedance speaker directly. The standard 3.5 mm jack is shown in the figure below.

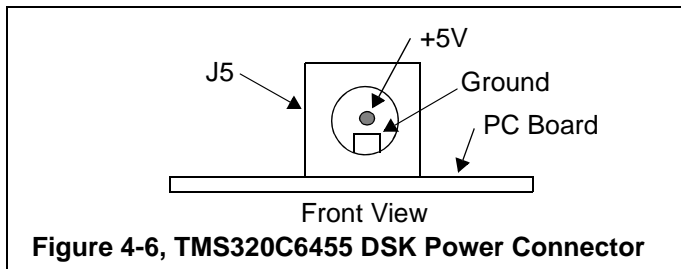


4.5 Power Connectors

The C6455 DSK has 2 power connectors. They are described in the following sections.

4.5.1 J5, +5 Volt Connector

Power (+5 volts) is brought onto the TMS320C6455 DSK via connector J5. The connector has an outside diameter of 5.5 mm. and an inside diameter of 2.5 mm. The A diagram of J5 is shown below.



4.5.2 J6, Optional Power Connector

Connector J6 is an optional power connector. It will operate with the standard personal computer power supply. To populate this connector use a Molex #15109-0410 or Tyco #174552-1. The table below shows the voltages on the respective pins.

Table 6: J6, Optional Power Connector

Pin #	Voltage Level
1	+12 Volts
2	-12 Volts
3	Ground
4	+5 Volts

WARNING !
Do not plug into J5 and J6 at the same time.

4.6 Miscellaneous Connectors

The C6455 DSK has 6 additional connectors to aid the user in developing with this product. They are described in the following sections.

4.6.1 J1201, USB Connector

Connector J1201 provides a Universal Serial Bus (USB) Interface to the embedded JTAG emulation logic on the DSK. This allows for code development and debug without the use of an external emulator. The signals on this connector are shown in the below.

Table 7: J1201, USB Connector

Pin #	USB Signal Name
1	USBVdd
2	D+
3	D-
4	USB Vss
5	Shield
6	Shield

4.6.2 J8, 14 Pin External JTAG Connector

The TMS320C6455 DSK is supplied with a 14 pin header interface, J8. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown figure 4-6 below.

TMS	1	2	TRST-	Header Dimensions Pin-to-Pin spacing, 0.100 in. (X,Y) Pin width, 0.025-in. square post Pin length, 0.235-in. nominal
TDI	3	4	GND	
PD (+3.3V)	5	6	no pin (key)	
TDO	7	8	GND	
TCK-RET	9	10	GND	
TCK	11	12	GND	
EMU0	13	14	EMU1	

Figure 4-7, JTAG INTERFACE

The signal names for each pin are shown in the table below.

Table 8: J8, JTAG Interface

Pin #	Signal Name
1	TMS
2	TRST-
3	TDI
4	GND
5	PD
6	no pin
7	TDO
8	GND
9	TCK-RET
10	GND
11	TCK
12	GND
13	EMU0
14	EMU1

4.6.3 J7, 60 Pin Advanced Emulation Connector

The 60 pin emulation connector is mounted on the side of the board near the 14 pin JTAG connector. This connector is for advanced emulation capability. The signals on this connector are 4 columns by 15 rows as shown in the table below

Table 9: J7, 60 Pin Emulation Connector

Row #	Column A Signal Name	Column B Signal Name	Column C Signal Name	Column D Signal Name
1	Ground	IDO	ID2	Ground
2	Ground	TMS	EMU18	Ground
3	Ground	EMU17	TRSTn	Ground
4	Ground	TDI	EMU16	Ground
5	Ground	EMU14	EMU15	Ground
6	Ground	EMU12	EMU13	Ground
7	Ground	TDO	EMU11	Ground
8	TYPE0	TVD	TCLKRTN	TYPE1
9	Ground	EMU9	EMU10	Ground
10	Ground	EMU7	EMU8	Ground
11	Ground	EMU5	EMU6	Ground
12	Ground	TCLK	EMU4	Ground
13	Ground	EMU2	EMU3	Ground
14	Ground	EMU0	EMU1	Ground
15	Ground	ID1	ID3	Ground

4.6.4 JP3, PLD Programming Connector

This connector interfaces to the Altera CPLD, U12. It is used in the in the factory for the programming of the CPLD. This connector is not intended to be used outside the factory.

4.6.5 J9, AMCC Connector

This connector provides a high speed Serial Rapid I/O to other platforms. This connector has 170 pins. Pin 1 is across from pin 170, and pin 85 is across from pin 86. This connector is populated on DSK platform when the board is incorporated into the EVM product. The two tables below shoe the signals on each pin.

Table 10: J9, AMCC Connector, Pins 1-42, 170-129

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	GND			170	GND		
2	+12V			169	DSPB.TDI	I	JTAG TDI
3	PRESENT			168	DSPB.TDO	O	JTAG TDO
4	+3.3V			167	DSPB.TRSTn	O	JTAG TRSTn
5	GND			166	DSPB.TMS	O	JTAG TMS
6				165	DSPB.TCK	O	JTAG Clock
7	GND			164	GND		
8				163			
9	+12V			162			
10	GND			161	GND		
11				160			
12				159			
13	GND			158	GND		
14				157			
15				156			
16	GND			155	GND		
17				154			
18	+12V			153			
19	GND			152	GND		
20				151			
21				150			
22	GND			149	GND		
23				148			
24				147			
25	GND			146	GND		
26				145			
27	+12V			144			
28	GND			143	GND		
29				142			
30				141			
31	GND			140	GND		
32				139			
33				138			
34	GND			137	GND		
35				136			
36				135			
37	GND			134	GND		
38				133			
39				132			
40	GND			131	GND		
41	ENABLE			130			
42	+12V			129			

Table 11: J9, AMCC Connector, Pins 43-128-86

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
43	GND			128	GND		
44	DSPA.RIORXP0	I	SRIO Channel 0 RCV+	127			
45	DSPA.RIORXN0	I	SRIO Channel 0 RCV-	126			
46	GND			125	GND		
47	DSPA.RIOTXP0	O	SRIO Channel 0 TXMT+	124			
48	DSPA.RIOTXN0	O	SRIO Channel 0 TXMT-	123			
49	GND			122	GND		
50	DSPA.RIORXP1	I	SRIO Channel 1 RCV+	121			
51	DSPA.RIORXN1	I	SRIO Channel 1 RCV-	120			
52	GND			119	GND		
53	DSPA.RIOTXP1	O	SRIO Channel 1 TXMT+	118			
54	DSPA.RIOTXN1	O	SRIO Channel10 TXMT-	117			
55	GND			116	GND		
56	I2C_SCL	O	I ² C clock	115			
57	+12V			114			
58	GND			113	GND		
59	DSPA.RIORXP2	I	SRIO Channel 2 RCV+	112			
60	DSPA.RIORXN2	I	SRIO Channel 2 RCV-	111			
61	GND			110	GND		
62	DSPA.RIOTXP2	O	SRIO Channel 2 TXMT+	109			
63	DSPA.RIOTXN2	O	SRIO Channel 2 TXMT-	108			
64	GND			107	GND		
65	DSPA.RIORXP3	I	SRIO Channel 3 RCV+	106			
66	DSPA.RIORXN3	I	SRIO Channel 3 RCV-	105			
67	GND			104	GND		
68	DSPA.RIOTXP3	O	SRIO Channel 3 TXMT+	103			
69	DSPA.RIOTXN3	O	SRIO Channel 3 TXMT-	102			
70	GND			101	GND		
71	I2C_SDA	I/O	I ² C Data	100			
72	+12V			99			
73	GND			98	GND		
74				97			
75				96			
76	GND			95	GND		
77				94			
78				93			
79	GND			92	GND		
80				91			
81				90			
82	GND			89	GND		
83	GND			88			
84	+12V			87			
85	GND			86	GND		

4.6.6 P1102, Ethernet Connector

Connector P1102 is a standard RJ-45 ethernet connector. The connector pin out is shown below.

Table 12: P1102, Ethernet Connector

Pin #	USB Signal Name
1	TXD+
2	TXD-
3	RXD+D-
4	TXD-CT
5	Not Used
6	RXD-
7	NC
8	Ground

4.7 System LEDs

The TMS320C6455 DSK has four system light emitting diodes (LEDs). These LEDs indicate various conditions on the DSK. These function of each LED is shown in the table below.

Table 13: System LEDs

Reference Designator	Color	Function	On Signal State
D4	Green	USB Emulation in use. When External JTAG Emulator is used this LED is off.	1
D3	Green	+5 Volt present	1
D6	Orange	RESET Active	1
DS201	Green	USB Active, Blinks during USB data transfer	1
DS1101	Yellow	Ethernet	0
DS1102	green	Ethernet	0

4.8 SW2, Reset Switch

There are three resets on the TMS320C6455 DSK. The first reset is the power on reset. This circuit waits until power is within the specified range before releasing the power on reset pin to the TMS320C6455.

External sources which control the reset are push button SW2, and the on board embedded USB JTAG emulator.

Chapter 5

Introduction to the TMS320C6455 EVM Mezzanine Board

Chapter five provides a description of the TMS320C6455 EVM Mezzanine Board along with the key features and a block diagram of the circuit board.

Topic	Page
5.1 Key Features	5-2
5.2 Functional Overview	5-3
5.3 Basic Operation	5-3
5.4 Memory Map	5-4
5.5 Configuration Switch Settings	5-5
5.6 Bootmode Configurations	5-6

5.1 Key Features

The C6455 Mezzanine Board is a high performance development platform that enables users to evaluate and develop applications for the TI C64xx DSP family. The Mezzanine Board along with the mating C6455 DSK board serve as a hardware reference design for TMS320C6455 DSPs connected via Serial Rapid I/O (SRIO). Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.

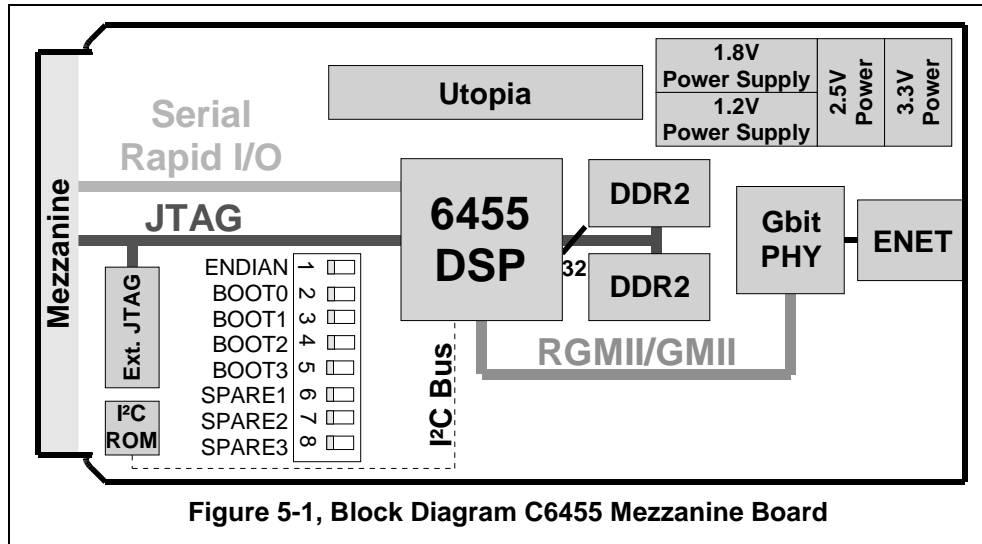


Figure 5-1, Block Diagram C6455 Mezzanine Board

The Mezzanine Board comes with a full compliment of on-board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments TMS320C6455 DSP operating at 1 Gigahertz.
- 128 Mbytes of DDR2 memory
- 100/1000 MBPs ethernet interface
- I²C Serial ROM
- Configured boot options and clock input selection
- AMCC SRIO connector
- Optional Utopia interface
- JTAG emulation through on-board JTAG emulator with USB host interface or external emulator
- Single voltage power supply (+12V)

5.2 Functional Overview of the TMS320C6455 Mezzanine Board

The DSP on the C6455 Mezzanine Board interfaces to on-board peripherals dedicated I/O pins or SRIO interface connector. The DDR2 memory is on its own dedicated EMIF.

The DSK has a 100/1000 mbit Phy which is connected to the DSP's on board EMAC.

The board is powered by +12 volts delivered via the SRIO connector. On-board switching voltage regulators provide the 1.2V DSP core voltage, 1.5V for RGMII, 1.8V for DDR, and 3.3V I/O supplies. The board is held in reset until these supplies are within operating specifications.

Code Composer communicates with the Mezzanine Board via the SRIO connector to the embedded JTAG emulator on the DSK with a USB host interface. The Mezzanine board can also be used with an external emulator through the external 60 pin connector.

5.3 Basic Operation

The Mezzanine board is designed to work in conjunction with a DSK base platform and with TI's DSK specific Code Composer Studio development environment that ships with the board. Code Composer communicates with the board through the on-board JTAG emulator. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

After the install is complete, follow these steps to run Code Composer. The DSK and Mezzanine board must be fully connected to launch the DSK/EVM version of Code Composer.

- 1) Connect the included power supply to the EVM.
- 2) Connect the EVM to your PC with a standard USB cable (also included).
- 3) Launch Code Composer from its icon on your desktop.

Detailed information about the EVM including a tutorial, examples and reference material is available in the help file.

5.4 Memory Map

The C64xx family of DSPs has a large byte addressable address space. Program code and data can be placed anywhere in the unified address space. Addresses are always 32-bits wide.

The memory map shows the address space of a generic 6455 processor on the left with specific details of how each region is used on the right. By default, the internal memory sits at the beginning of the address space. Portions of memory can be remapped in software as L2 cache rather than fixed RAM.

EMIFA (External Memory Interface A) has 4 separate addressable regions called chip enable spaces (CE2-CE5). On the Mezzanine board this region is disabled via Boot Load resistors. The DDR2 occupies CE0 of DDR2 Memory bus.

Address	Generic 6455 Address Space	6455 DSK
0x00000000	Internal Memory	Internal Memory
0x00100000	Reserved Space or Peripheral Regs	Reserved or Peripheral
0xA0000000	EMIFA CE2	Disabled
0xB0000000	EMIFA CE3	Disabled
0xC0000000	EMIFA CE4	Disabled
0xD0000000	EMIFA CE5	
0xE0000000	DDR2 CE0	DDR2 Memory

Figure 5-2, Memory Map, C6455 Mezzanine Board

5.5 Configuration Switch Settings

The Mezzanine board has 8 configuration (SW3,1-8) switches that allows users to control the operational state of the DSP when it is released from reset. The configuration switch block is labeled SW3 on the DSK board, next to the reset switch.

Configuration switch 1 controls the endianness of the DSP. The factory default is little endian. The settings of switch 1 are shown in the table below.

Table 1: Endian Configuration Switch Settings

SW3-1	Configuration Description
Off	Little endian *
On	Big endian

* Default

Switches 2-5 configure the boot mode that will be used when the DSP starts executing. These boot modes are shown in the table below. The default boot mode is EMIFA 8 bit ROM Boot.

Table 2: Boot Load Configuration Switch Settings

SW3-5 AE19	SW3-4 * AE18	SW3-3 AE17	SW3-2 AE16	Configuration Description
Off	Off	Off	Off	No Boot
Off	Off	Off	On	Host Boot HPI
Off	Off	On	Off	Reserved
Off	Off	On	On	Reserved
Off	On	Off	Off	EMIFA 8 bit ROM Boot
Off	On	Off	On	I ² C Boot Master
Off	On	On	Off	I ² C slave
Off	On	On	On	Host Boot PCI
On	x	x	x	Serial Rapid I/O Boot see DSP data sheet for more details

On revision “C” and newer boards the switch positions 6-8 are spare switches. The CLKIN frequency is now set to a fixed 50 Mhz. oscillator.

5.6 Bootmode Configurations

The C6455 uses the address lines to configure the device configuration at RESET. Although many of these configurations can be changed in software via internal DSP configuration registers, the defaults for the DSK are shown in the table below.

Table 3: Bootmode Configurations

Config Pin Name	Function	Controlled By
AE19	Boot Mode 3	SW3-5
AE18	Boot Mode 2	SW3-4
AE17	Boot Mode 1	SW3-3
AE16	Boot Mode 0	SW3-2
AE15	AECLKIN Selected	Resistor Strap
AE14	HPI 16 bit Mode Selected	Resistor Strap
AE13	Endian Mode	SW3-1
AE12	Ethernet MAC Enabled	Resistor Strap
AE11	Reserved	Resistor Strap
AE10	EMAC RGMII Mode	Resistor Strap
AE9	EMAC RGMII Mode	Resistor Strap
AE8	PCI I ² C ROM Disabled	Resistor Strap
AE7	Reserved	Resistor Strap
AE6	PCI 33 Mhz.	Resistor Strap
AE5	McBSP1 Enabled	Resistor Strap
AE4	SYSCLK3 Enabled	Resistor Strap
AE3	Reserved	Resistor Strap
AE2	CFGGP2	Resistor Strap
AE1	CFGGP1	Resistor Strap
AE0	CFGGP0	Resistor Strap
ABA1	EMIFA Disabled	Resistor Strap
ABA0	DDR Enabled	Resistor Strap

Chapter 6

Physical Description

This chapter describes the physical layout of the TMS320C6455 Mezzanine Board and its connectors.

Topic	Page
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6.2.1 J1, Utopia Connector	6-3
6.2.2 J7, 60 Pin JTAG Connector	6-5
6.2.3 J9, AMCC Interface Connector	6-5
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6.1 Board Layout

The C6455 Mezzanine Board is a 7.107 x 2.893 inch (180.5 x 73.48 mm.) multi-layer board which is powered through connector J9. Figure 6-1 shows the layout of the C6455 Mezzanine Board.

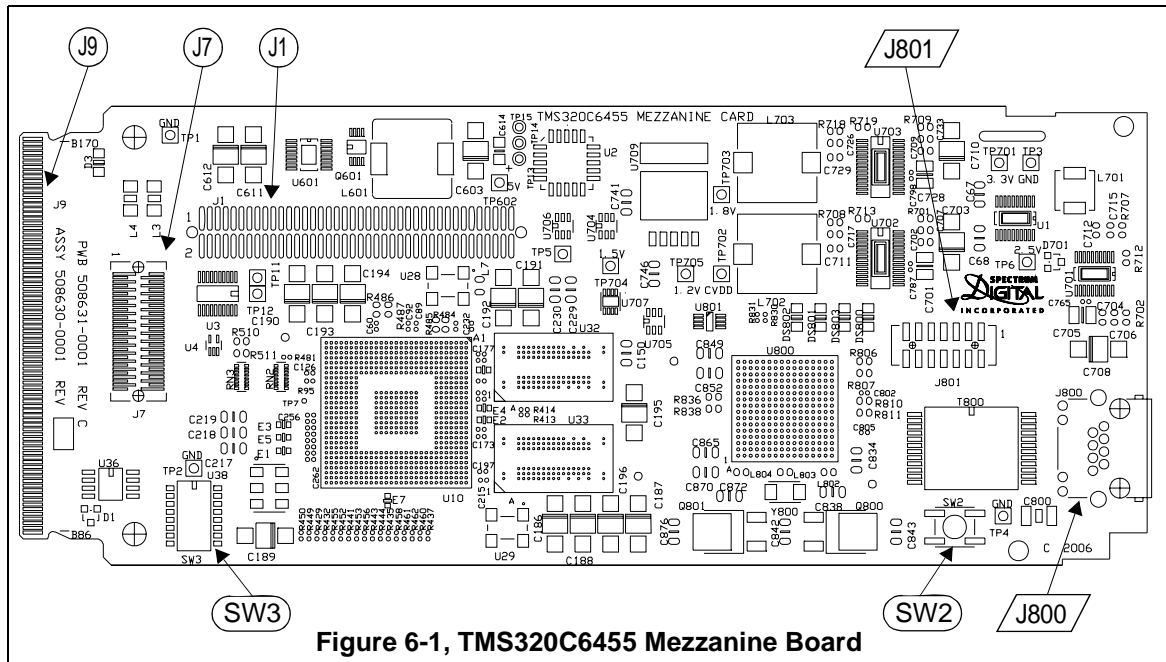


Figure 6-1, TMS320C6455 Mezzanine Board

6.2 Connector Index

The TMS320C6455 Mezzanine Board has several connectors which provide the user access to the various signals on the board.

Table 1: TMS320C6455 Mezzanine Board Connectors

Connector	# Pins	Function
J1	80	Utopia
J7	60	JTAG
J9	170	SRIO/AMCC Connector
J800	8	Ethernet
J801	14	Factory Use

6.2.1 J1, Utopia Connector

The TMS320C6455 Mezzanine supports one expansion connector for optional enable Utopia interface. The expansion connector pinouts for J1 are described below.

The this expansion connector is an 80 pin 0.050 x 0.050 inches low profile connectors from Samtec or AMP. The Samtec SFM Series (surface mount) connectors are designed for high speed interconnections because they have low propagation delay, capacitance, and cross talk. The recommended mating connector, whose part number is TFM-140-32-S-D-LC, is a surface mount connector that provides a 0.465" mated height.

Note: Utopia interface is not the strapped default.
EMAC is disabled when using the Utopia interface

Table 2: J1, Expansion Connector

Pin	Signal	Description	Pin	Signal	Description
1	GND		2		
3			4		
5			6		
7			8		
9			10		
11	GND		12	URADDR4	Receive Address 4
13	URADDR3	Receive Address 3	14	URADDR2	Receive Address 2
15	URADDR1	Receive Address 1	16	URADDR0	Receive Address 0
17			18		
19			20		
21			22		
23			24		
25	GND		26	URSOC	
27	URDATA7	Receive Data 7	28	URDATA6	Receive Data 6
29	URDATA5	Receive Data 5	30	URDATA4	Receive Data 4
31	URDATA3	Receive Data 3	32	URDATA2	Receive Data 2
33	URDATA1	Receive Data 1	34	URDATA0	Receive Data 0
35	URCLAV		36		
37	GND		38	URENB	Receive Enable
39	URCLK	Receive Clock	40		
41			42	UXCLK	Transmit Clock
43	UXENB	Transmit Enable	44	GND	
45			46	UXDATA1	Transmit Data 1
47	UXDATA0	Transmit Data 0	48	UXDATA3	Transmit Data 3
49	UXDATA2	Transmit Data 2	50	UXDATA5	Transmit Data 5
51	UXDATA4	Transmit Data 4	52	UXDATA7	Transmit Data 7
53	UXDATA6	Transmit Data 6	54		
55	UXSOC		56	GND	
57			58		
59			60		
61			62		
63			64		
65	UXADDR0	Transmit Address 0	66	UXADDR1	Transmit Address 1
67	UXADDR2	Transmit Address 2	68	UXADDR3	Transmit Address 3
69	UXADDR4	Transmit Address 4	70	GND	
71			72		
73			74		
75			76		
77			78		
79			80	GND	System ground

6.2.2 J7, 60 Pin JTAG Connector

The Mezzanine board can operate its JTAG interface with either the on board JTAG connector or via the AMCC interface connector when plugged into a DSK.

This connector is for advanced emulation capability. The signals on this connector are 4 columns by 15 rows as shown in the table below

Table 3: J7, 60 Pin Emulation Connector

Row #	Column A Signal Name	Column B Signal Name	Column C Signal Name	Column D Signal Name
1	Ground	IDO	ID2	Ground
2	Ground	TMS	EMU18	Ground
3	Ground	EMU17	TRSTn	Ground
4	Ground	TDI	EMU16	Ground
5	Ground	EMU14	EMU15	Ground
6	Ground	EMU12	EMU13	Ground
7	Ground	TDO	EMU11	Ground
8	TYPE0	TVD	TCLKRTN	TYPE1
9	Ground	EMU9	EMU10	Ground
10	Ground	EMU7	EMU8	Ground
11	Ground	EMU5	EMU6	Ground
12	Ground	TCLK	EMU4	Ground
13	Ground	EMU2	EMU3	Ground
14	Ground	EMU0	EMU1	Ground
15	Ground	ID1	ID3	Ground

6.2.3 J9, AMCC Interface Connector

The J9 card edge connector plugs into the J9 connector on the DSK circuit board. This connector provides a high speed Serial Rapid I/O to the DSK board. This connector has 170 pins. Pin 1 is across from pin 170, and pin 85 is across from pin 86. The signals on this connector are shown in the tables below.

Table 4: J9, AMCC Connector, Pins 1-42, 170-129

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	GND			170	GND		
2	+12V			169	DSPB.TDI		JTAG TDI
3	PRESENT			168	DSPB.TDO		JTAG TDO
4	+3.3V			167	DSPB.TRSTn		JTAG TRSTn
5	GND			166	DSPB.TMS		JTAG TMS
6				165	DSPB.TCK		JTAG CLK
7	GND			164	GND		
8				163			
9	+12V			162			
10	GND			161	GND		
11				160			
12				159			
13	GND			158	GND		
14				157			
15				156			
16	GND			155	GND		
17				154			
18	+12V			153			
19	GND			152	GND		
20				151			
21				150			
22	GND			149	GND		
23				148			
24				147			
25	GND			146	GND		
26				145			
27	+12V			144			
28	GND			143	GND		
29				142			
30				141			
31	GND			140	GND		
32				139			
33				138			
34	GND			137	GND		
35				136			
36				135			
37	GND			134	GND		
38				133			
39				132			
40	GND			131	GND		
41	ENABLE			130			
42	+12V			129			

Table 5: J9, AMCC Connector, Pins 43-128-86

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
43	GND			128	GND		
44	DSPB.RIOTXP0		SRIO Channel 0 TXMT+	127			
45	DSPB.RIOTXN0		SRIO Channel 0 TXMT-	126			
46	GND			125	GND		
47	DSPB.RIORXP0		SRIO Channel 0 RCV+	124			
48	DSPB.RIORXN0		SRIO Channel 0 RCV-	123			
49	GND			122	GND		
50	DSPB.RIOTXP1		SRIO Channel 1 TXMT+	121			
51	DSPB.RIOTXN1		SRIO Channel 1 TXMT-	120			
52	GND			119	GND		
53	DSPB.RIORXP1		SRIO Channel 1 RCV+	118			
54	DSPB.RIORXN1		SRIO Channel 1 RCV-	117			
55	GND			116	GND		
56	I2C_SCL	I	I ² C Clock	115			
57	+12V			114			
58	GND			113	GND		
59	DSPB.RIOTXP2		SRIO Channel 2 TXMT+	112			
60	DSPB.RIOTXN2		SRIO Channel 2 TXMT-	111			
61	GND			110	GND		
62	DSPB.RIOTXP2		SRIO Channel 2 RCV+	109			
63	DSPB.RIORXN2		SRIO Channel 2 RCV-	108			
64	GND			107	GND		
65	DSPB.RIOTXP3		SRIO Channel 3 TXMT+	106			
66	DSPB.RIOTXN3		SRIO Channel 3 TXMT-	105			
67	GND			104	GND		
68	DSPB.RIORXP3		SRIO Channel 3 RCV+	103			
69	DSPB.RIORXN3		SRIO Channel 3 RCV-	102			
70	GND			101	GND		
71	I2C_SDA	I/O	I ² C Data	100			
72	+12V			99			
73	GND			98	GND		
74				97			
75				96			
76	GND			95	GND		
77				94			
78				93			
79	GND			92	GND		
80				91			
81				90			
82	GND			89	GND		
83	GND			88			
84	+12V			87			
85	GND			86	GND		

6.2.4 J800, Ethernet Connector

Connector J800 is a standard Gigabit RJ-45 ethernet connector. The connector pin out is shown in the table below.

Table 6: J800, Ethernet Connector Pin Out

Pin #	Signal Name
1	LXT TXD
2	LXT TXM
3	LXT RXP
4	Terminator 1
5	Terminator 2
6	LXT RXM
7	Terminator 3
8	Terminator 4

6.3 Switches

The TMS320C6455 Mezzanine Board has two switches, SW2 and SW3. Their positions on the board are indicated in Figure 6-1. Switch SW1 is a push-button RESET witch that resets the processor on the Mezzanine board. SW3 has positions which determine how the board will operate when it comes out of reset. These options are described in section 5.5 of this document.

Table 7: Mezzanine Board Switches

Switch	Function
SW2	Reset
SW3	Board configuration

6.4 Test Points

The TMS320C6455 Mezzanine Board has 14 test points. The position of each test point is shown below.

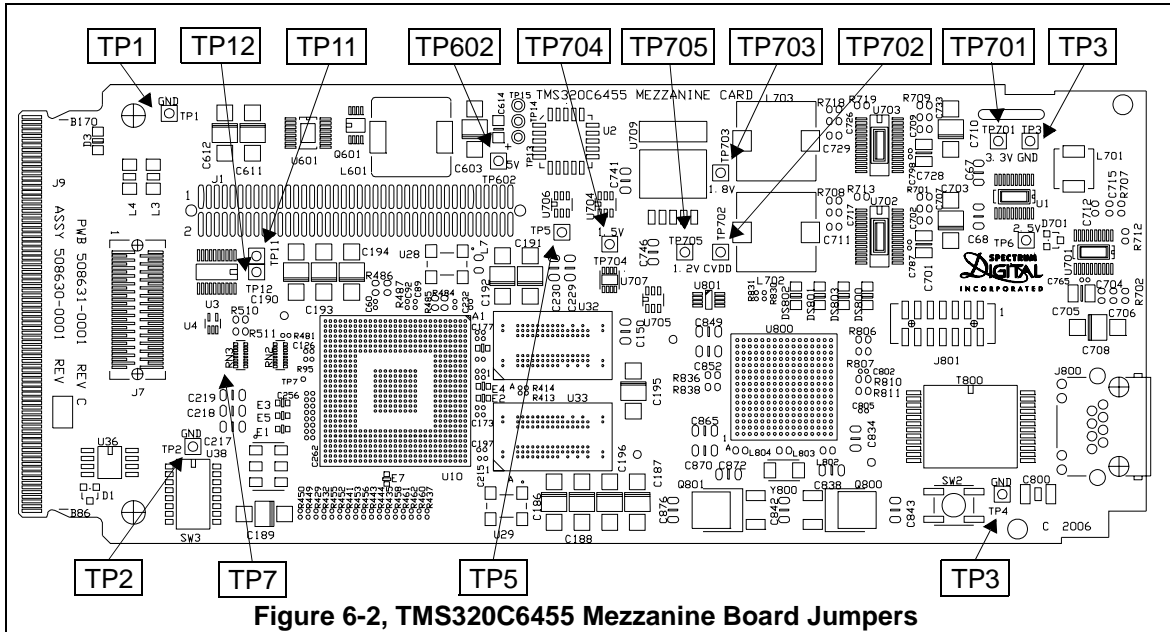


Figure 6-2, TMS320C6455 Mezzanine Board Jumpers

Table 8: TMS320C6455 Mezzanine Board Test Points

Test Point	Signal
TP1	GND
TP2	GND
TP3	GND
TP4	GND
TP5	
TP7	
TP11	
TP12	
TP602	+5 V
TP701	+3.3 V
TP702	CVDD
TP703	+1.8 V
TP704	+1.5 V
TP705	+1.2 V

Appendix A

Schematics

This appendix contains the schematics for the TMS320C6455 DSK.

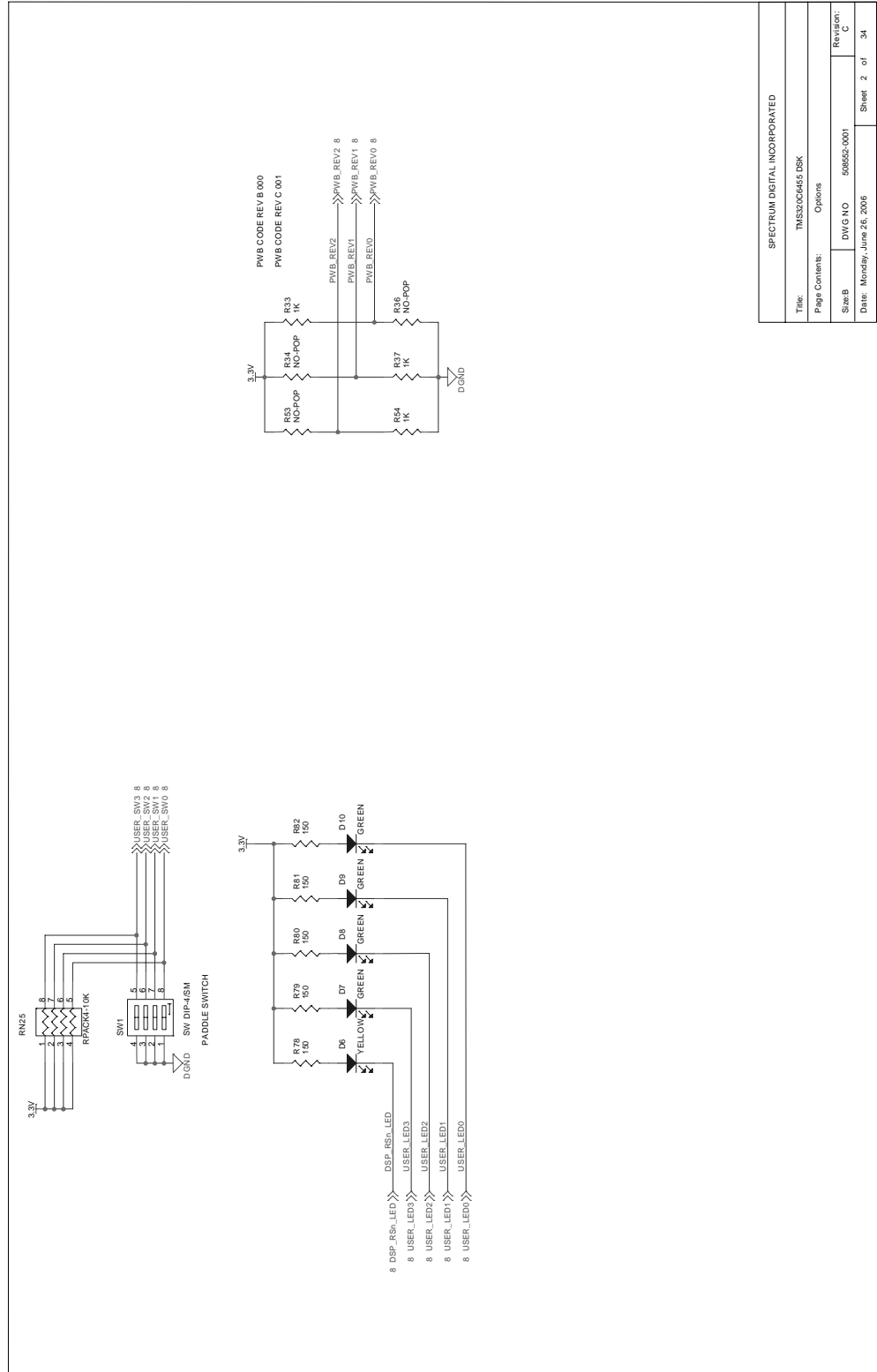
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- 1 COVER SHEET
- 2 USER OPTIONS
- 3 Clock Inputs
- 4 645X DDR2 Interface
- 5 DDR2 Memories
- 6 645X EMIF A
- 7 BOOT Options
- 8 CPLD
- 9 FLASH MEMORY
- 10 645X MII INTERFACE
- 11 MCBSP INTERFACE
- 12 645X HOST PORT INTERFACE
- 13 645X SPIO INTERFACE
- 14 DSK DAUGHTERCARD BUFFERS
- 15 DSK DAUGHTERCARD INTERFACE
- 16 645X POWER PINS I
- 17 645X POWER PINS II
- 18 645X EMULATION
- 19 645X EMULATION INTERFACE
- 20 EMULATION INTERFACE
- 21 HIERARCHICAL BLOCKS
- 22 645X RGMII INTERFACE
- 23 645X DECOUPLING CAPS I
- 24 645X DECOUPLING CAPS II
- 25 POWER INPUT
- 26 POWER OUTPUT
- 27 ETHERNET PHY
- 28 DSK POWER SUPPLIES I
- 29 DSK POWER SUPPLIES II
- 30-34 Embedded Emulation Not Included

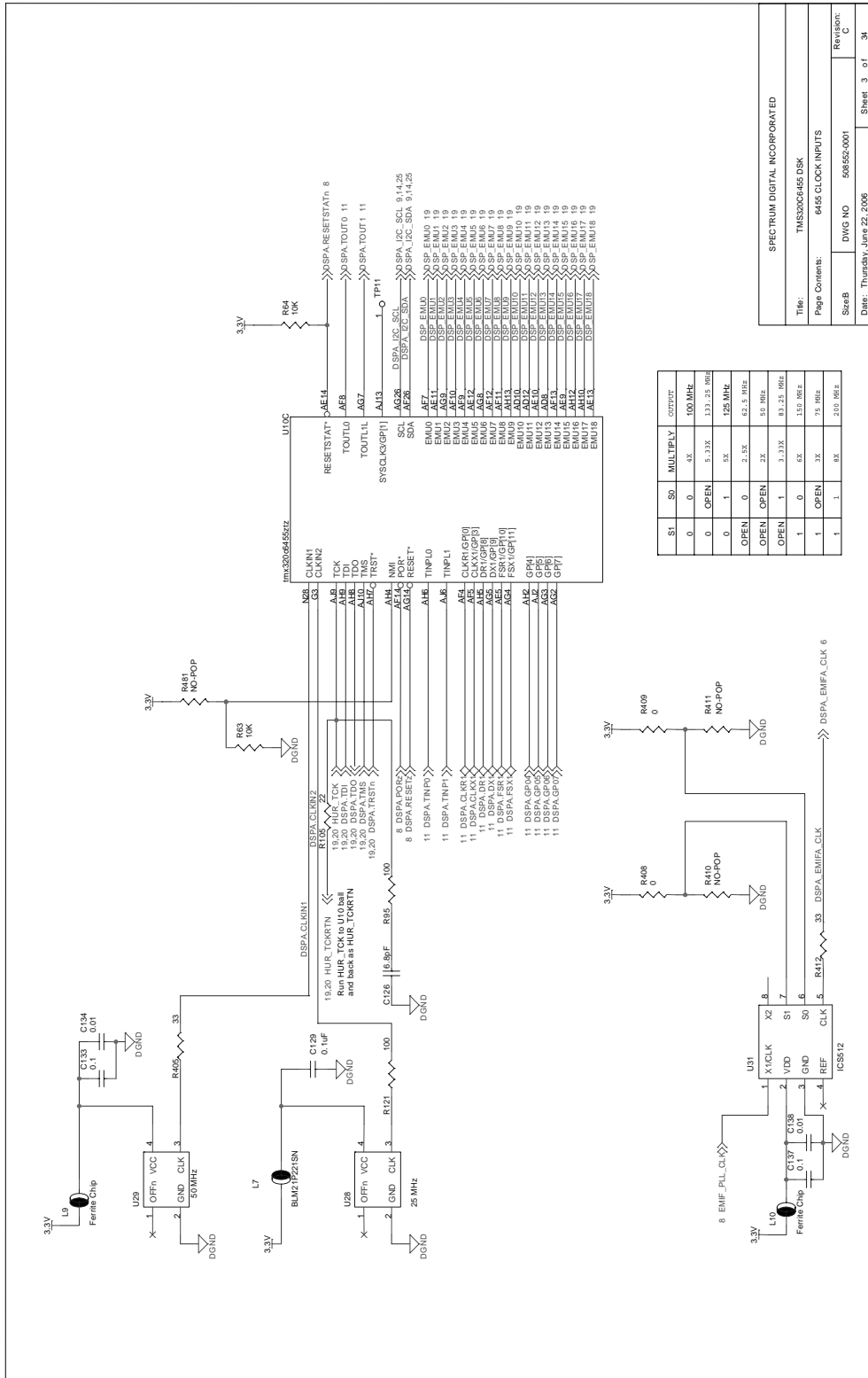
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REV	19	A	A	A	A	A	A	A	A	A
REV	18	A	A	A	A	A	A	A	A	A
REV	17	A	A	A	A	A	A	A	A	A
REV	16	A	A	A	A	A	A	A	A	A
REV	15	A	A	A	A	A	A	A	A	A
REV	14	A	A	A	A	A	A	A	A	A
REV	13	A	A	A	A	A	A	A	A	A
REV	12	A	A	A	A	A	A	A	A	A
REV	11	A	A	A	A	A	A	A	A	A
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REV	9	A	A	A	A	A	A	A	A	A
REV	8	A	A	A	A	A	A	A	A	A
REV	7	A	A	A	A	A	A	A	A	A
REV	6	A	A	A	A	A	A	A	A	A
REV	5	A	A	A	A	A	A	A	A	A
REV	4	A	A	A	A	A	A	A	A	A
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DATE	BY	CHK	APP	DESCRIPTION
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AUG 01, 2005	R.R.P.			
AUG 01, 2005	J.T.C.			
AUG 01, 2005	R.R.P.			
AUG 01, 2005	R.R.P.			
AUG 01, 2005	C.M.D.			
AUG 01, 2005	C.M.D.			
AUG 01, 2005	T.M.K.			

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Title:	TMS320C6455 DSK
Page Contents:	Title Block
Sheet:	DWG NO 50852-0001
Date:	Monday, June 26, 2006
Revision:	C
Sheet:	1 of 34



SPECTRUM DIGITAL INCORPORATED	
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Page Contents:	Options
Size B	DWG NO 598552-0001
Date: Monday, June 26, 2006	Revision: C
Sheet 2 of 34	



SPECTRUM DIGITAL INCORPORATED

Title: TMS320C6455 DSK

Page Contents: 6455 CLOCK INPUTS

Sheet: DWG NO 508552-0001

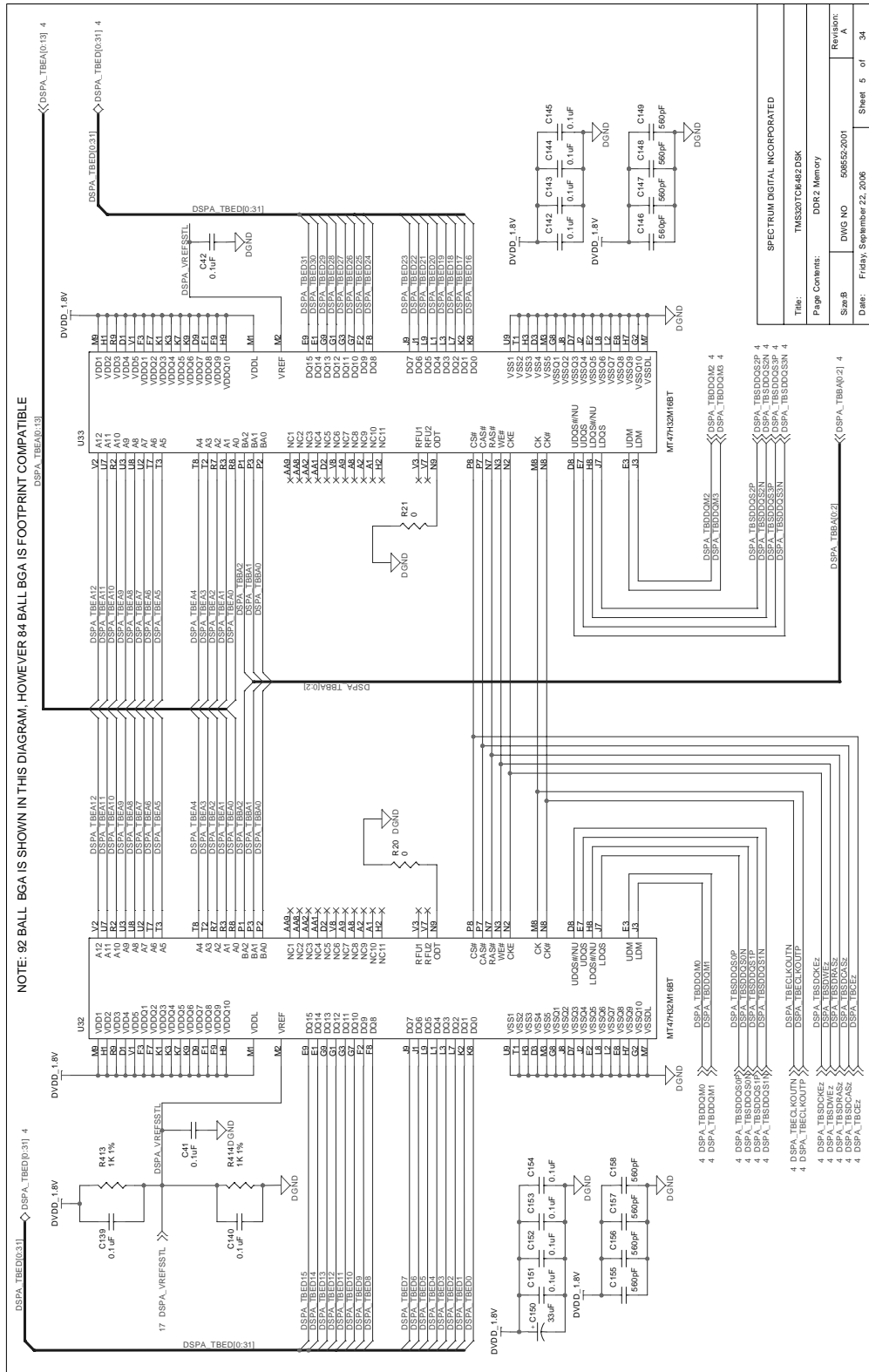
Date: Thursday, June 22, 2006

Revision: C

Sheet 3 of 34

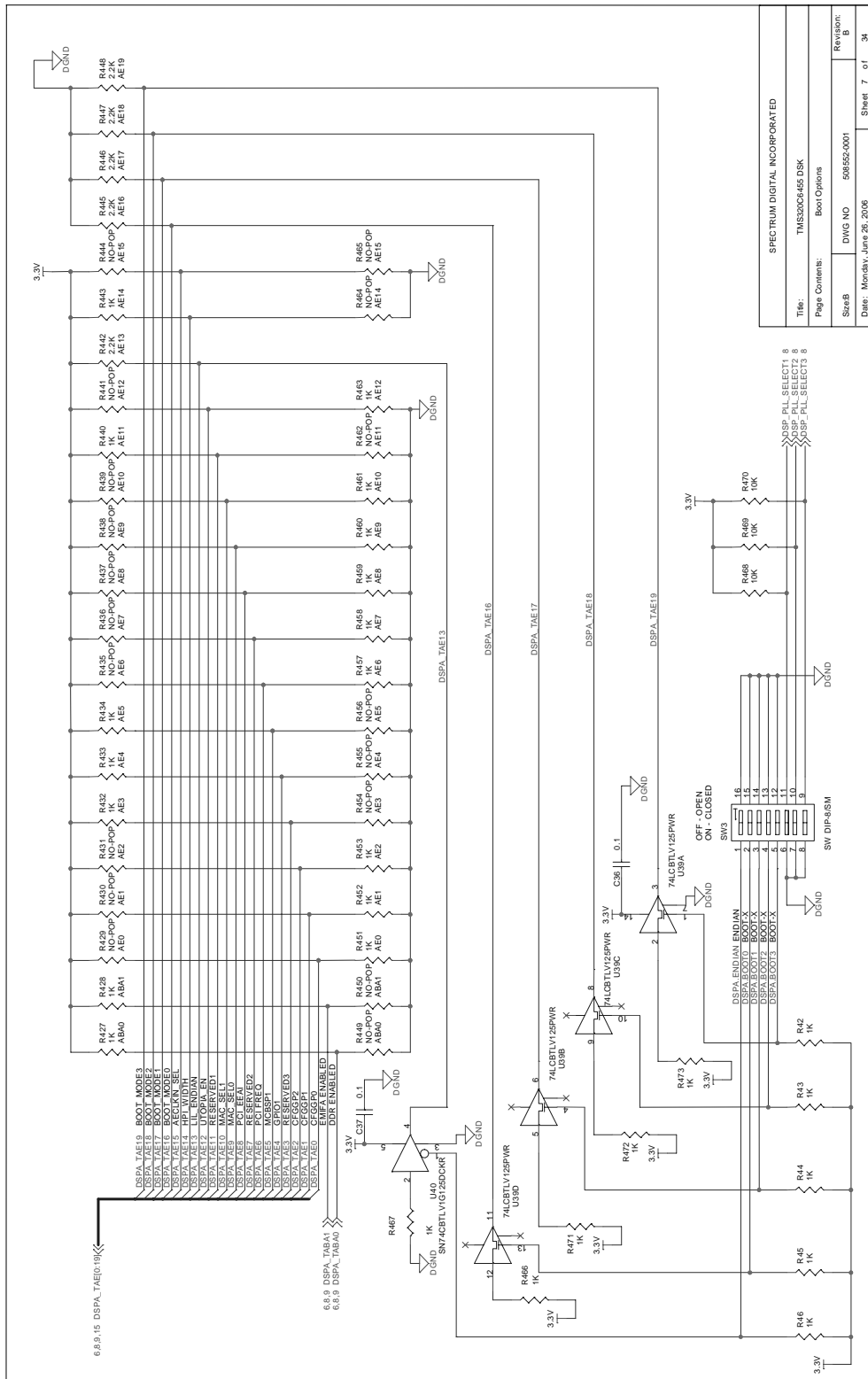
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0	1	OPEN	5.33X 137.25 MHz
0	1	5X	125 MHz
OPEN	0	2.5X	62.5 MHz
OPEN	OPEN	2X	50 MHz
OPEN	1	3.33X	83.25 MHz
1	0	6X	150 MHz
1	OPEN	7X	75 MHz
1	1	8X	200 MHz

NOTE: 92 BALL BGA IS SHOWN IN THIS DIAGRAM, HOWEVER 84 BALL BGA IS FOOTPRINT COMPATIBLE

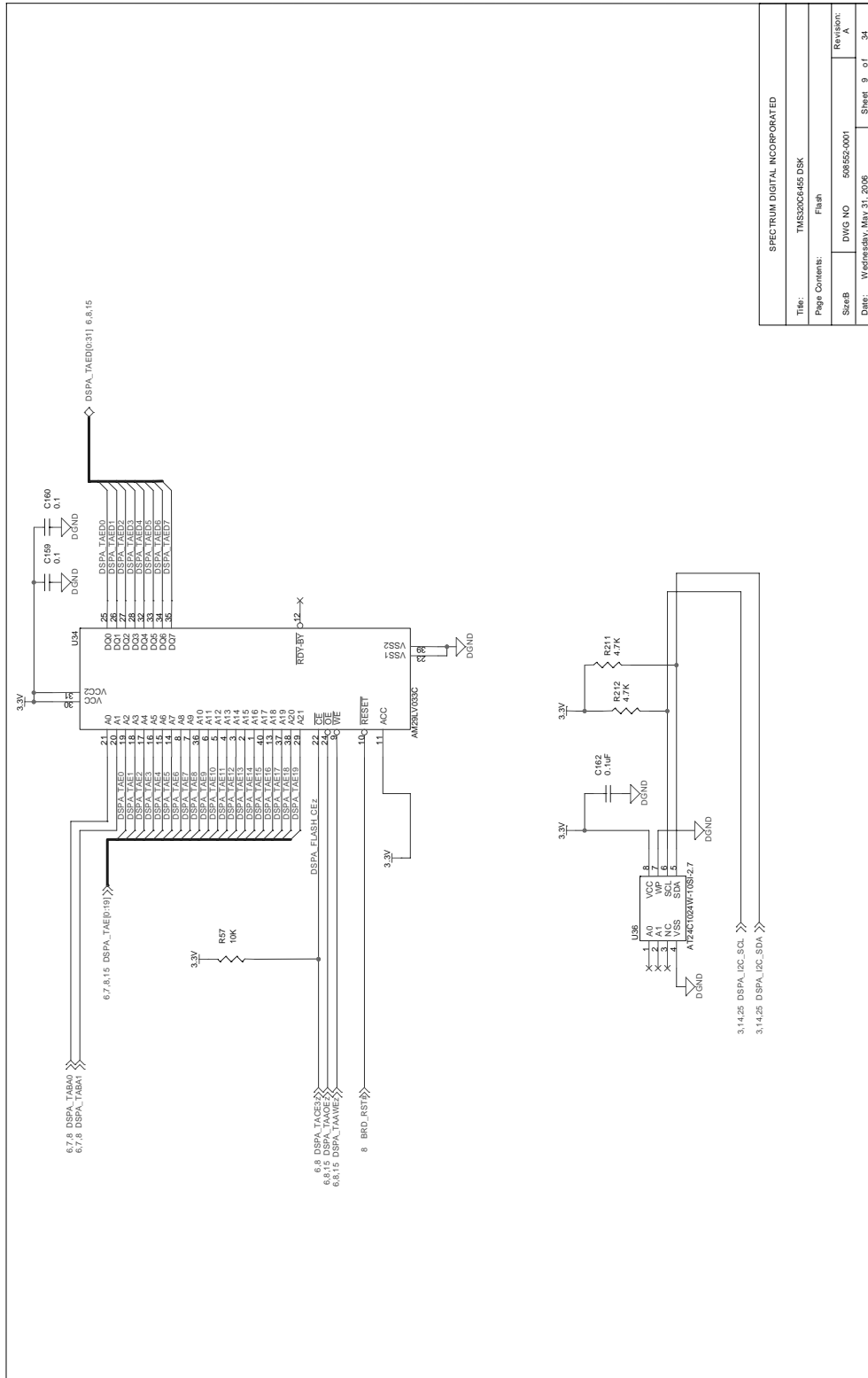


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Date: Friday, September 22, 2006

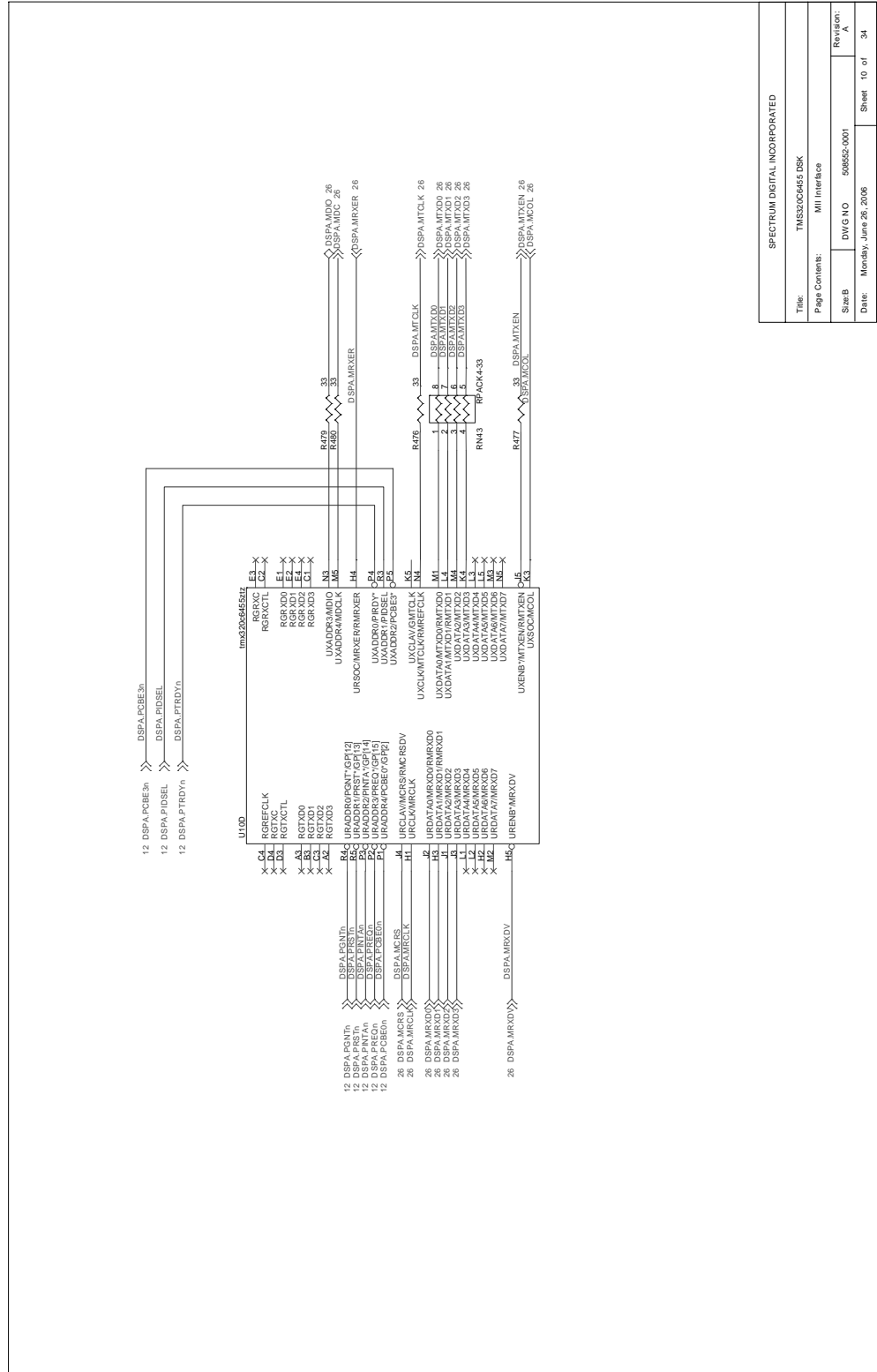
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Sheet 5 of 34



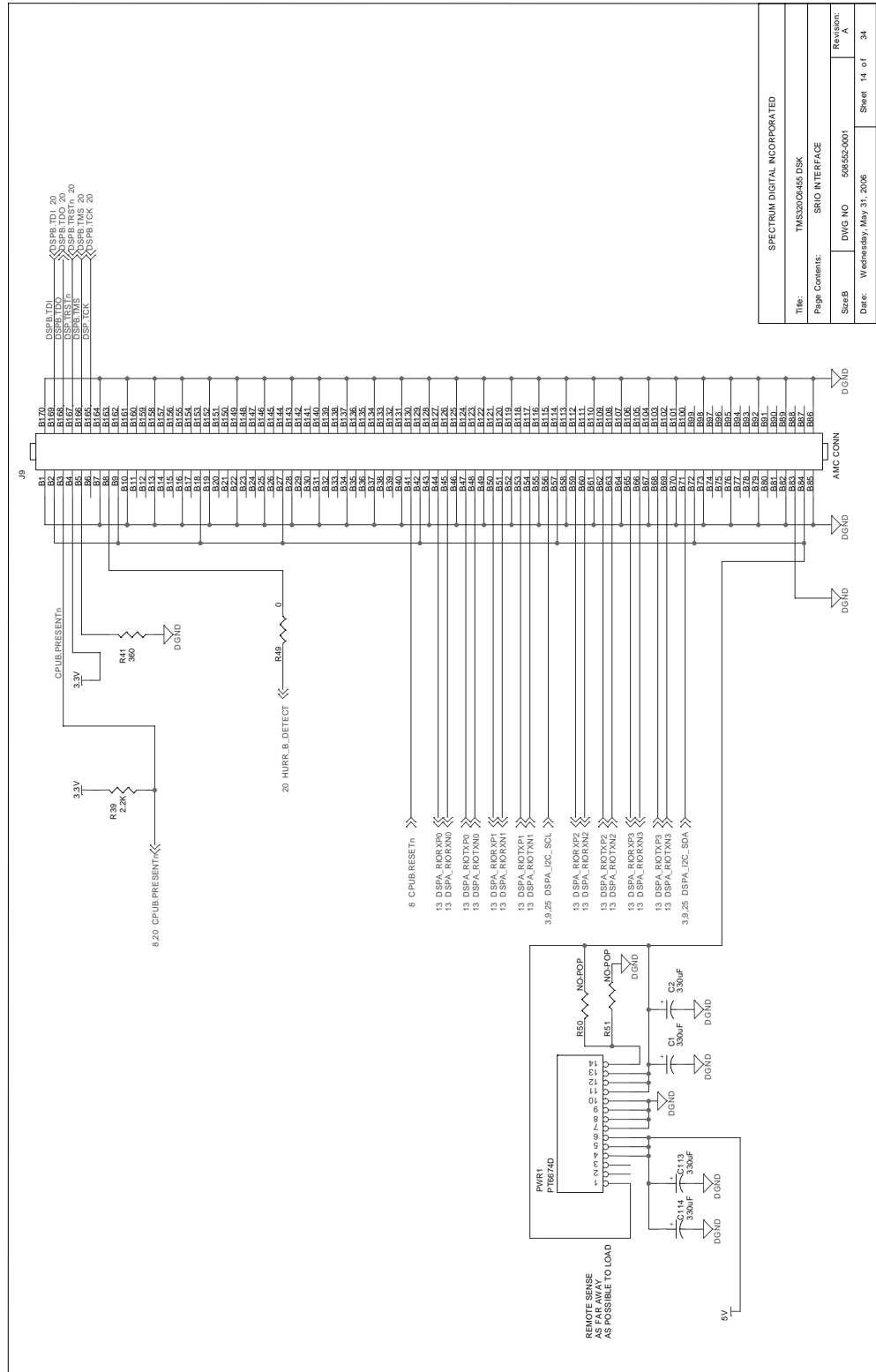
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Revision:	B
Sheet:	7 of 34



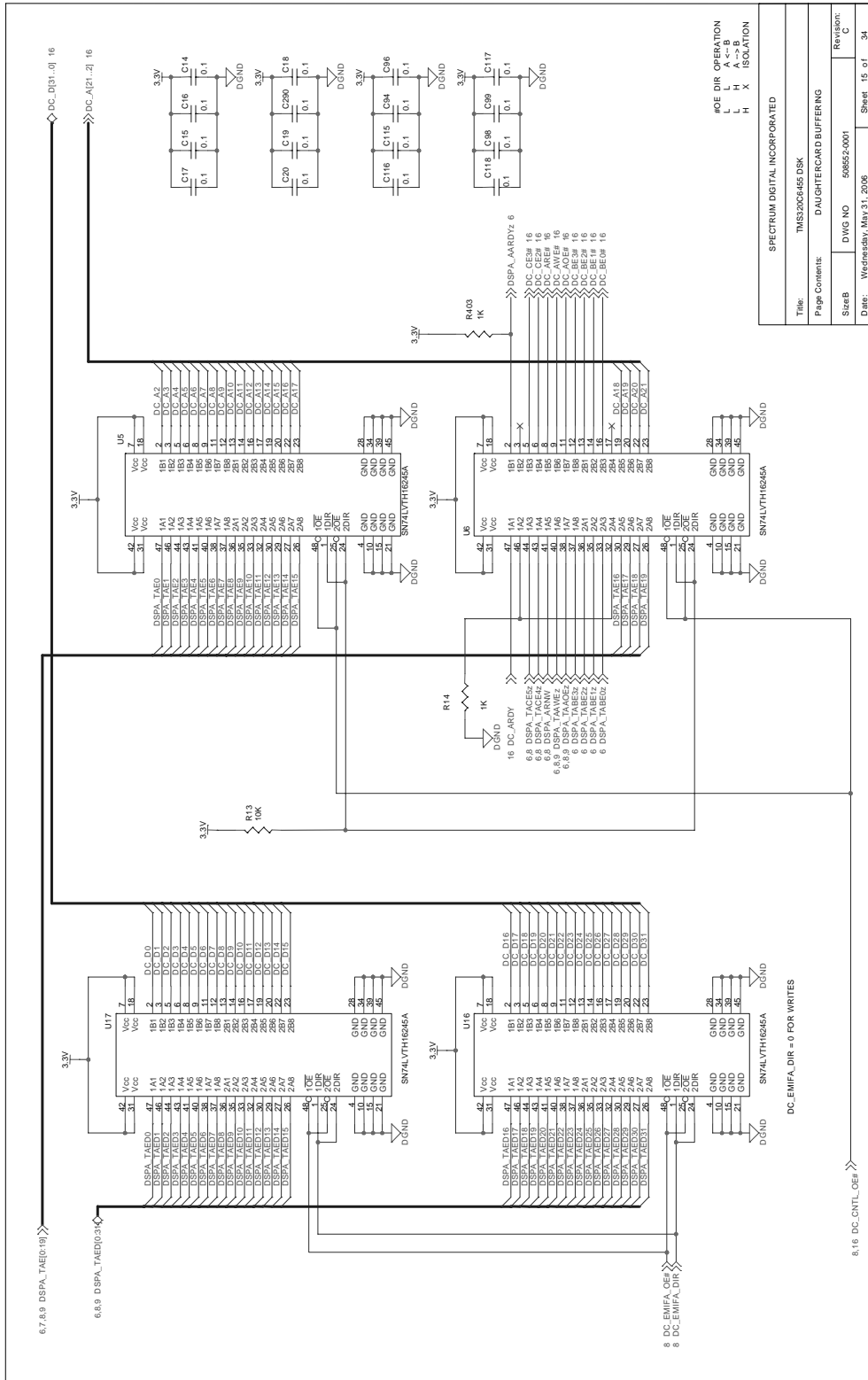
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Date:	Wednesday, May 31, 2006	Sheet 9 of 34	



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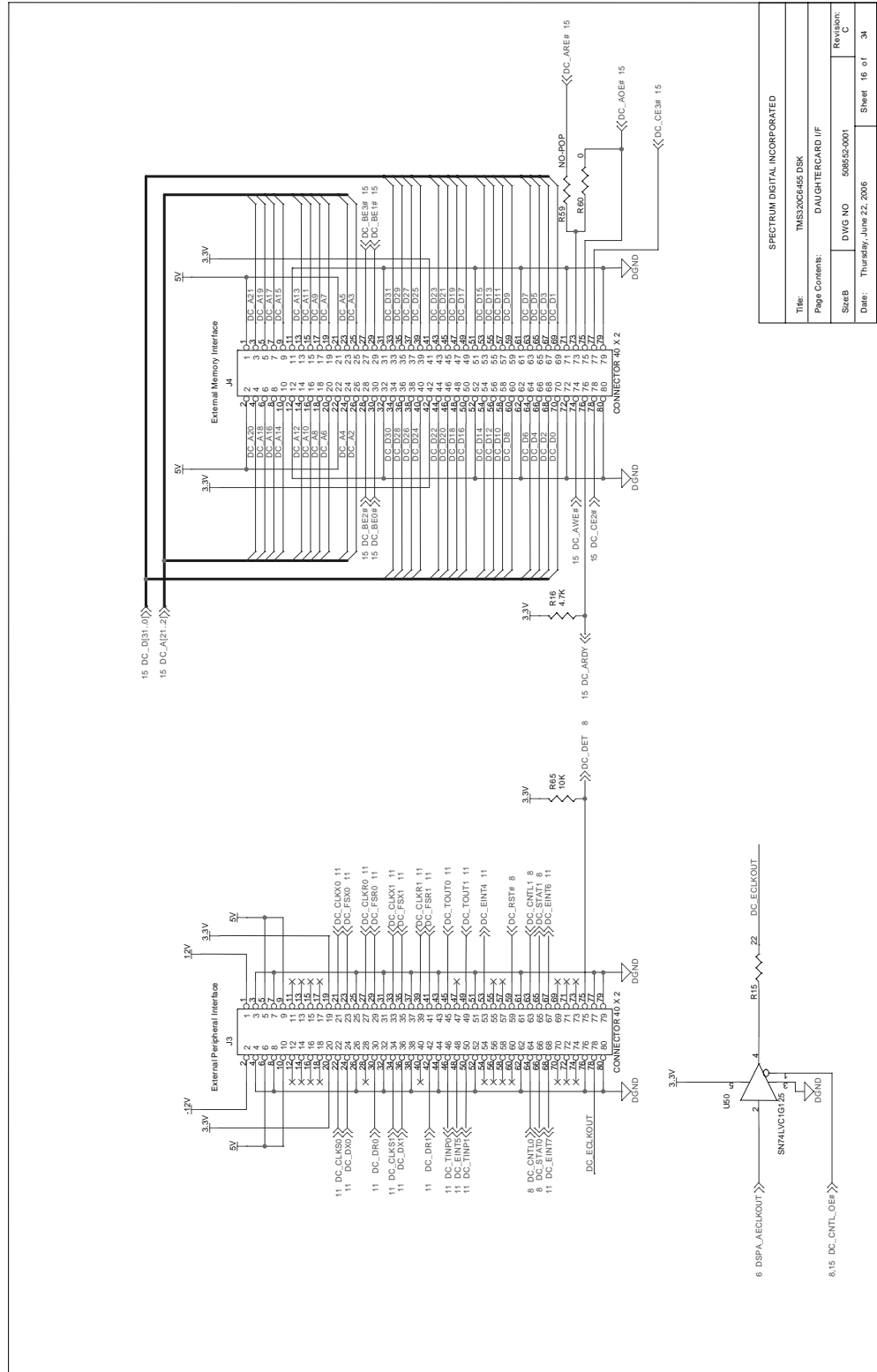


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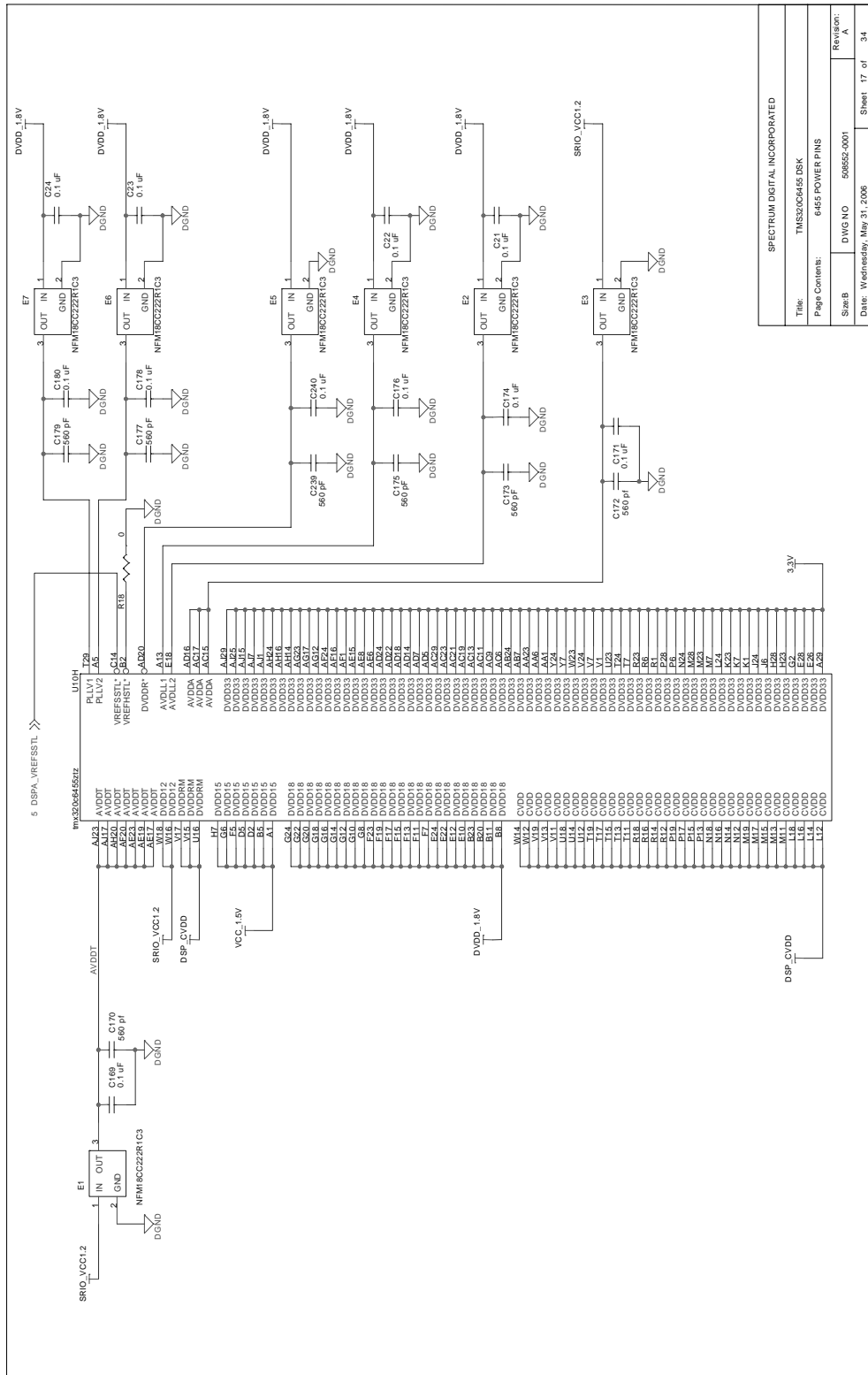


MODE DIR OPERATION
L L A-<-B
L H A->-B
H X ISOLATION

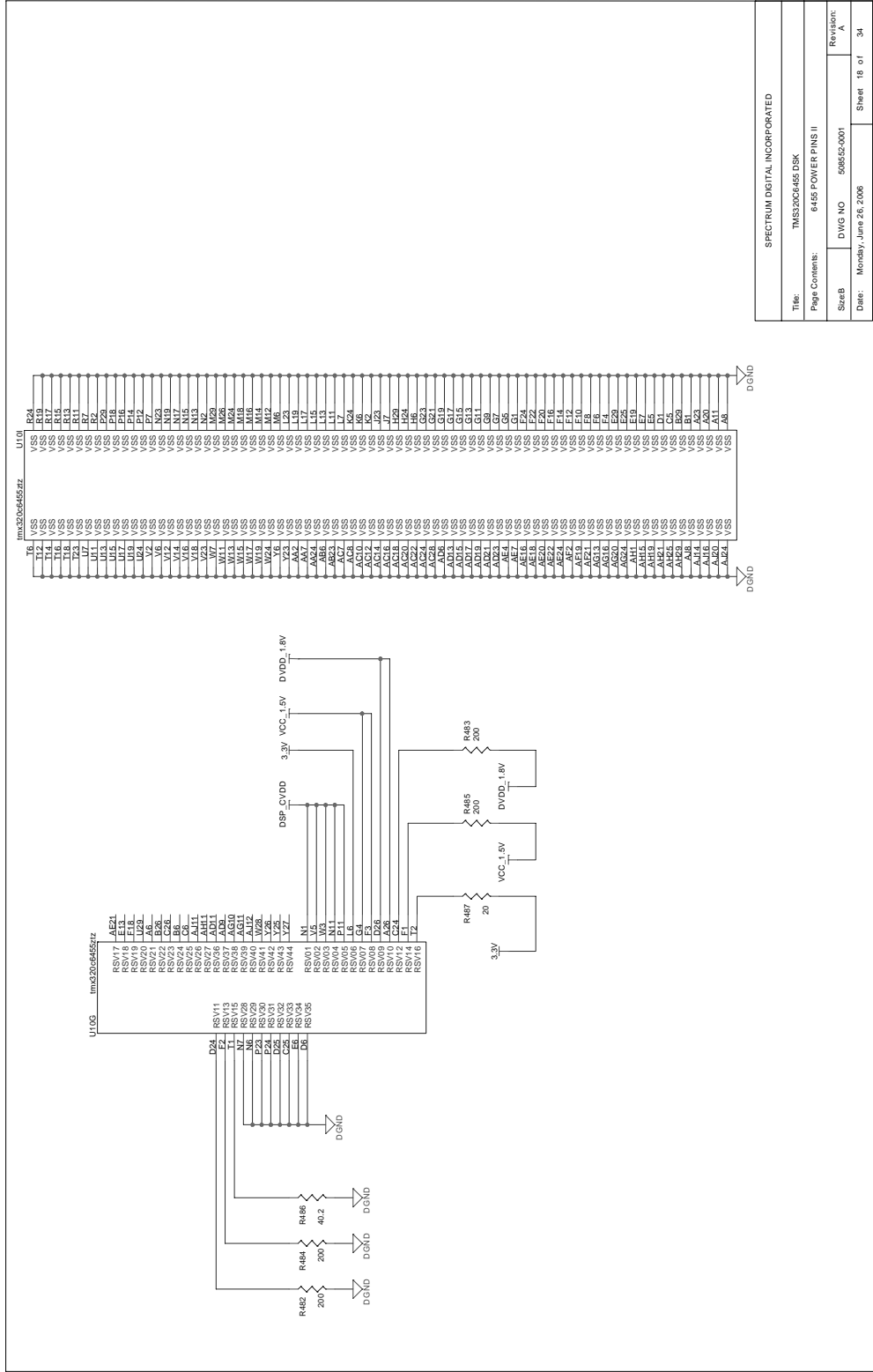
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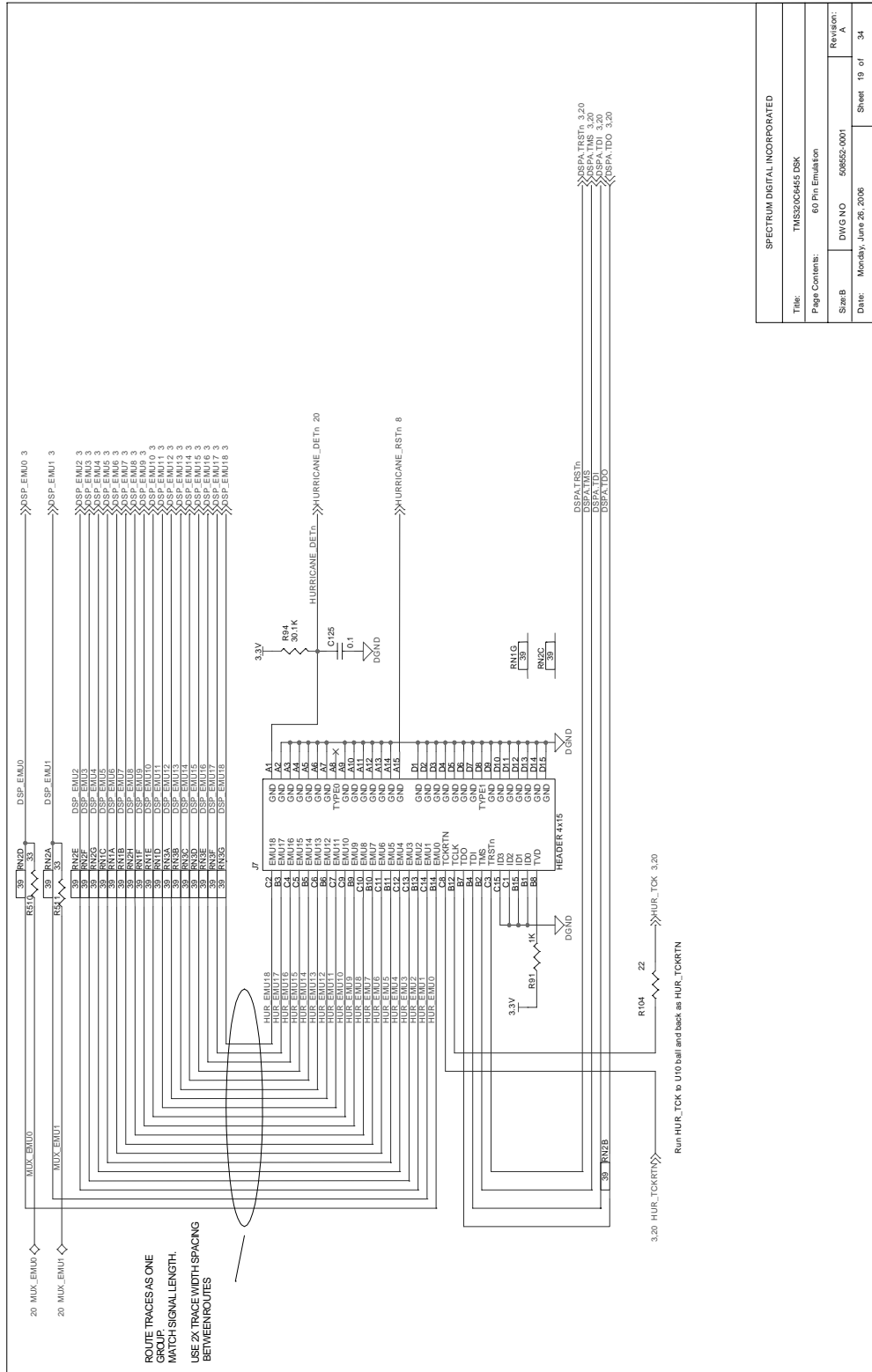


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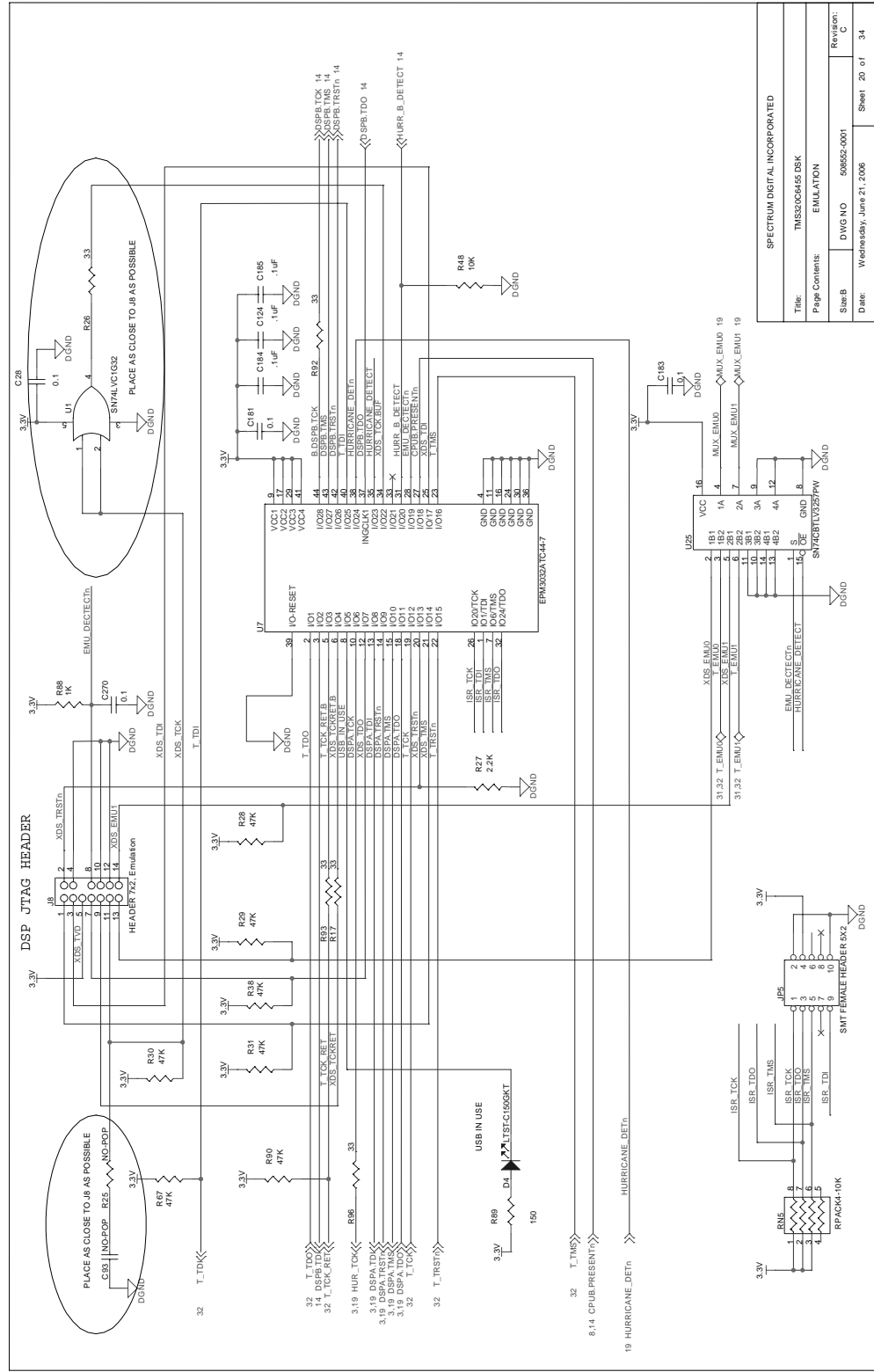


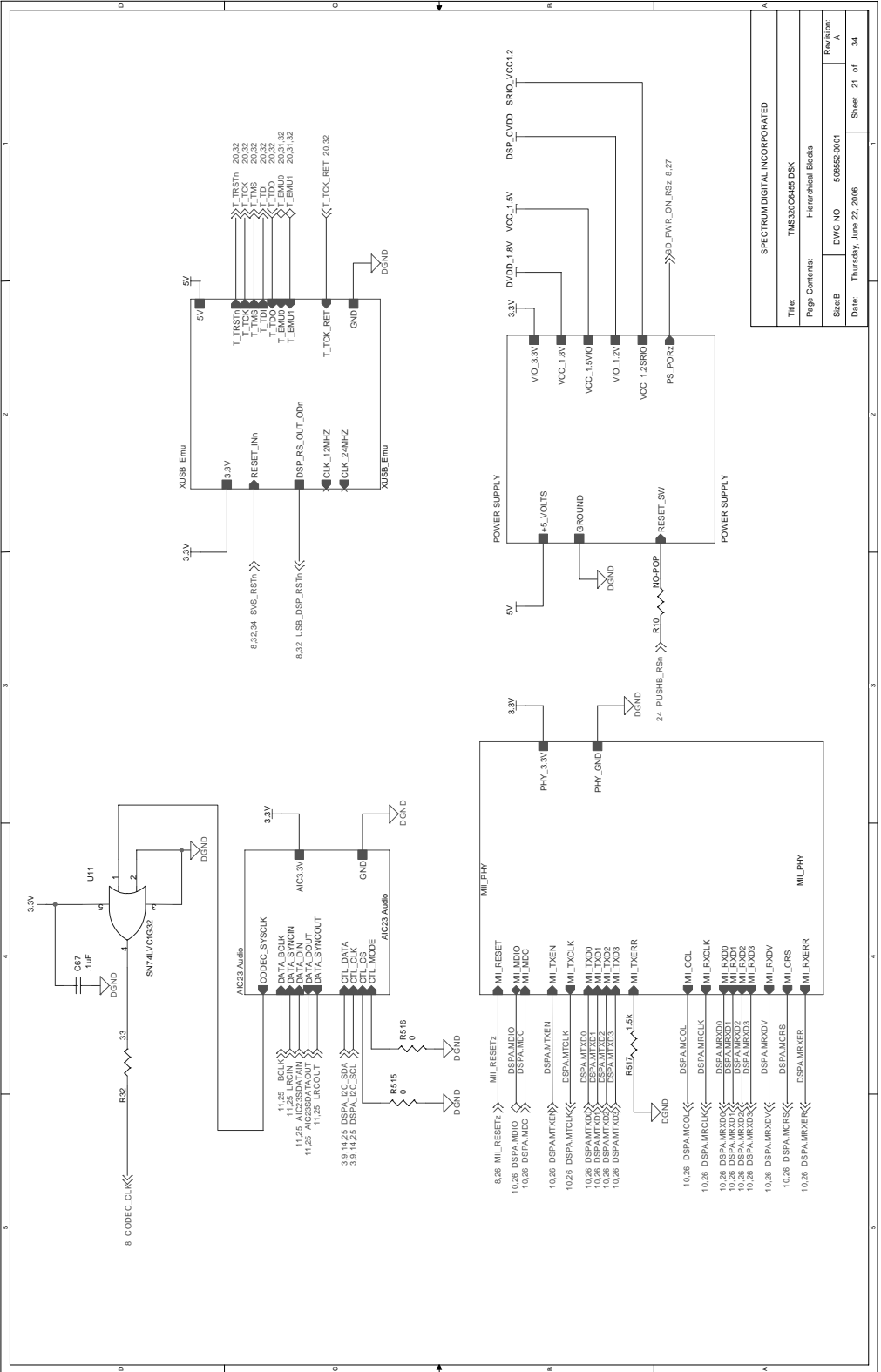
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Sheet:	DWG110 508552-0001
Date:	Wednesday, May 31, 2006
Revision:	A
Sheet:	17 of 34



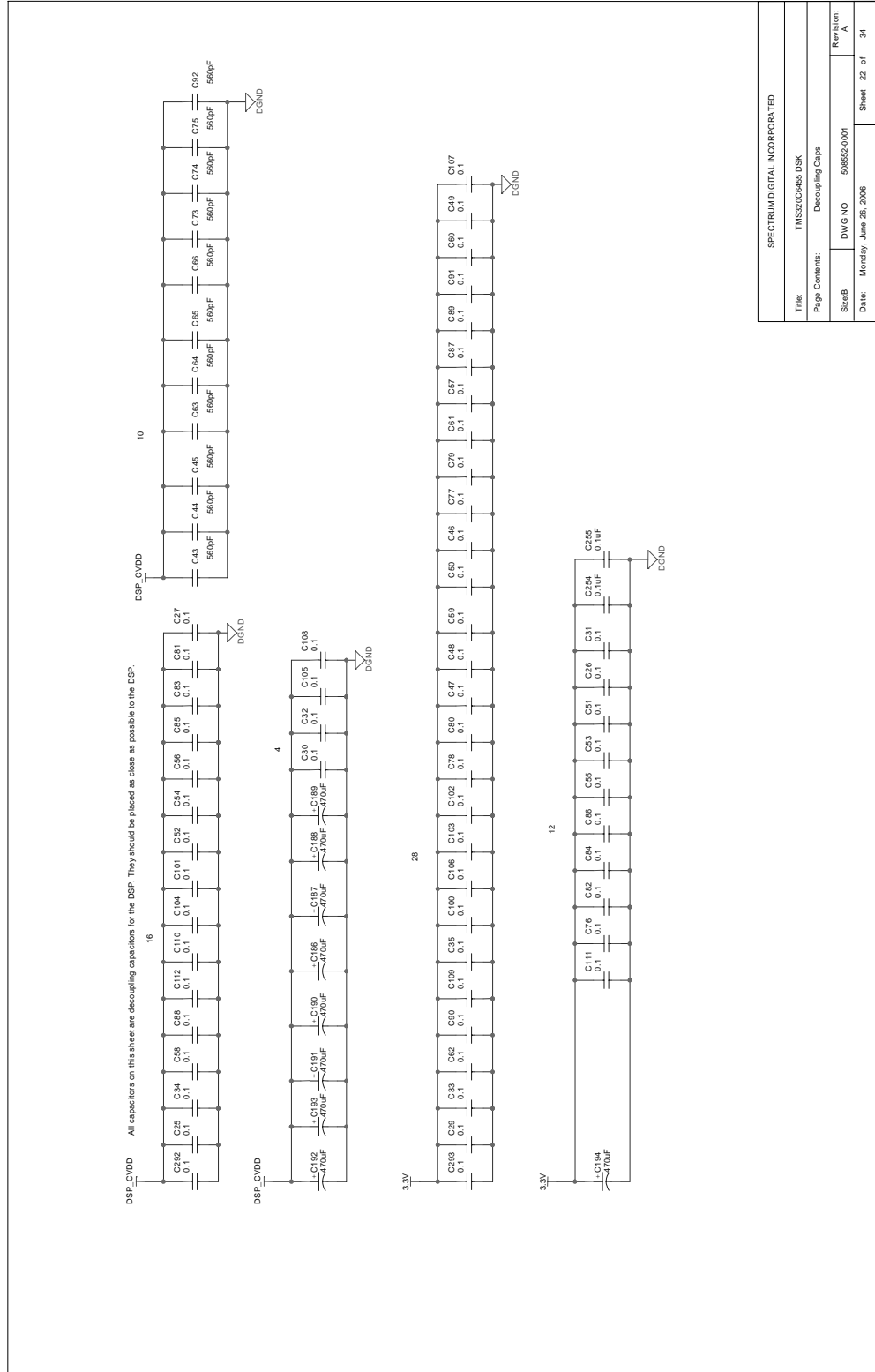


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Date:	Monday, June 26, 2006		Sheet 19 of 34

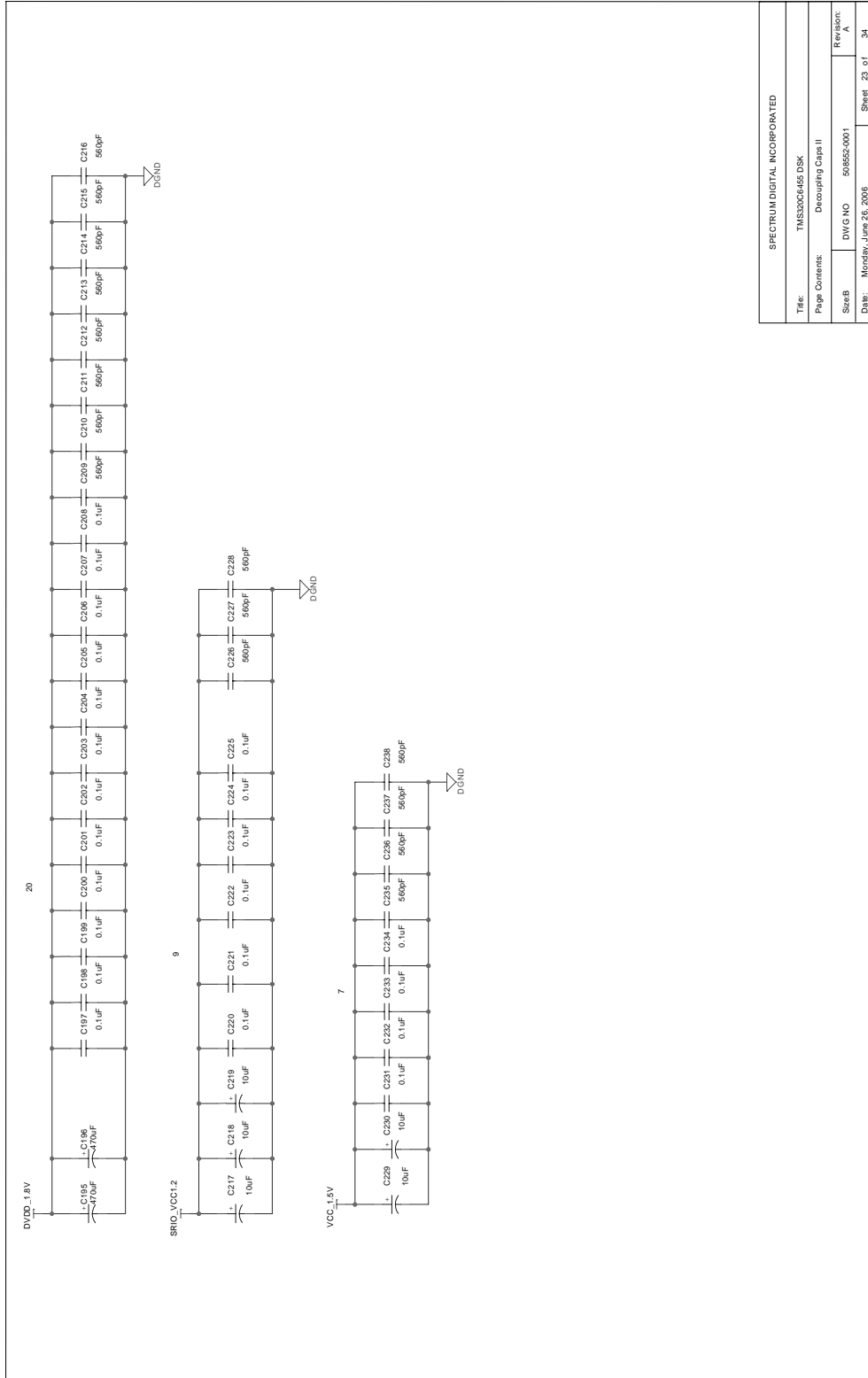




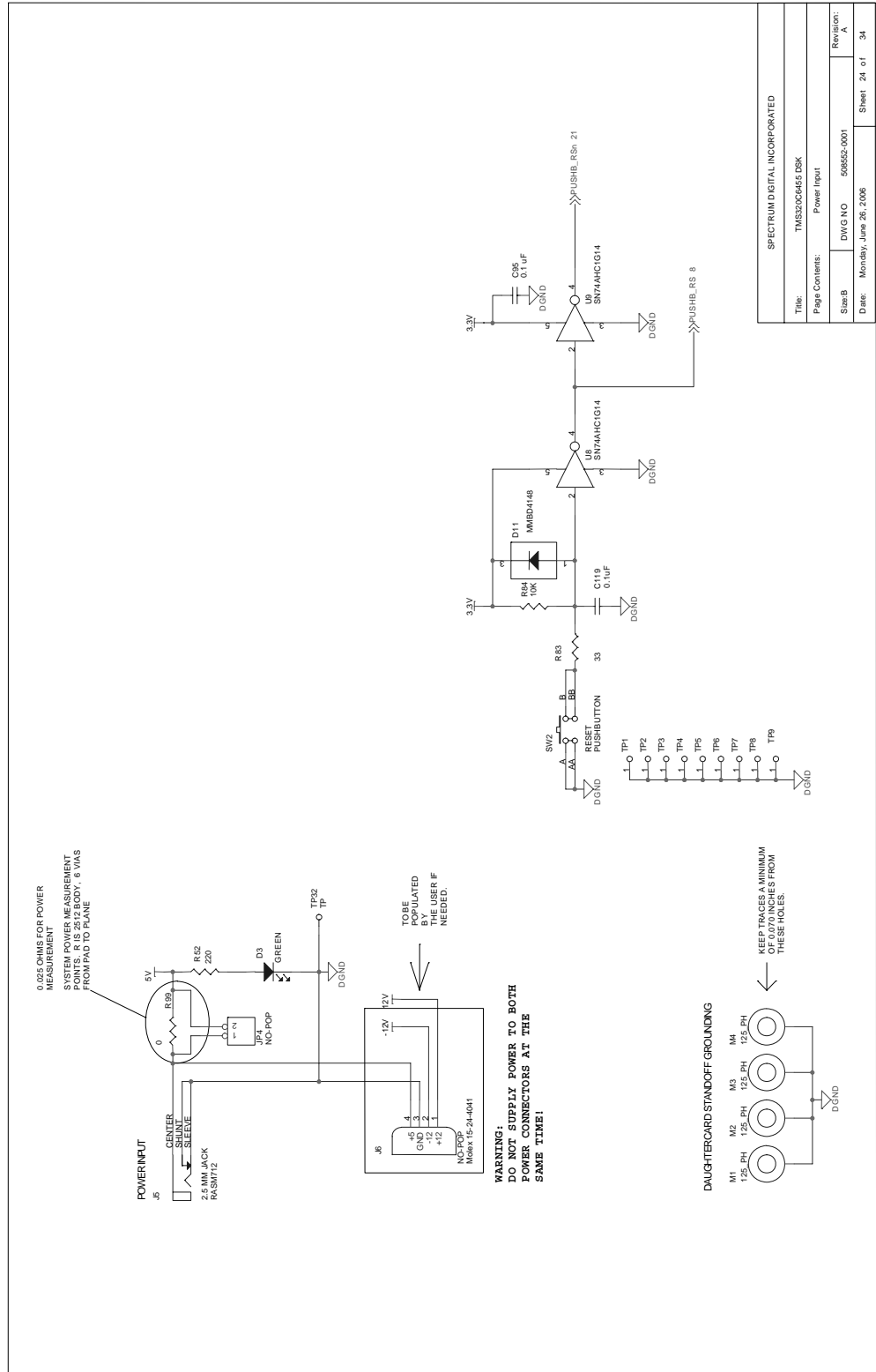
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		Sheet 21 of 34



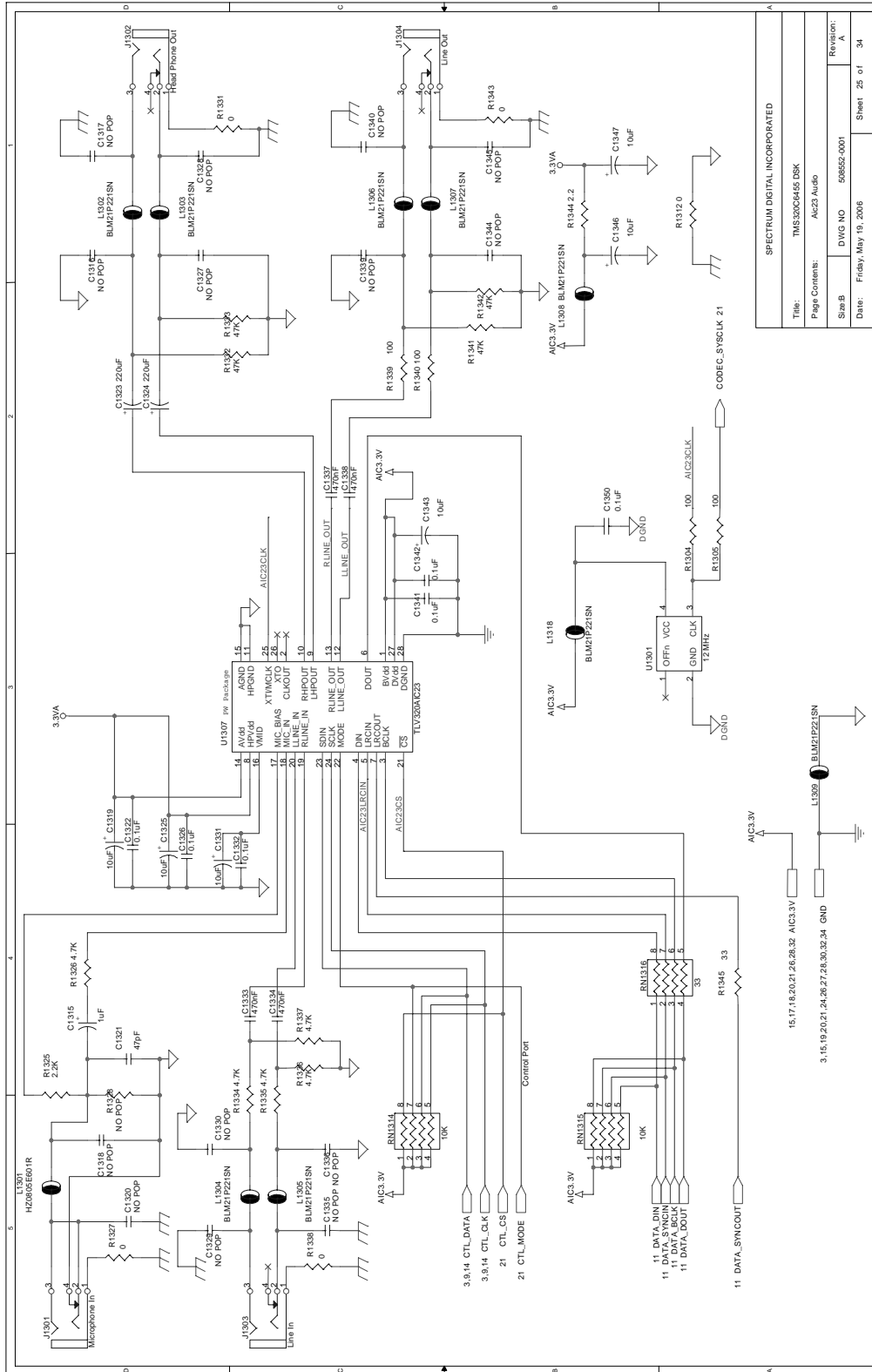
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Page Contents:	Decoupling Caps		
Sheet:	DWG/NO	598552-0001	Revision: A
Date:	Monday, June 28, 2006	Sheet	22 of 34



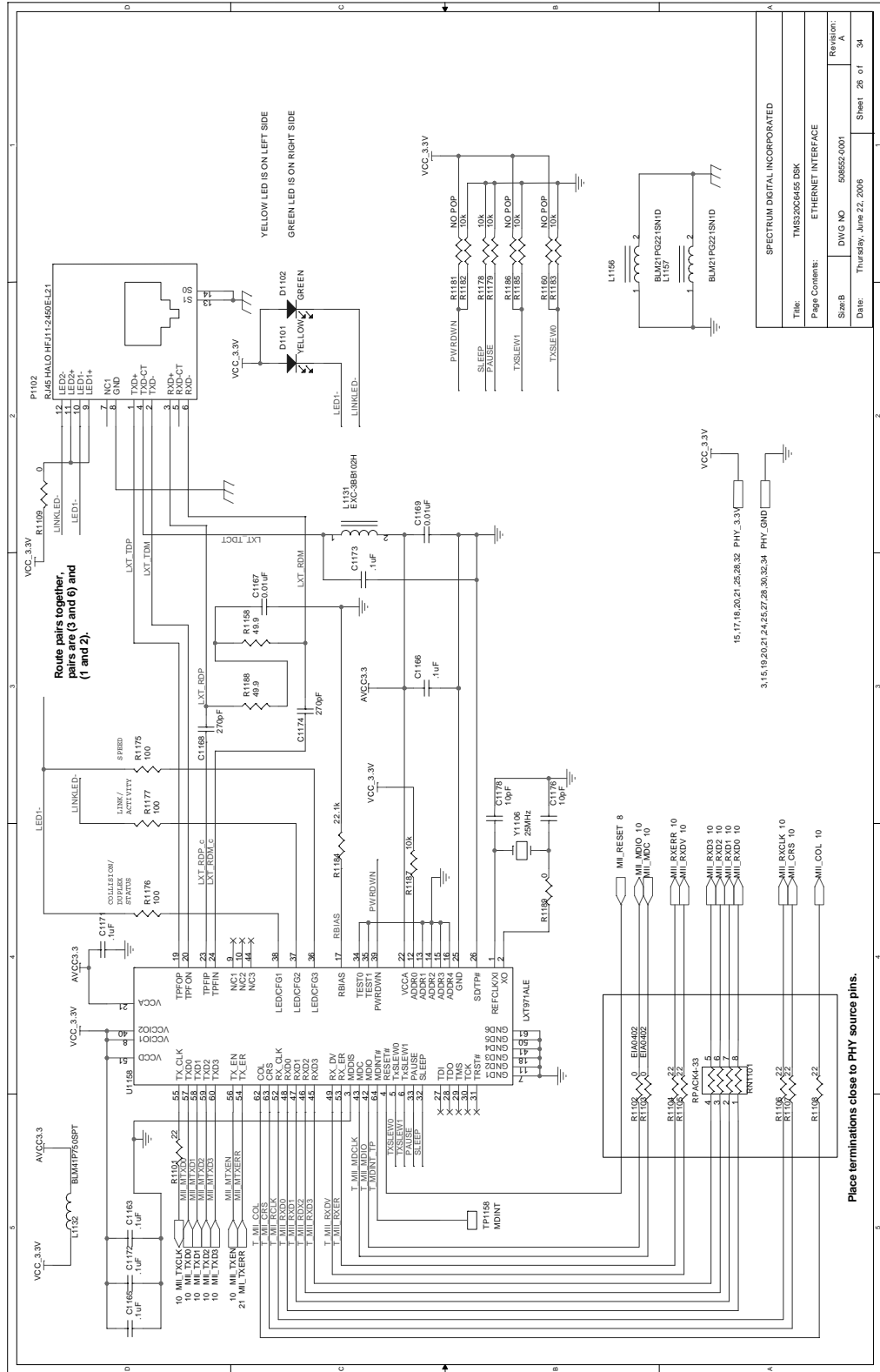
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Page Contents:	Decoupling Caps II
SizeB:	DWG NO 50655-001
Date:	Monday, June 26, 2006
Revision:	A
Sheet	23 of 34



Title:		TM352006466 DSK	
Page Contents:		Power Input	
Size B	DWG NO	508552-0001	Revision: A
Date:	Monday, June 26, 2006	Sheet	24 of 34



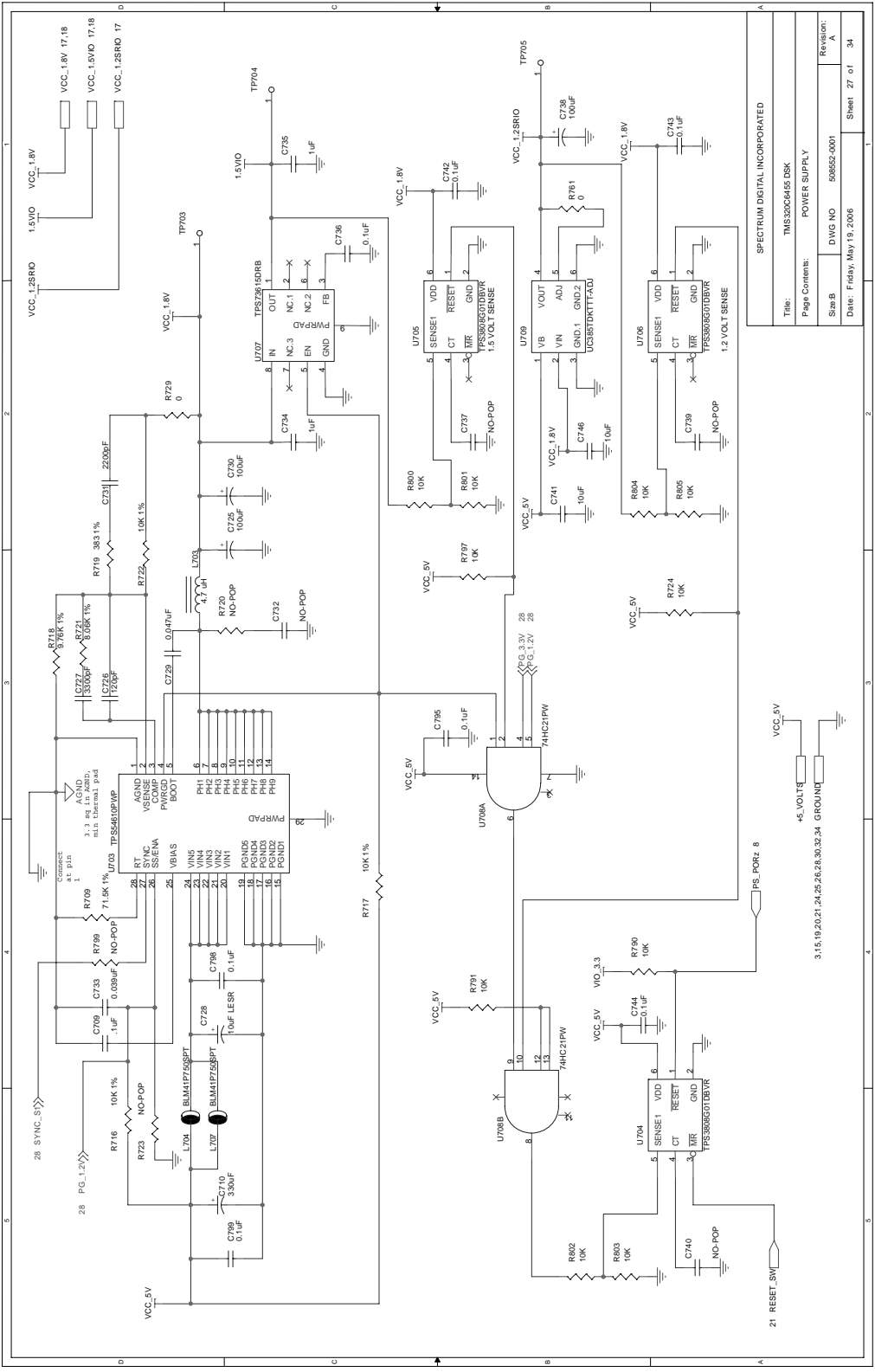
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Page Contents:	AC23 Audio
Sub B:	DWG NO 508552-0001
Date:	Friday, May 19, 2006
Revision:	A
Sheet	25 of 34



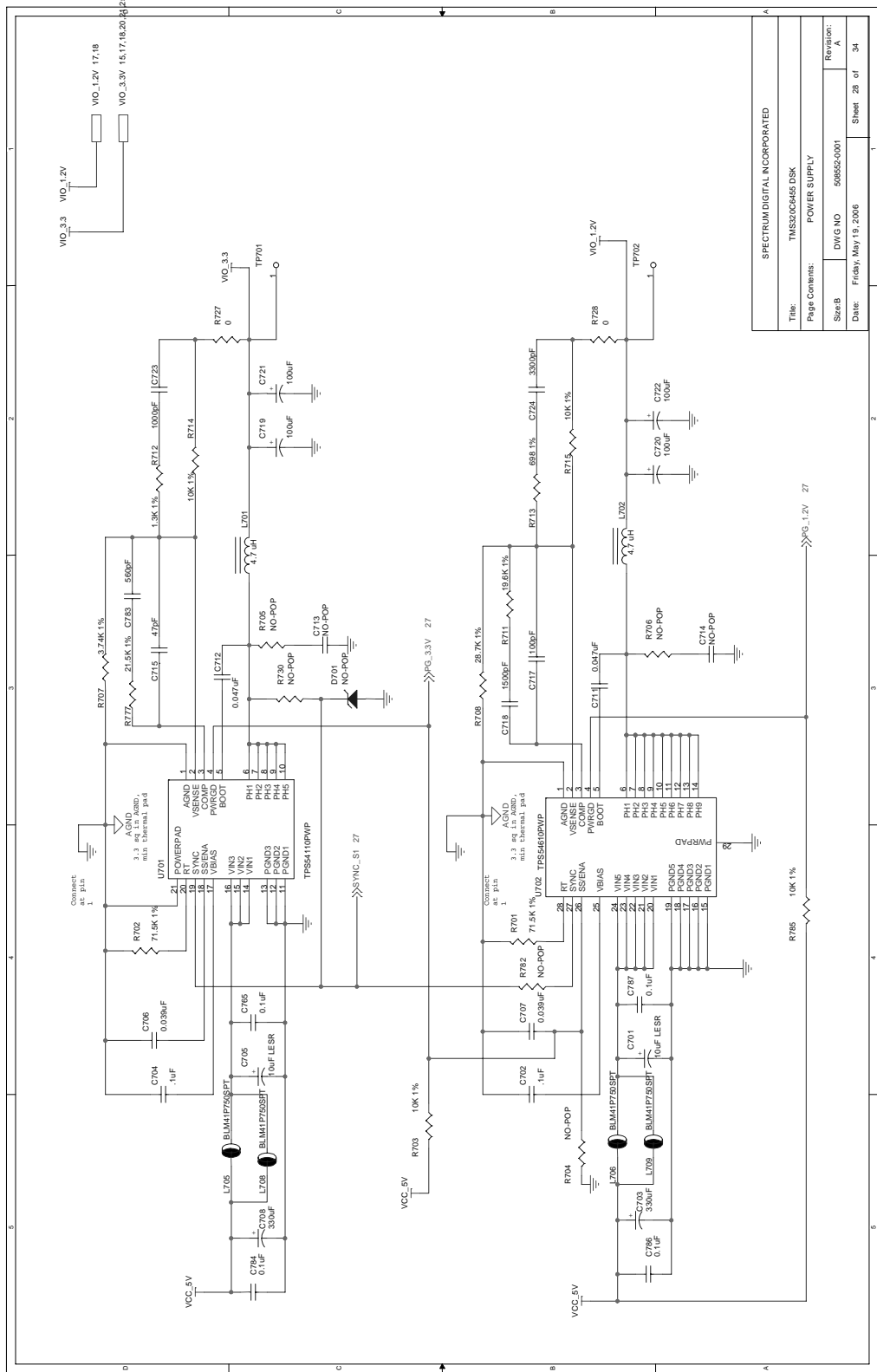
Route pairs together, pairs are (3 and 6) and (1 and 2).

Place terminations close to PHY source pins.

SPECTRUM DIGITAL INCORPORATED	
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Page Contents:	ETHERNET INTERFACE
Size B	DWG NO 506562-0001
Date:	Thursday, June 22, 2006
Revision:	A
Sheet	26 of 34



SPECTRUM DIGITAL INCORPORATED	
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Page Contents:	POWER SUPPLY
Sheet B:	DWG NO 598552-0001
Date:	Friday, May 19, 2006
Sheet	27 of 34

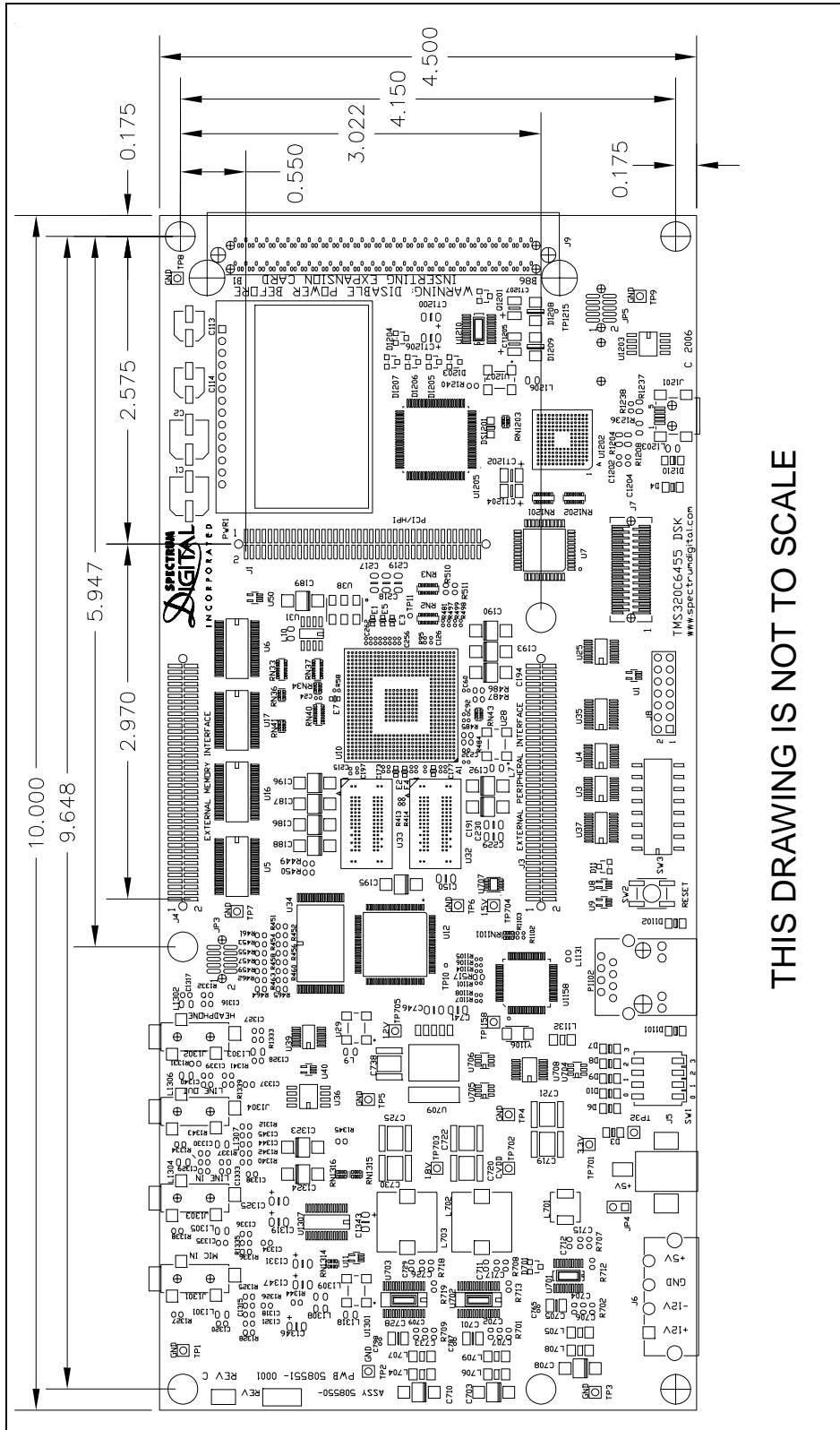


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Title:	TMS320C6455.DSK
Page Contents:	POWER SUPPLY
Sheet B	DWG NO 508552-001
Date:	Friday, May 19, 2006
Revision:	A
Sheet 28 of	34

Appendix B

Mechanical Information

This appendix contains the mechanical information about the TMS320C6455 DSK produced by Spectrum Digital.



THIS DRAWING IS NOT TO SCALE

Appendix C

Schematics

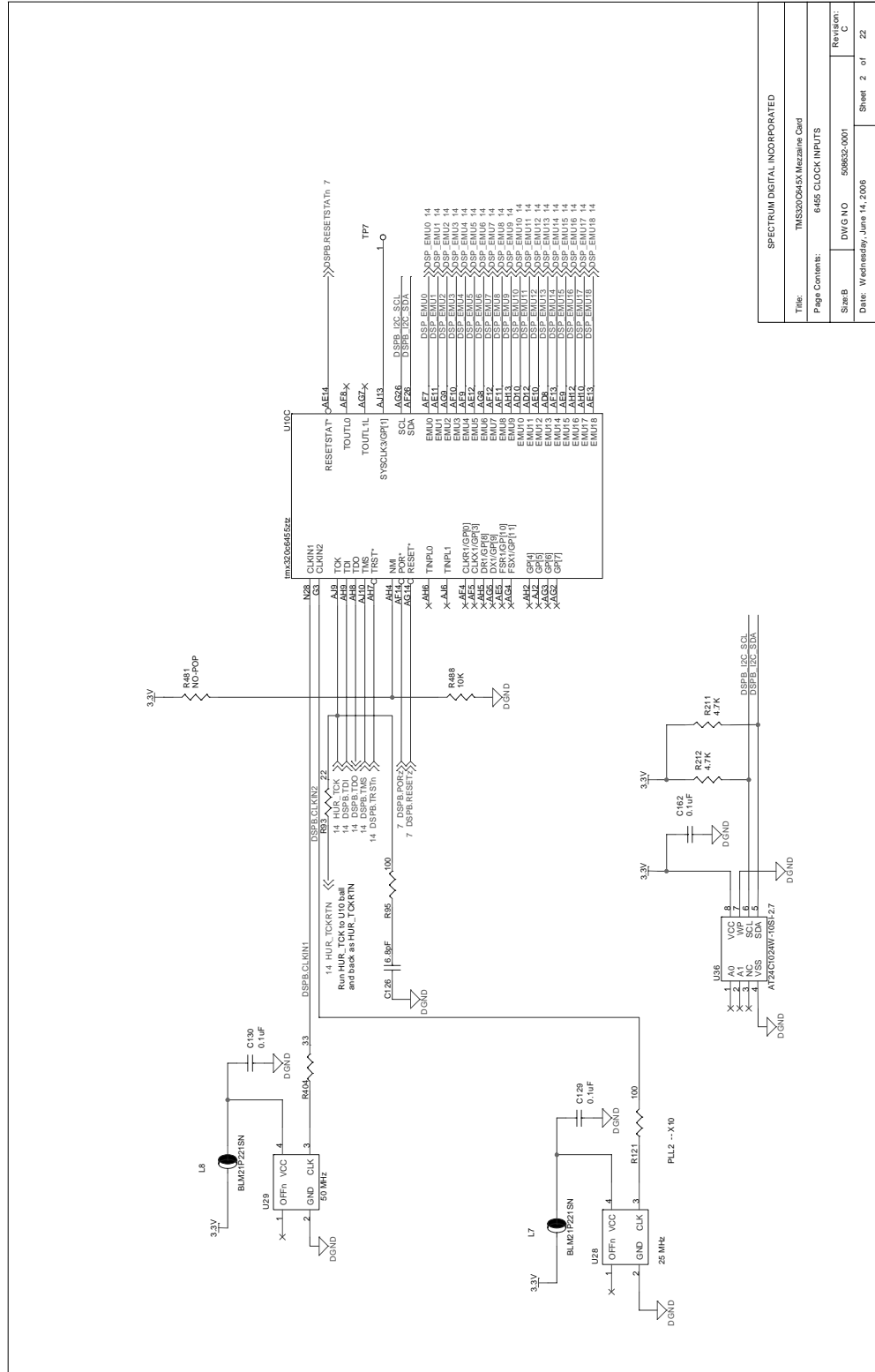
This appendix contains the schematics for the TMS320C6455 mezzanine Board.

SCHEMATIC CONTENTS:

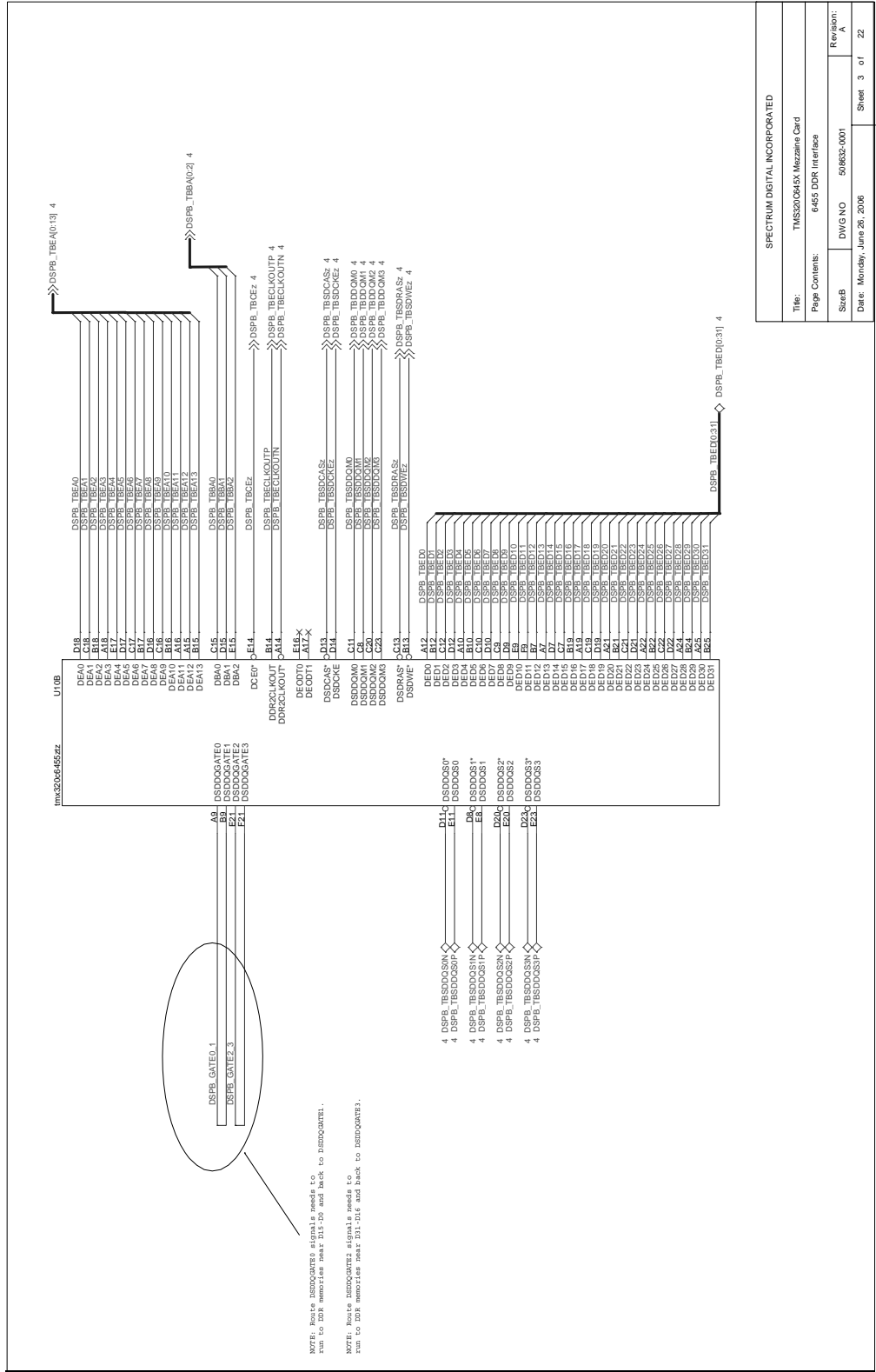
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- 2 Clock Inputs
- 3 645X DDR2 Interface
- 4 DDR2 Memories
- 5 645X EMIF A
- 6 BOOT Options
- 7 CPLD
- 8 645X MII INTERFACE
- 9 645X HOST PORT INTERFACE
- 10 645X SPIO INTERFACE
- 11 645X POWER PINS I
- 12 645X POWER PINS II
- 13 645X EMULATION
- 14 645X EMULATION INTERFACE
- 15 HIERARCHICAL BLOCKS
- 16 645X DECOUPLING CAPS I
- 17 645X DECOUPLING CAPS II
- 19 POWER SUPPLIES I
- 20 POWER SUPPLIES II
- 21 ETHERNET PHY
- 22 ETHERNET PHY
- 23 ETHERNET PHY

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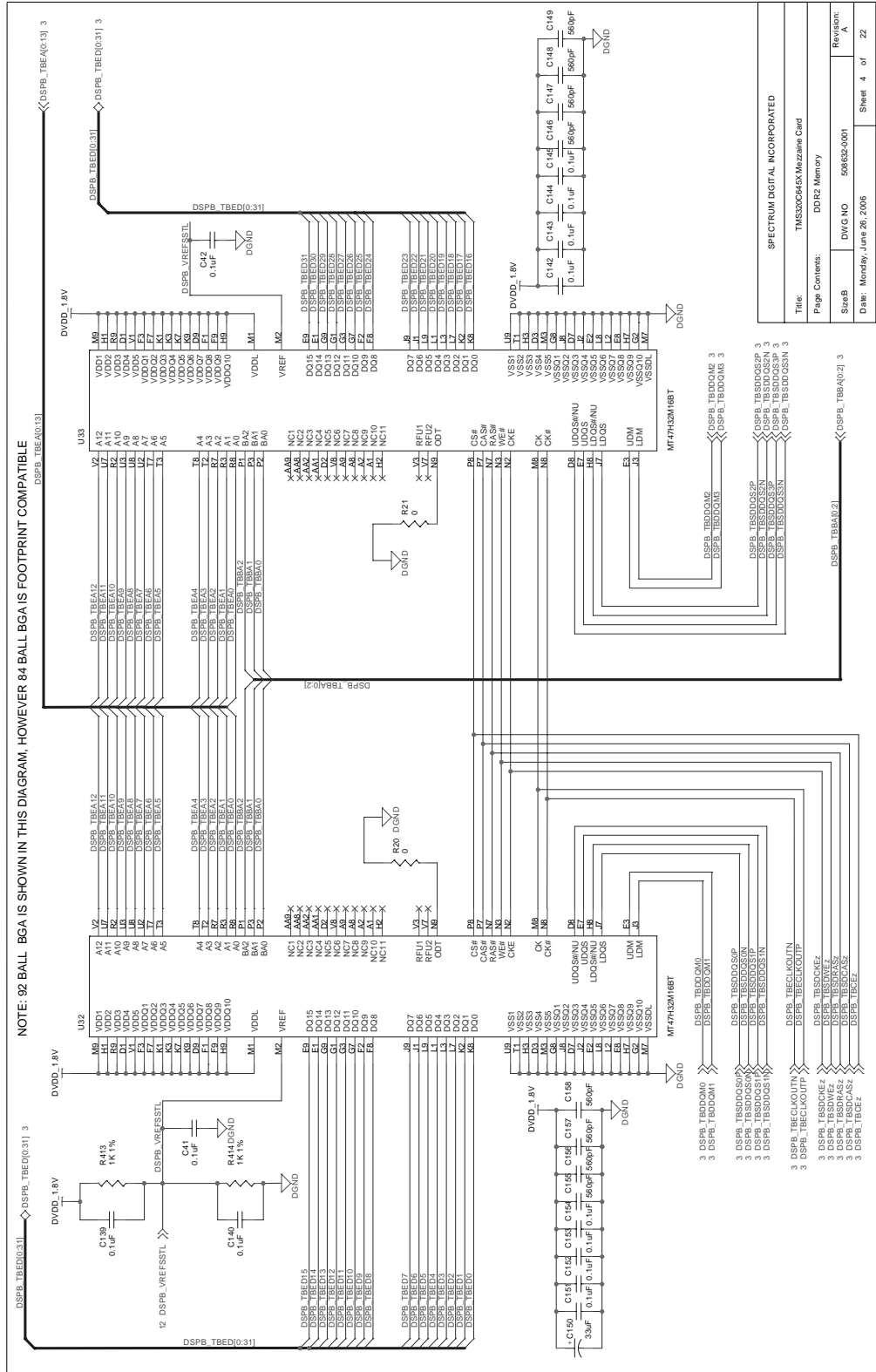
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Date:	Wednesday, June 14, 2006
Revision:	C
Sheet:	1 of 22



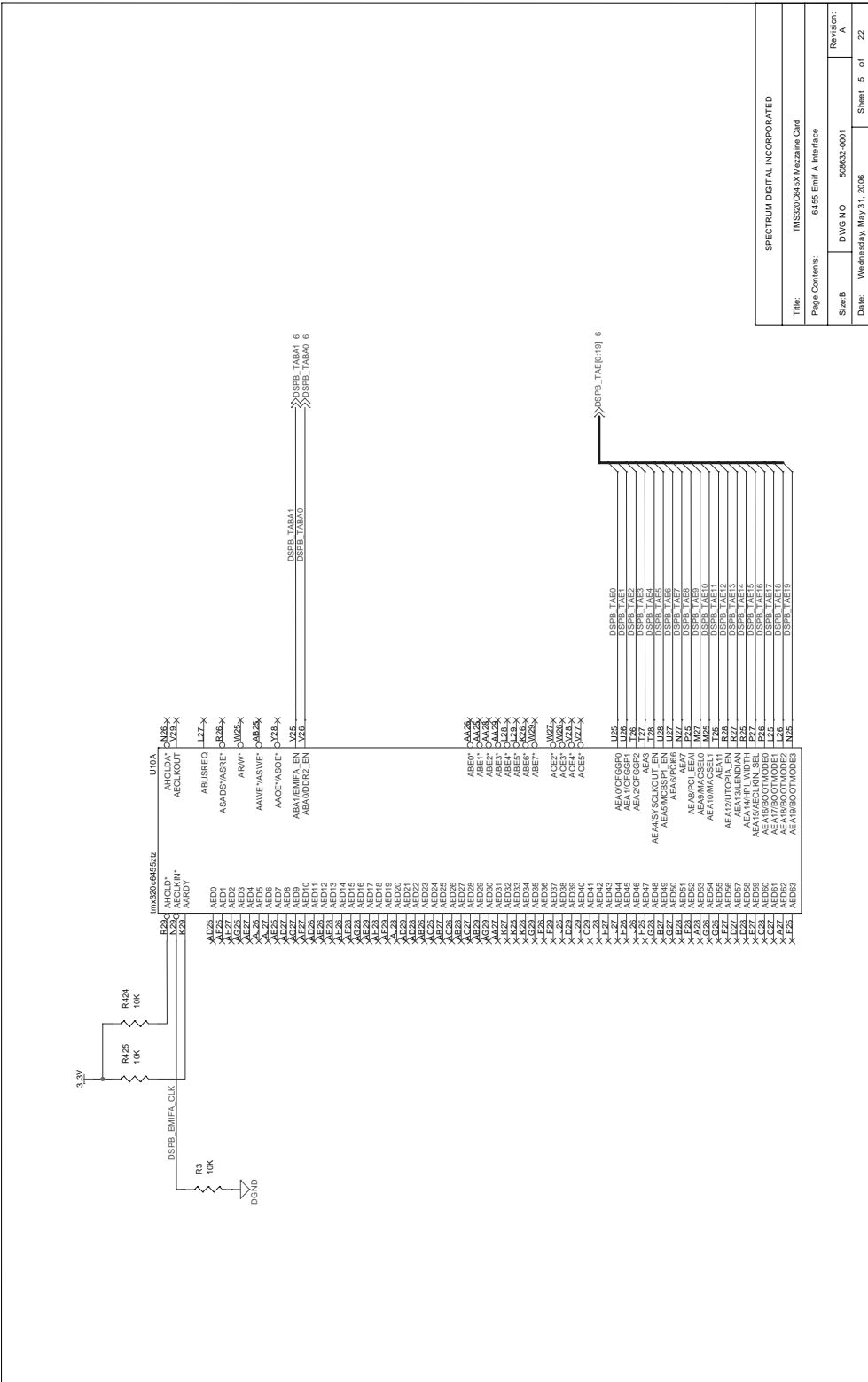
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	Sheet	2	of 22



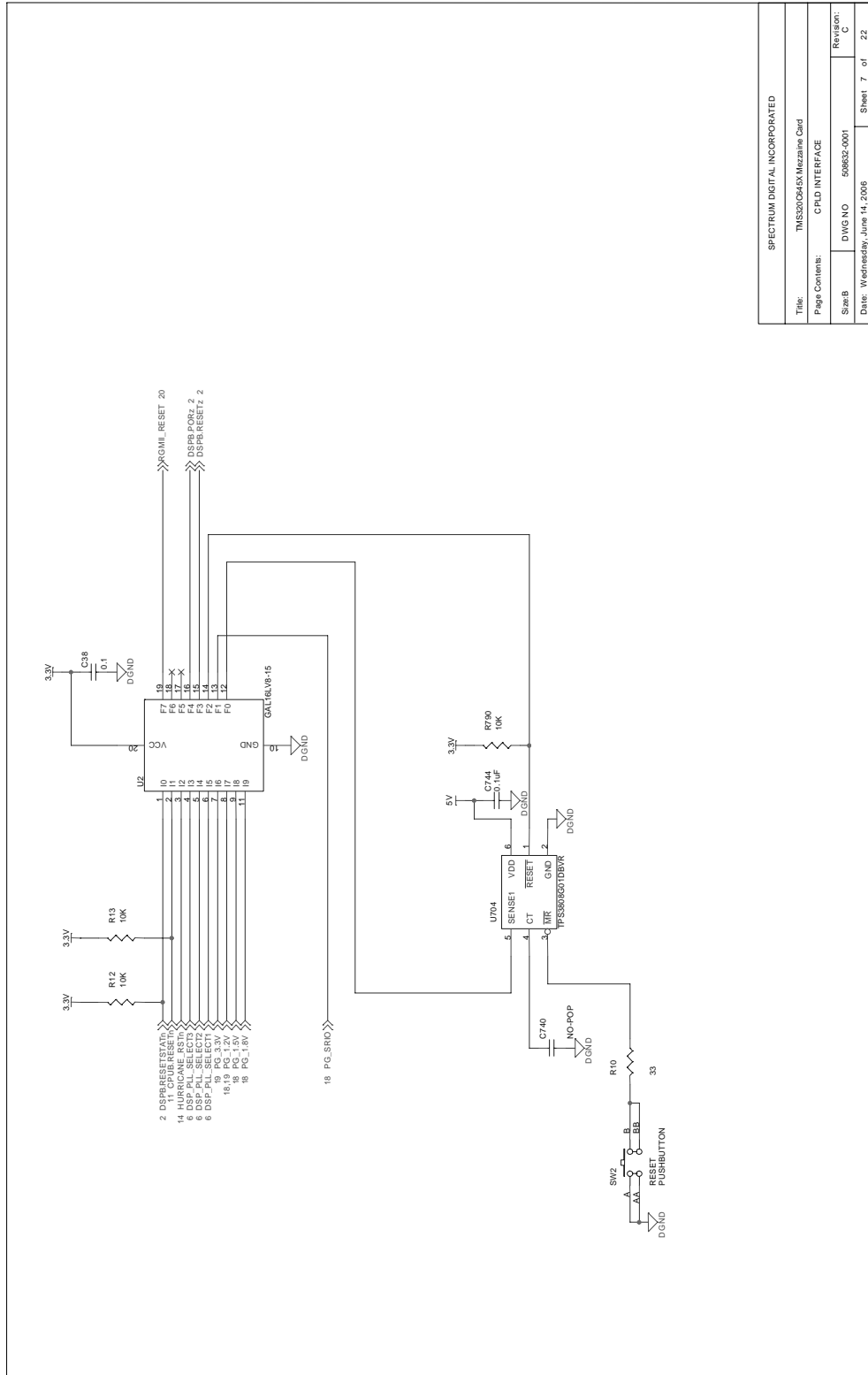
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Sheet:	DWG NO 501632-0001
Date:	Monday, June 26, 2006
	Sheet 3 of 22



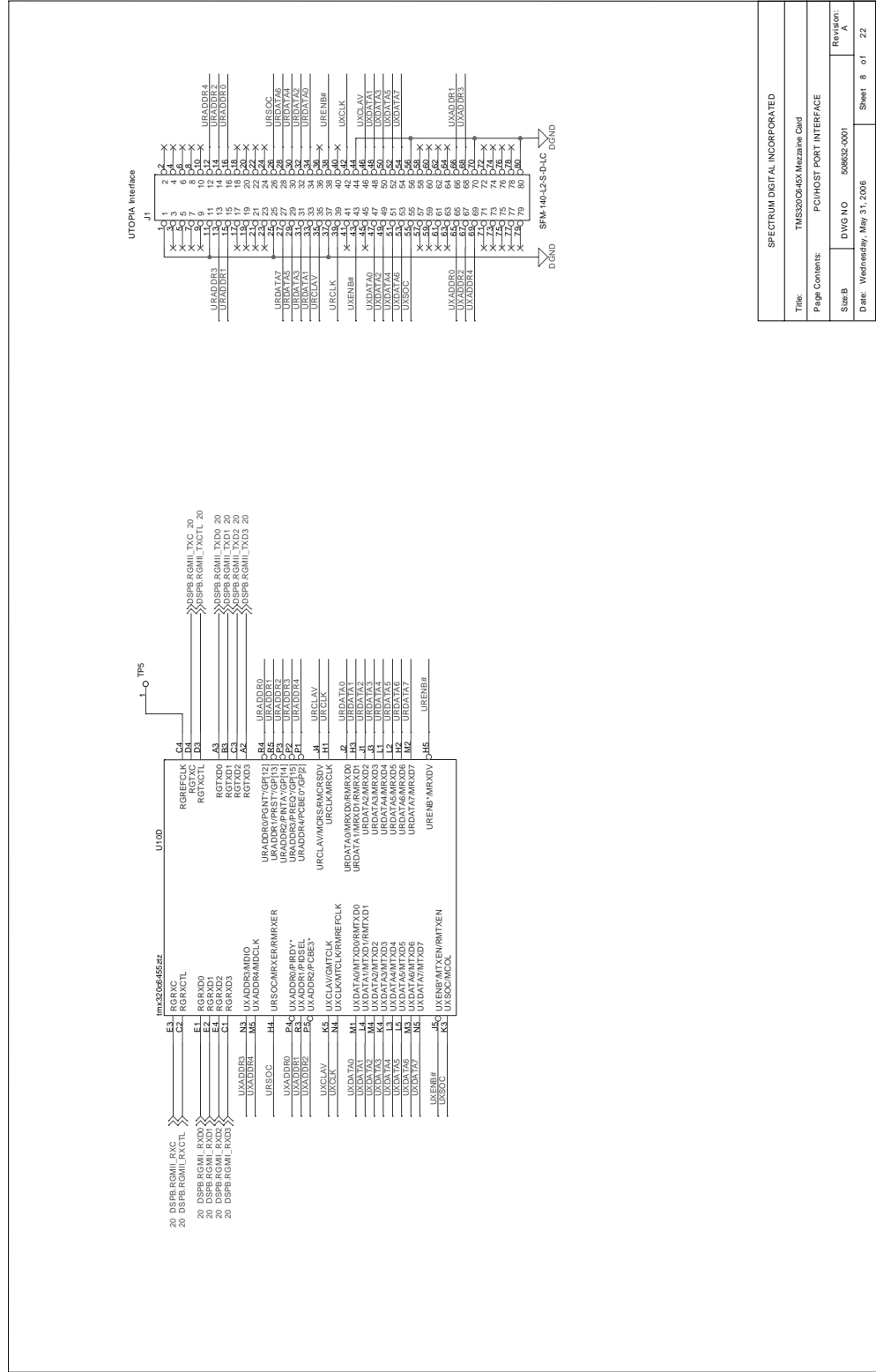
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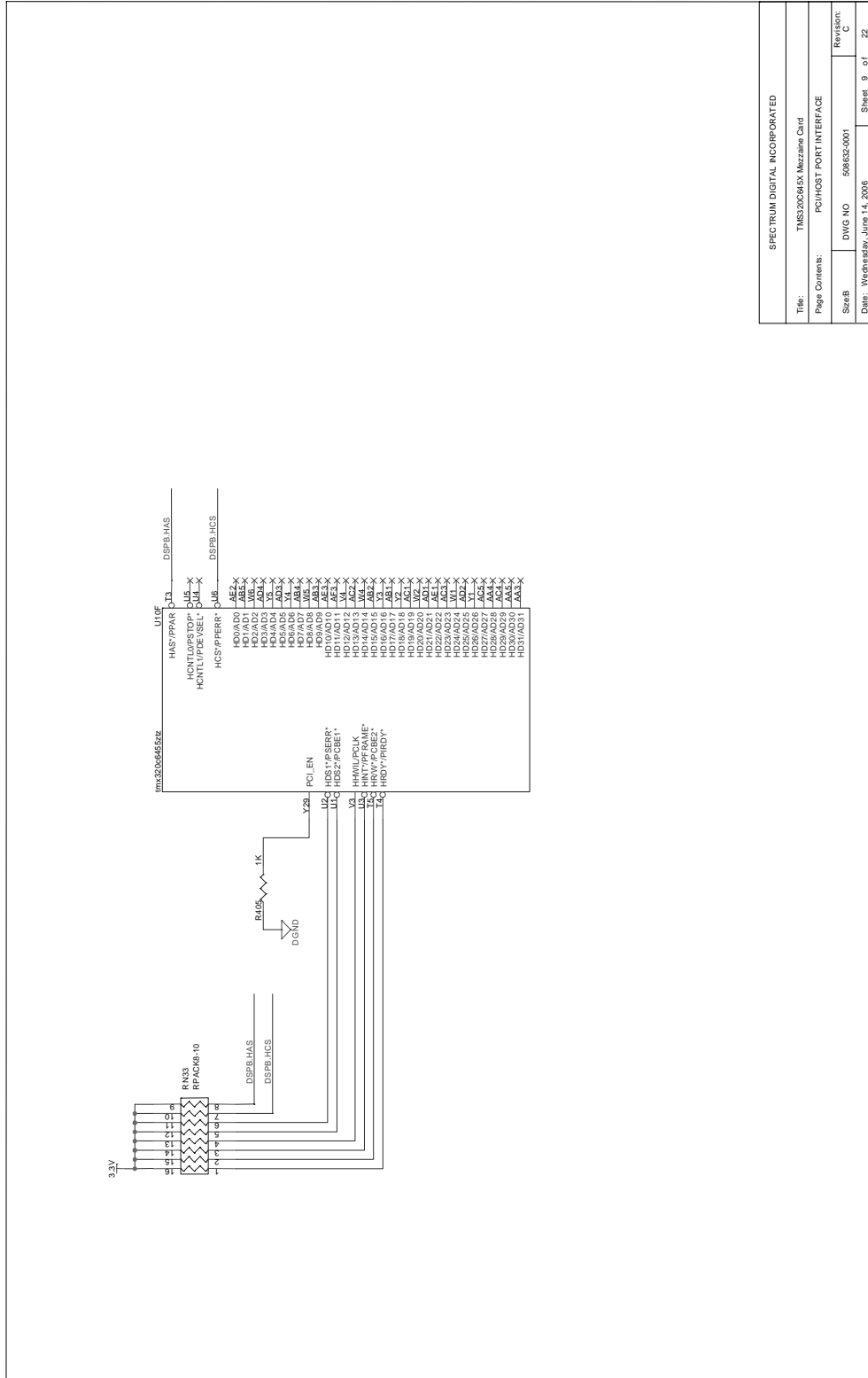
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Sheet:	DWG110 50852-0001
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Revision: A	
Sheet 5 of 22	



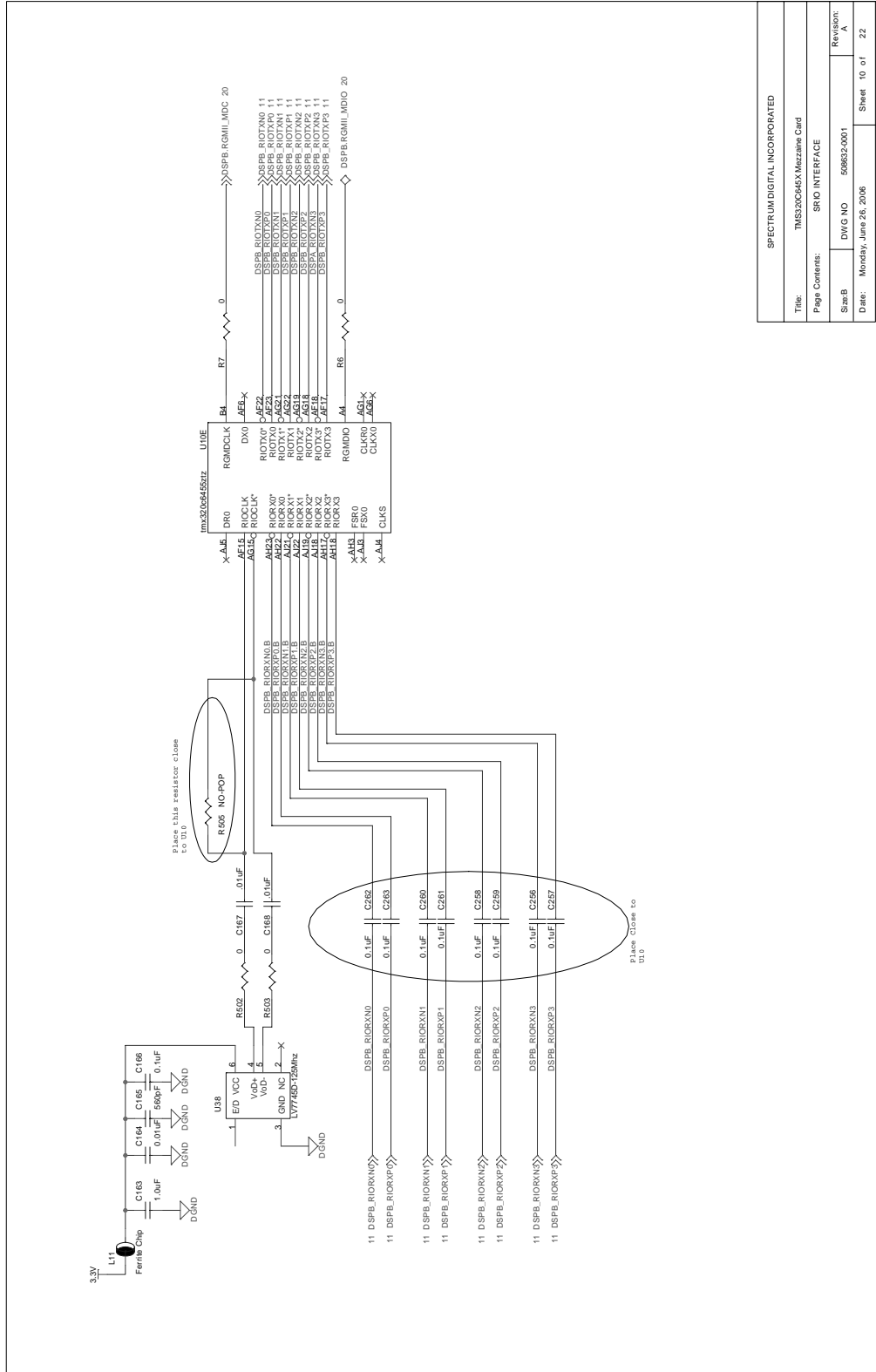
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Revision:	C
Sheet:	7 of 22



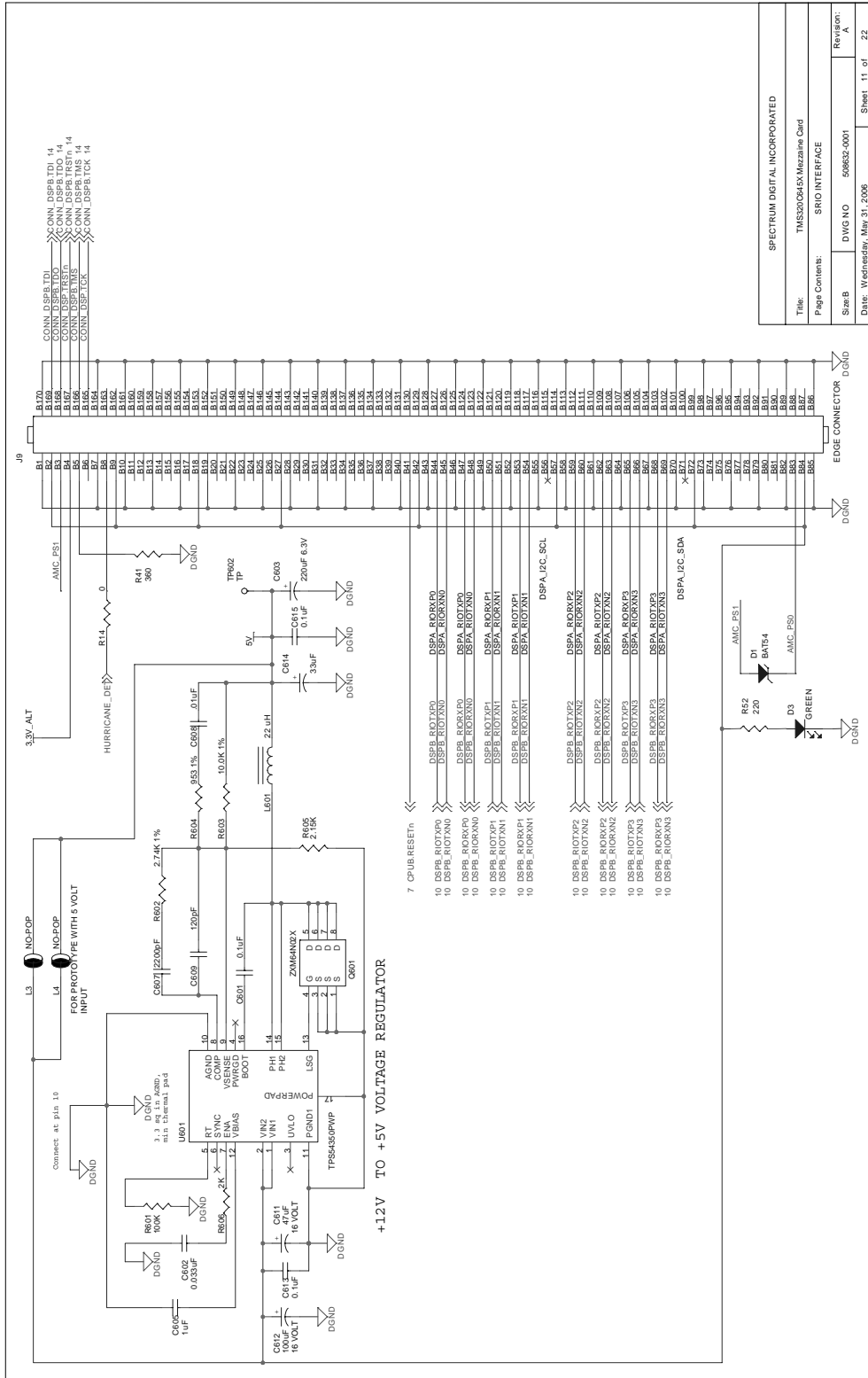
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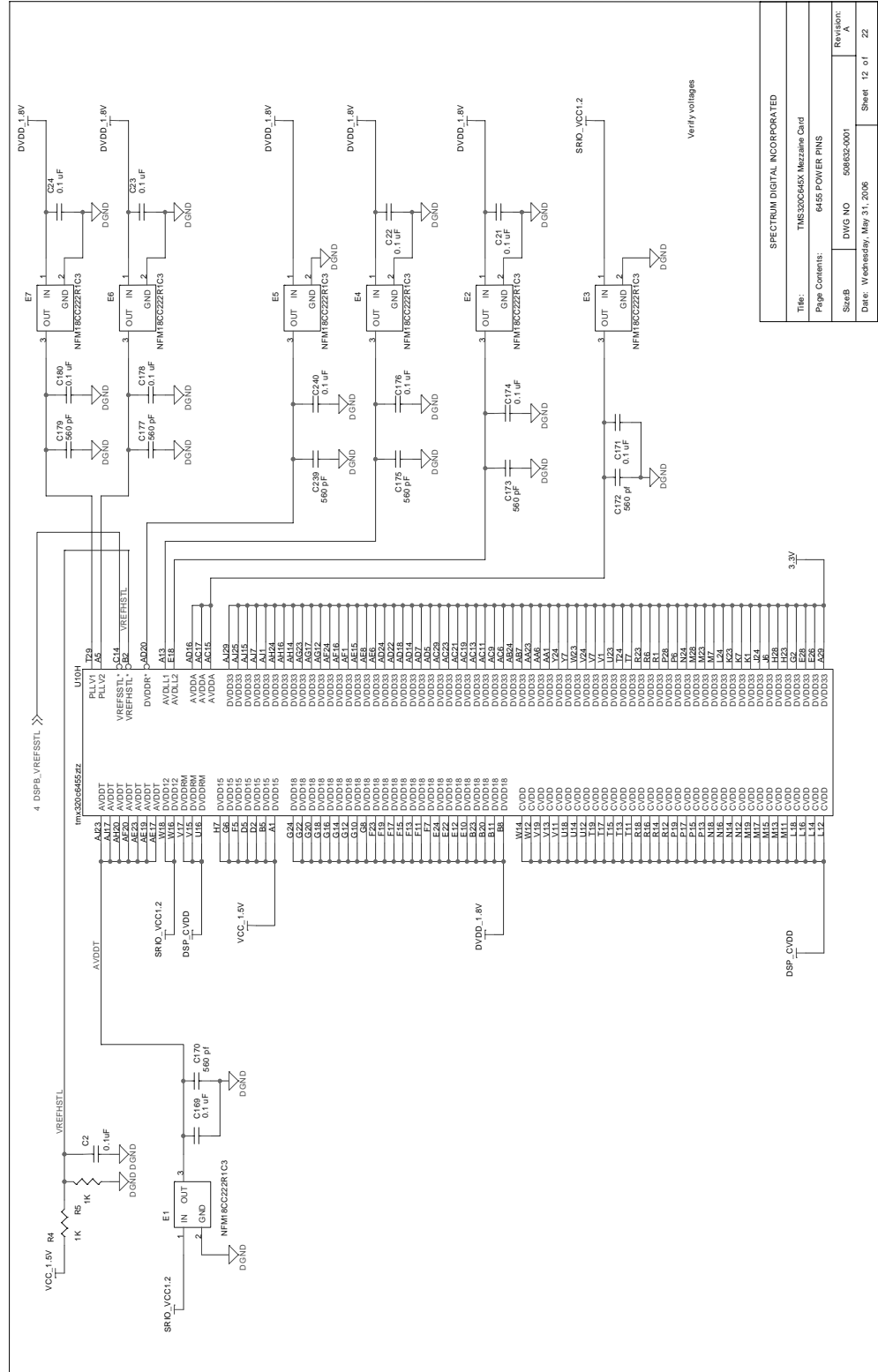
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Revision: C	
Date: Wednesday, June 14, 2006	Sheet 9 of 22



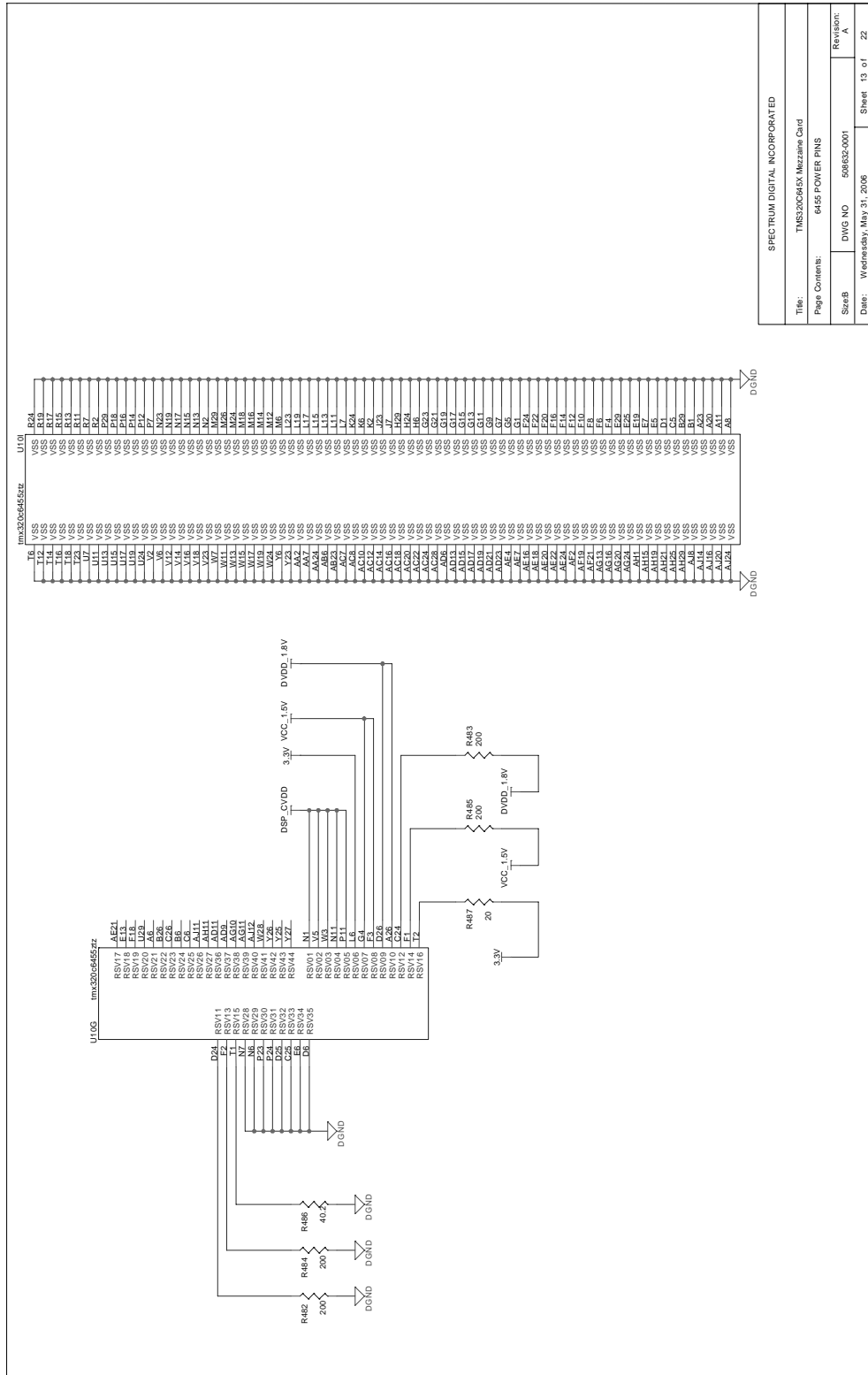
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Date:	Monday, June 26, 2006
Sheet:	10 of 22



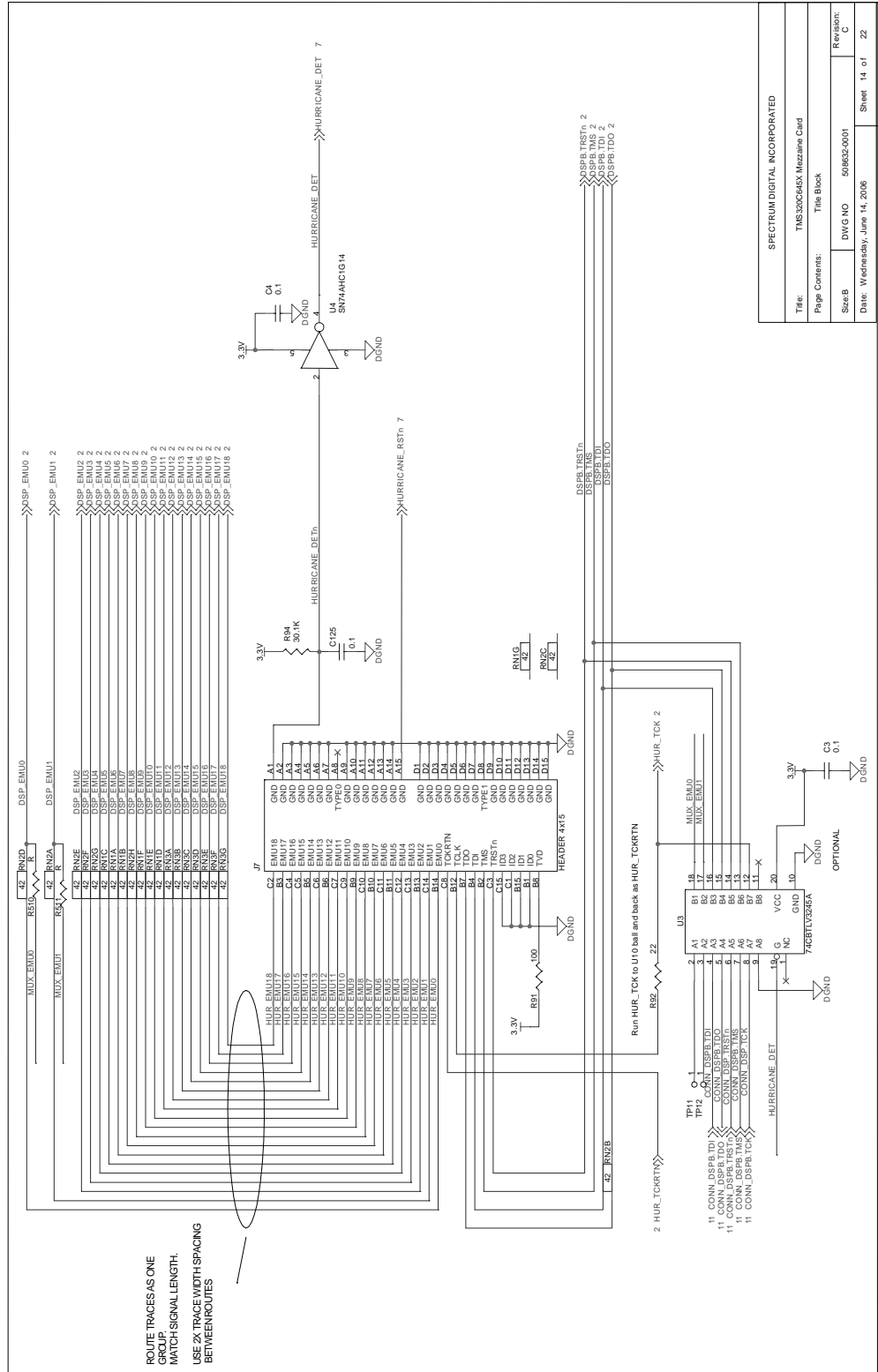
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Revision:	A
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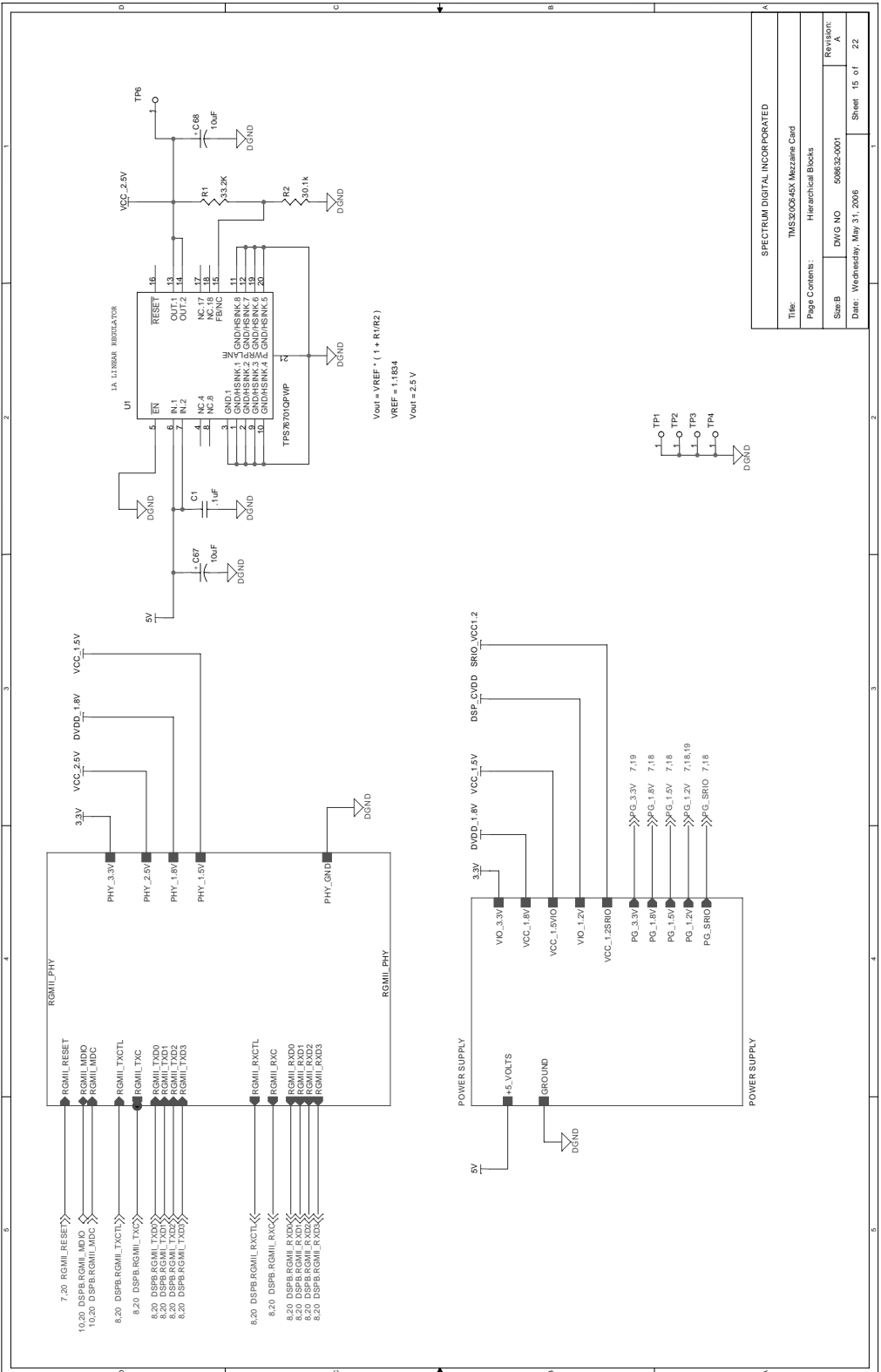
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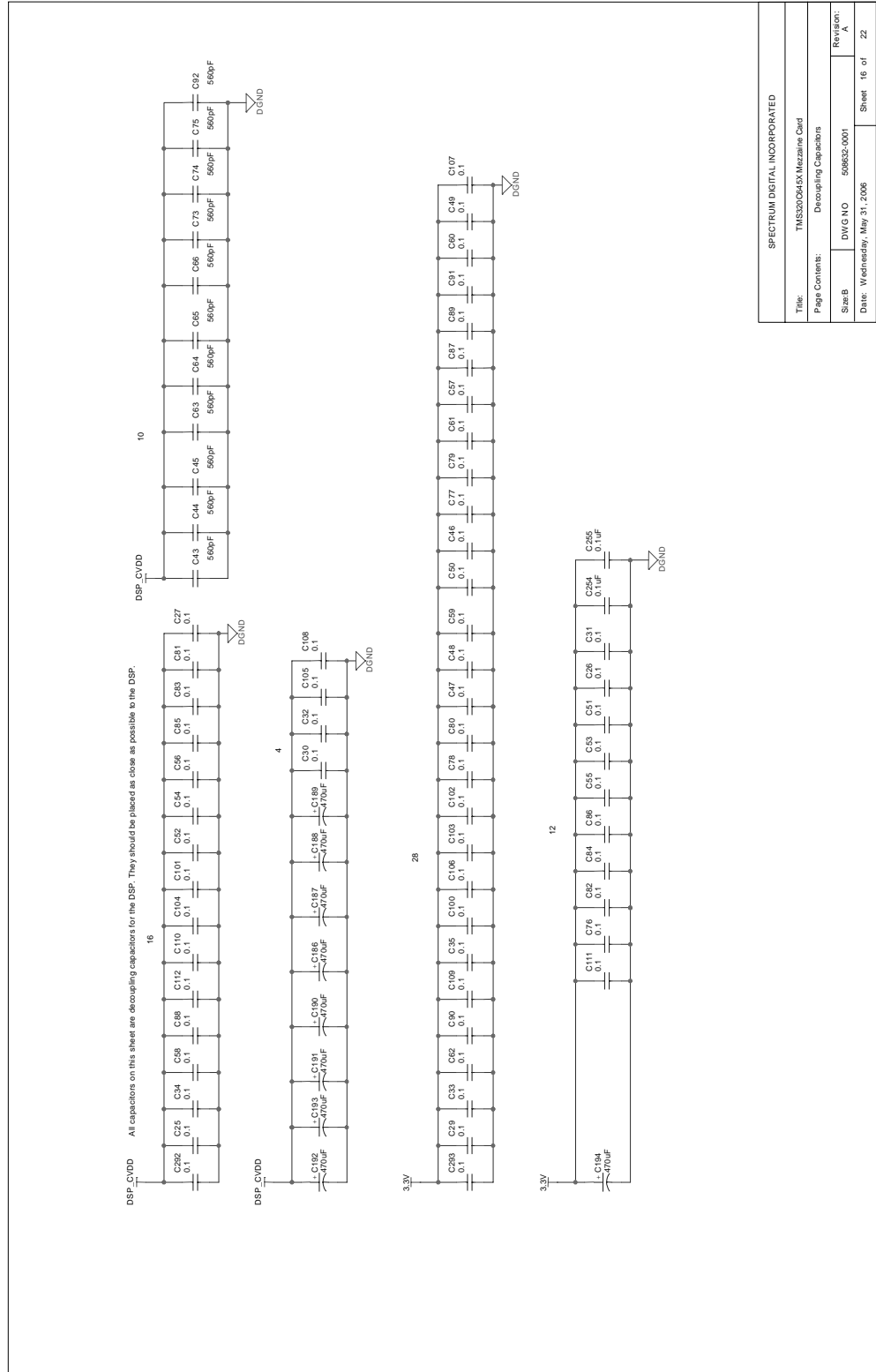


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Sheet 13 of 22	

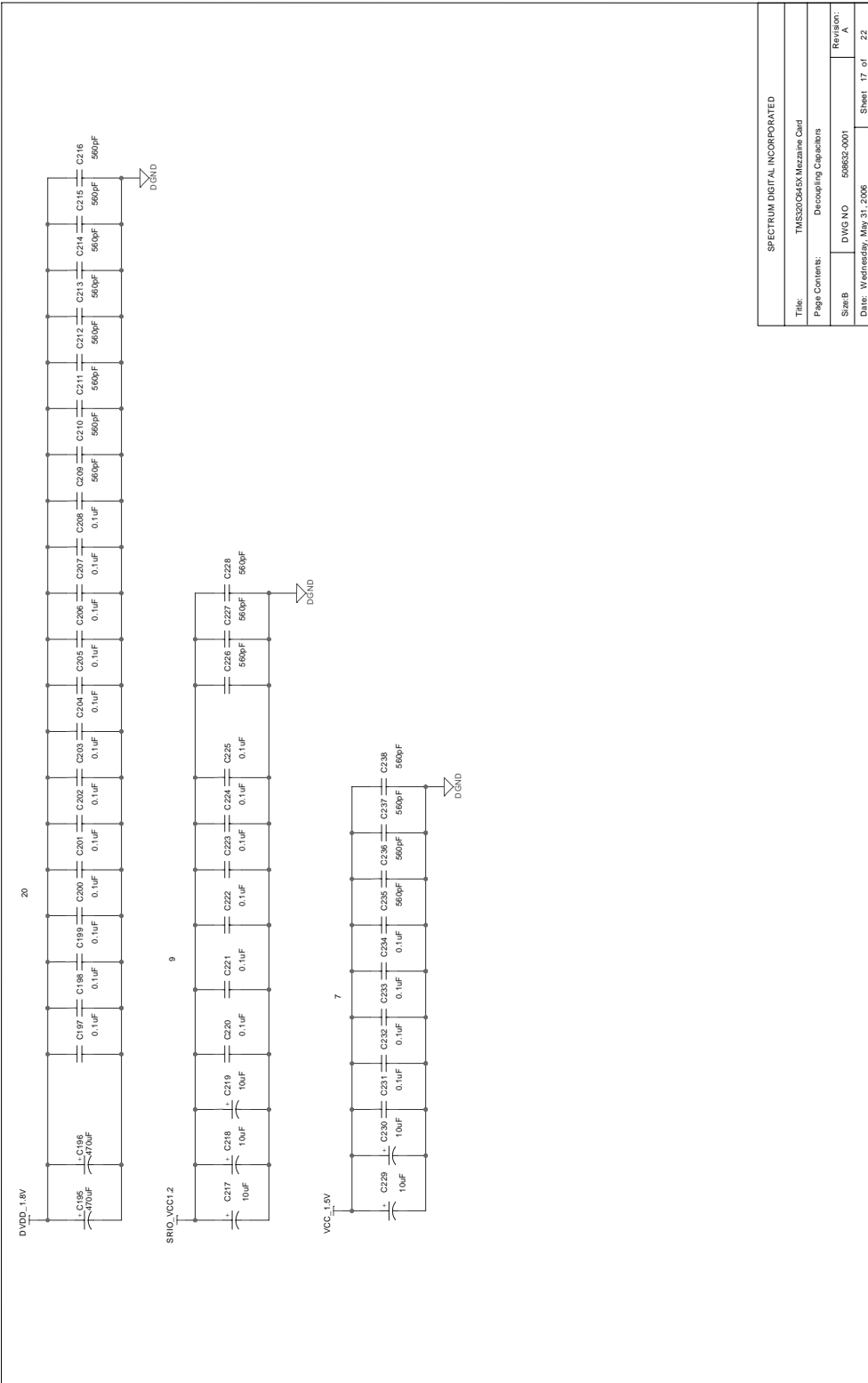


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Revision:	C
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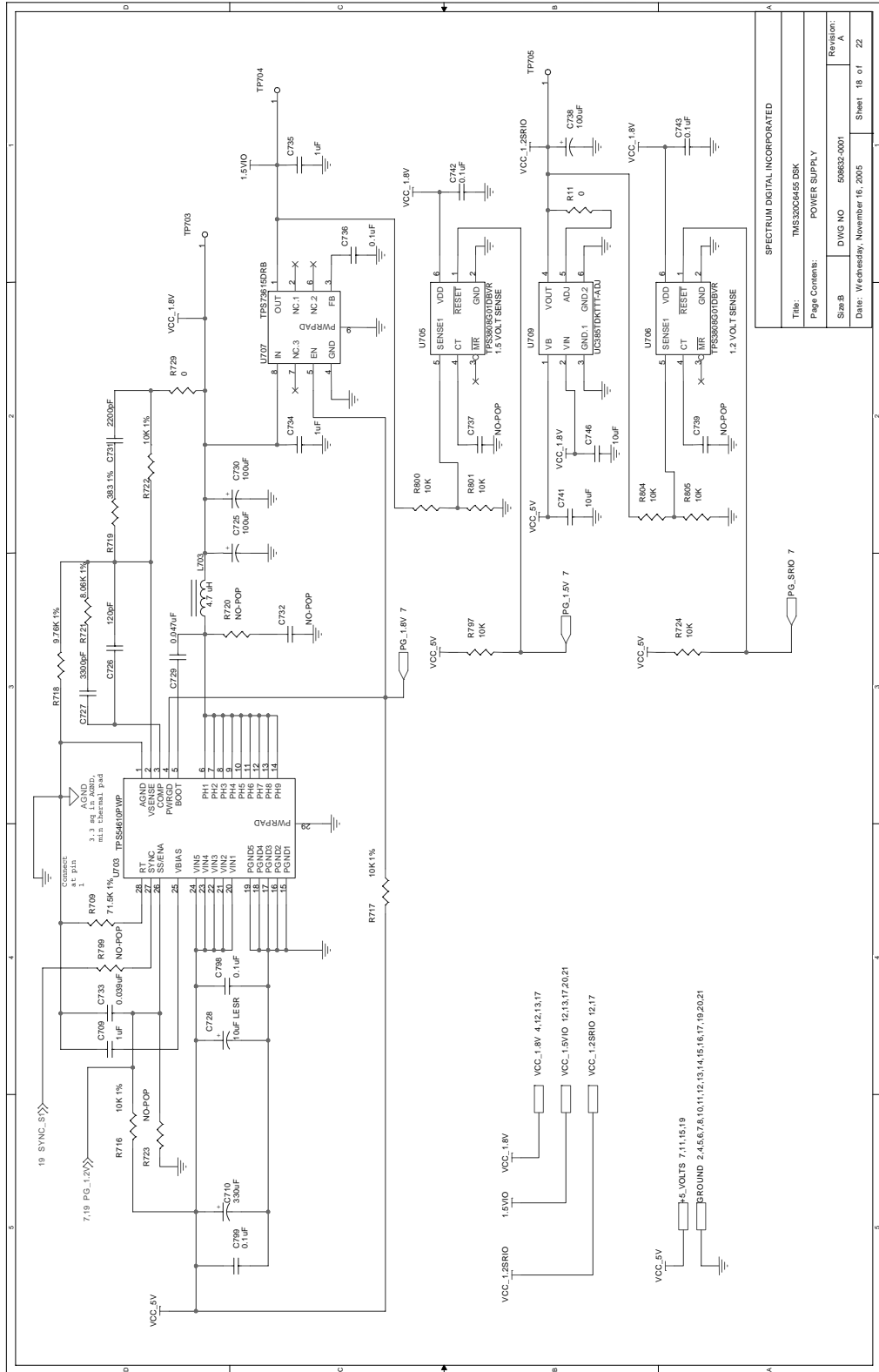




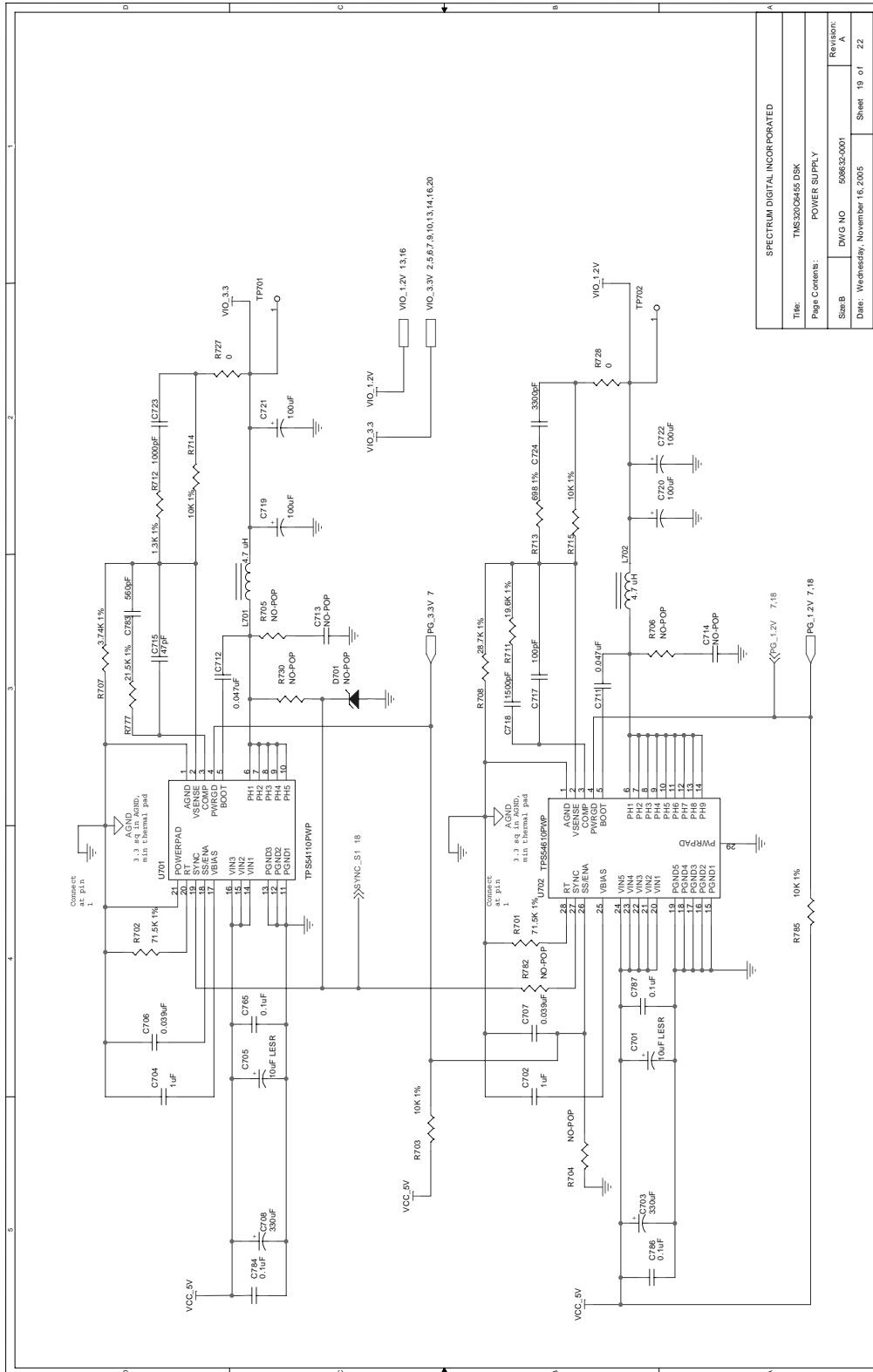
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Sheet:	16 of 22



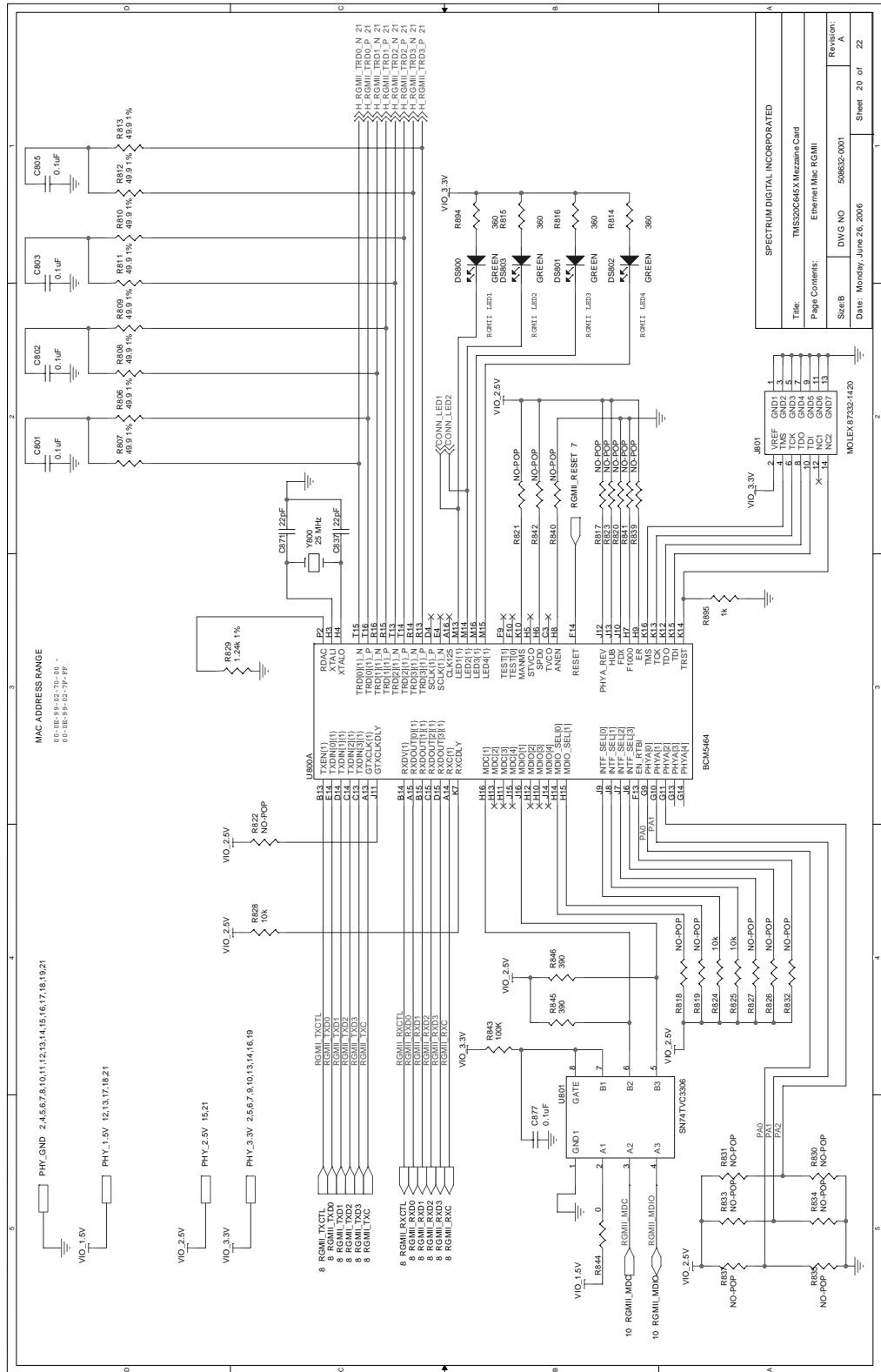
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Revision:	A
Sheet:	17 of 22



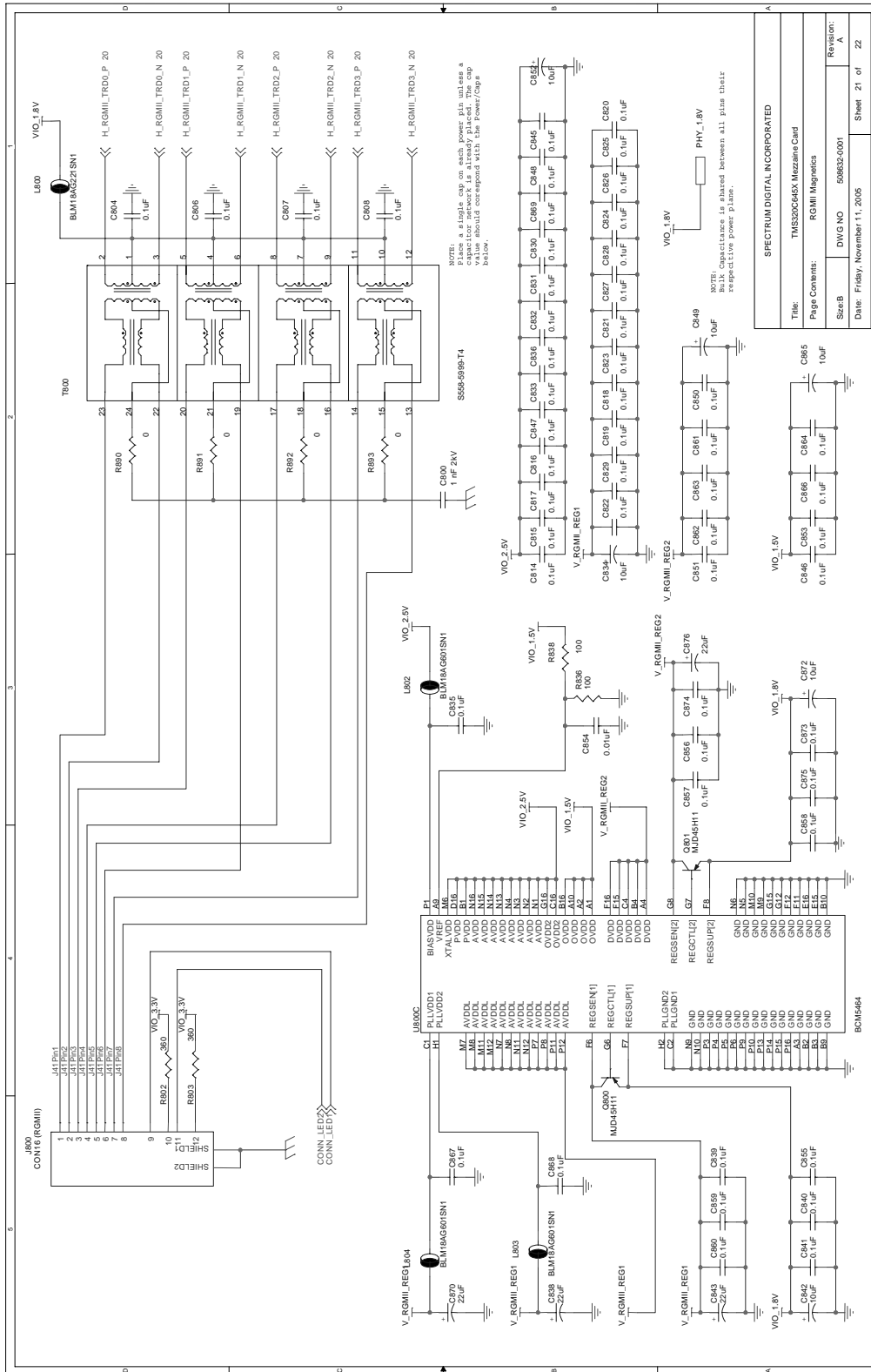
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Size B	DWG NO	58652-001	Revision:
			A
Date:	Wednesday, November 16, 2005		Sheet 18 of 22



SPECTRUM DIGITAL INCORPORATED	
Title:	TMS320C6455 DSK
Page Contents:	POWER SUPPLY
Size:	B
DWG NO:	506832-0001
Date:	Wednesday, November 16, 2005
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SPECTRUM DIGITAL INCORPORATED	
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Sheet:	DWG NO. 50652-0001
Date:	Monday, June 26, 2006
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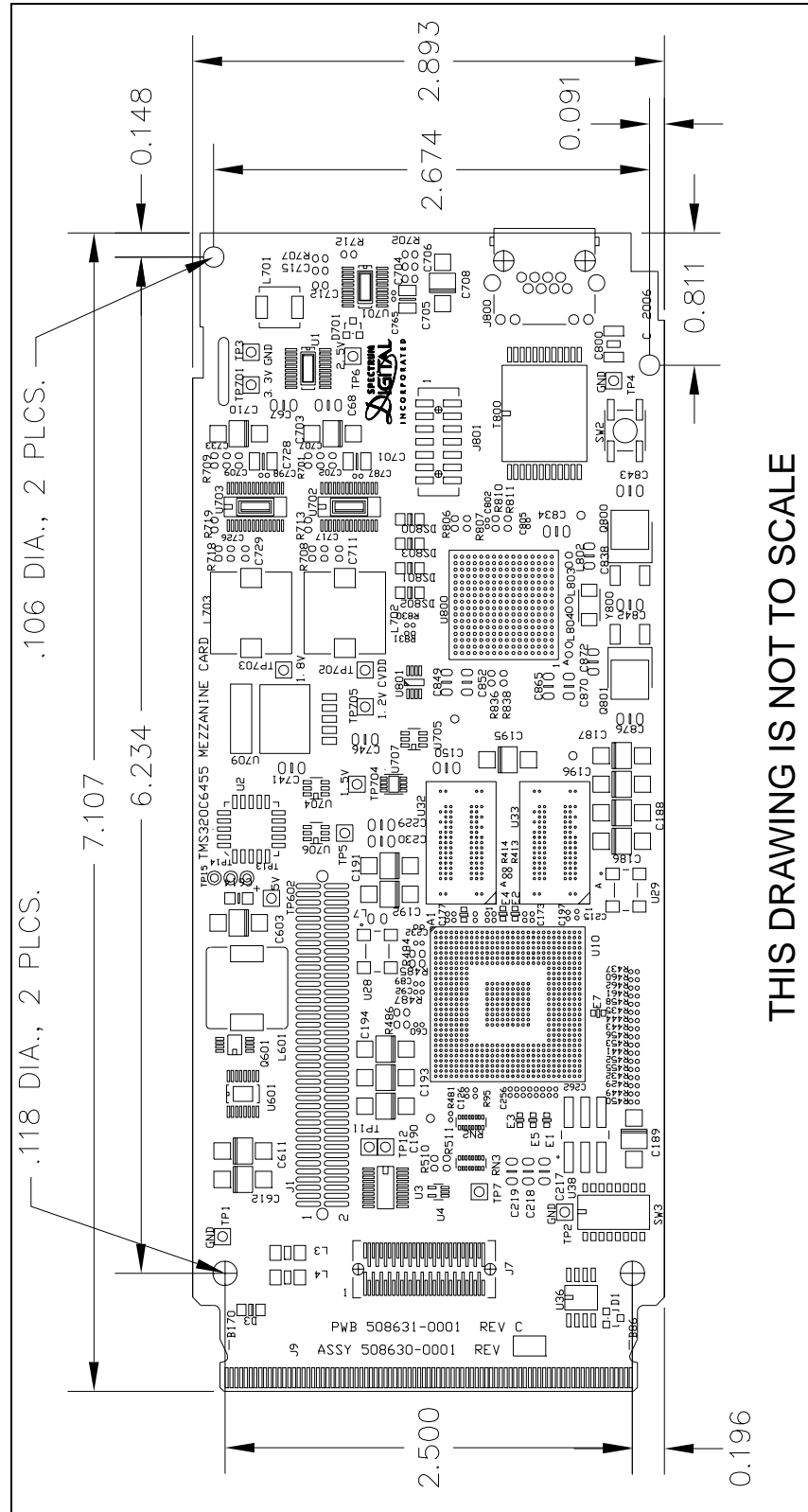


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Revision:	A
Sheet	21 of 22

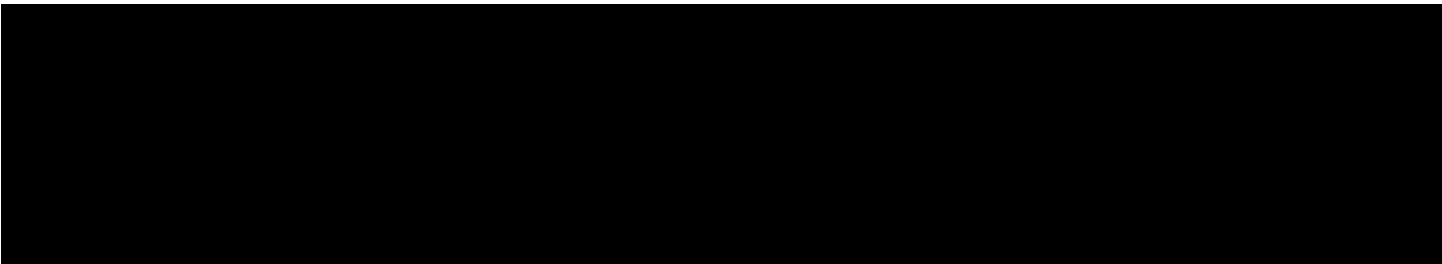
Appendix D

Mechanical Information

This appendix contains the mechanical information about the TMS320C6455 Mezzanine Board produced by Spectrum Digital.



THIS DRAWING IS NOT TO SCALE



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508635-0001 Rev. C