REV	DESCRIPTION	DATE	APPROVED
A	Initial schematic ready for layout - Alpha Release	09/15/05	RRP
B	Beta Release	10/15/05	RRP

NOTES, UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES IN OHMS.

2. CAPACTITANCE VALUES IN MICROFARADS.

3. REFERENCE DESIGNATORS USED:

4. ALL 0.1 uF AND 0.01uF CAPACITORS ARE DECOUPLING CAPS UNLESS OTHERWISE NOTED. THEY ARE SHOWN ON THE PAGE WITH THE INTEGRATED CIRCUITS THEY SHOULD BE PLACED NEAR.

5. OBSERVE THE FOLLOWING LAYOUT NOTES:

DDR2 ROUTING PER APPLICATION
SGMII ROUTING PER APPLICATION NOTE

6. BOARD PROPERTIES

A. ROUTE TO WITHIN 10% OF MANHATTAN DISTANCE
B. General layers 50 +/- 5 OHM MATCHED IMPEDANCE
C. OUTER LAYERS 0.5 OZ CU /W 0.5 OZ AU PLATING
D. INNER LAYERS 1.0 OZ CU
E. FR4 BOARD MATERIAL
F. MINIMUM TRACE WIDTH/SPACING 4 MILS
G. MINIMUM VIA SIZE 10/19 MIL
H. LAYER STACKUP:

SCHEMATIC CONTENTS:

REVISION STATUS OF SHEETS

REV	A	A	A	A	A	A	A	A	A			
SH	21	22	23	24	25	26	27	28	29			
REV	A	A	A	A	A	A	A	A	A	A		
SH	11	12	13	14	15	16	17	18	19	20		
REV	A	A	A	A	A	A	A	A	A	A	NEXT ASSY	USED ON
SH	1	2	3	4	5	6	7	8	9	10	APPLICATION	

DWN	R.R.P.	DATE AUG 01,2005
CHK	R.R.P.	DATE AUG 01,2005
ENGR	J.T.C.	DATE AUG 01,2005
ENGR-MGR	R.R.P.	DATE AUG 01,2005
QA	C.M.D.	DATE AUG 01,2005
MFG	C.M.D.	DATE AUG 01,2005
RLSE	T.M.K.	DATE AUG 01,2005

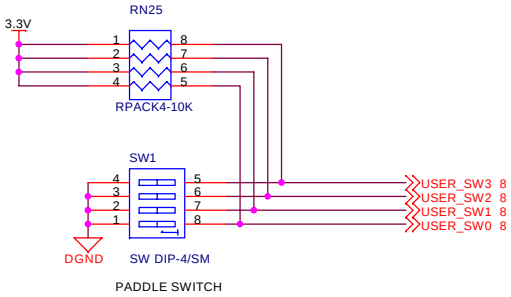
SPECTRUM DIGITAL INCORPORATED

Title: TMS320TCI6482 DSK

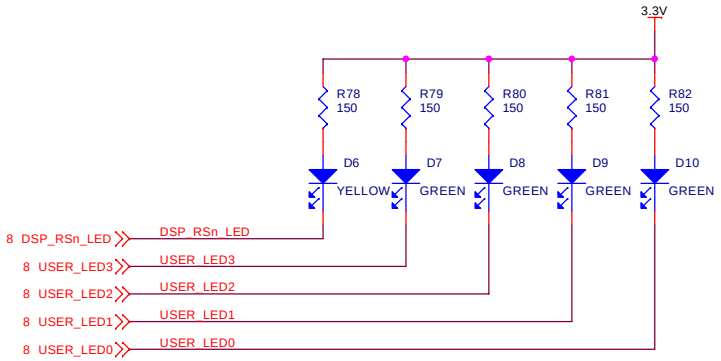
Page Contents: Title Block

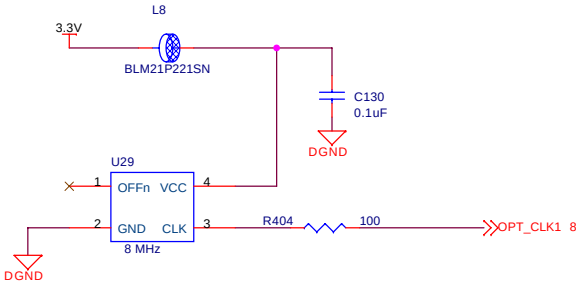
Size:B | DWG NO 508552-2001 | Revision: B

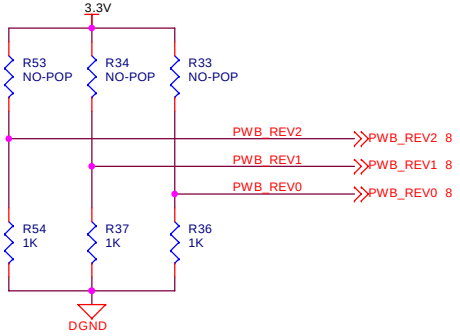
Date: Wednesday, April 12, 2006 | Sheet 1 of 34



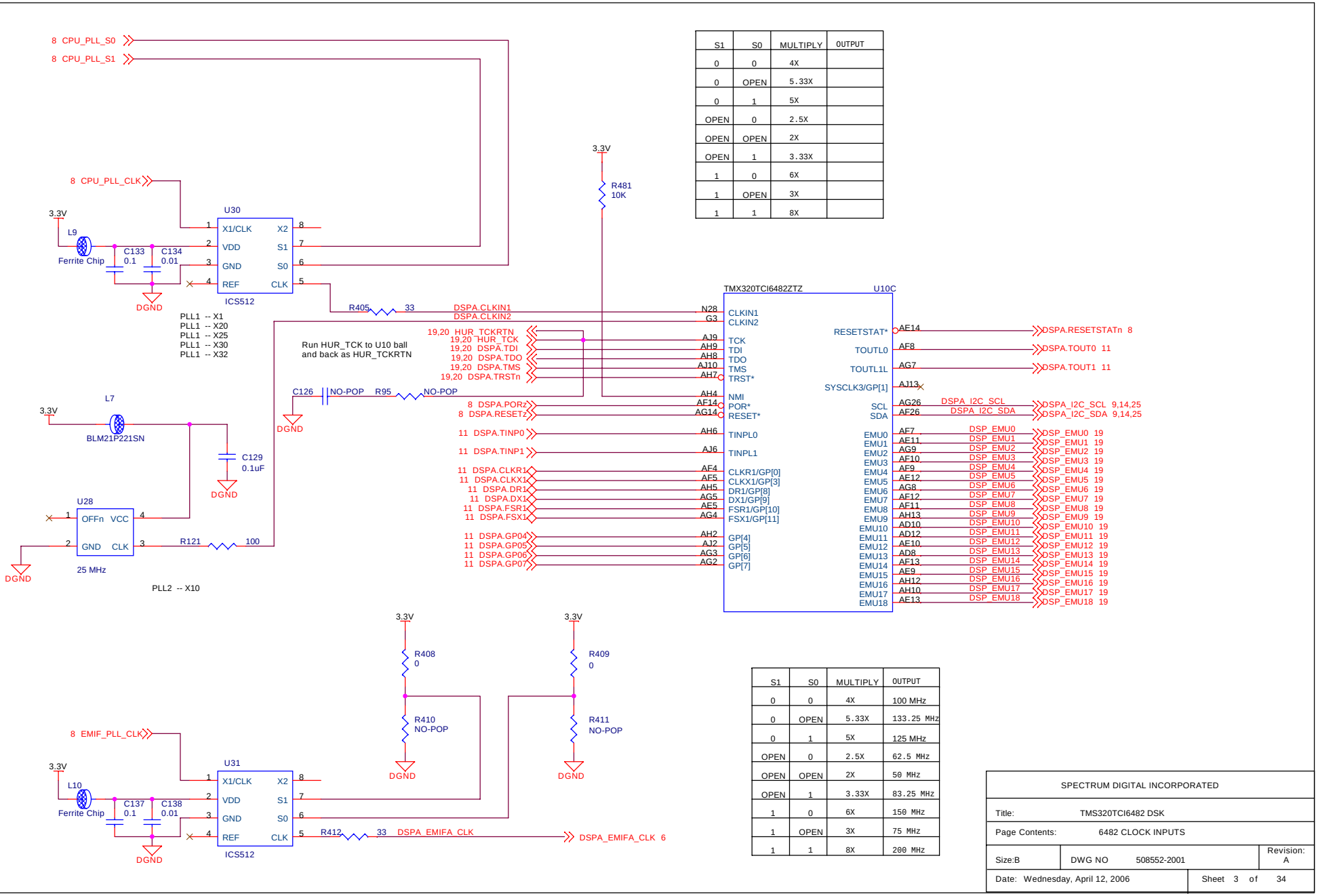
PADDLE SWITCH







SPECTRUM DIGITAL INCORPORATED		
Title: TMS320TCI6482 DSK		
Page Contents: Title Block		
Size:B	DWG NO 508552-2001	Revision: A
Date: Wednesday, April 12, 2006	Sheet 2 of 34	



S1	S0	MULTIPLY	OUTPUT
0	0	4X	
0	OPEN	5.33X	
0	1	5X	
OPEN	0	2.5X	
OPEN	OPEN	2X	
OPEN	1	3.33X	
1	0	6X	
1	OPEN	3X	
1	1	8X	

S1	S0	MULTIPLY	OUTPUT
0	0	4X	100 MHz
0	OPEN	5.33X	133.25 MHz
0	1	5X	125 MHz
OPEN	0	2.5X	62.5 MHz
OPEN	OPEN	2X	50 MHz
OPEN	1	3.33X	83.25 MHz
1	0	6X	150 MHz
1	OPEN	3X	75 MHz
1	1	8X	200 MHz

SPECTRUM DIGITAL INCORPORATED

Title: TMS320TCI6482 DSK

Page Contents: 6482 CLOCK INPUTS

Size:B | DWG NO 508552-2001 | Revision: A

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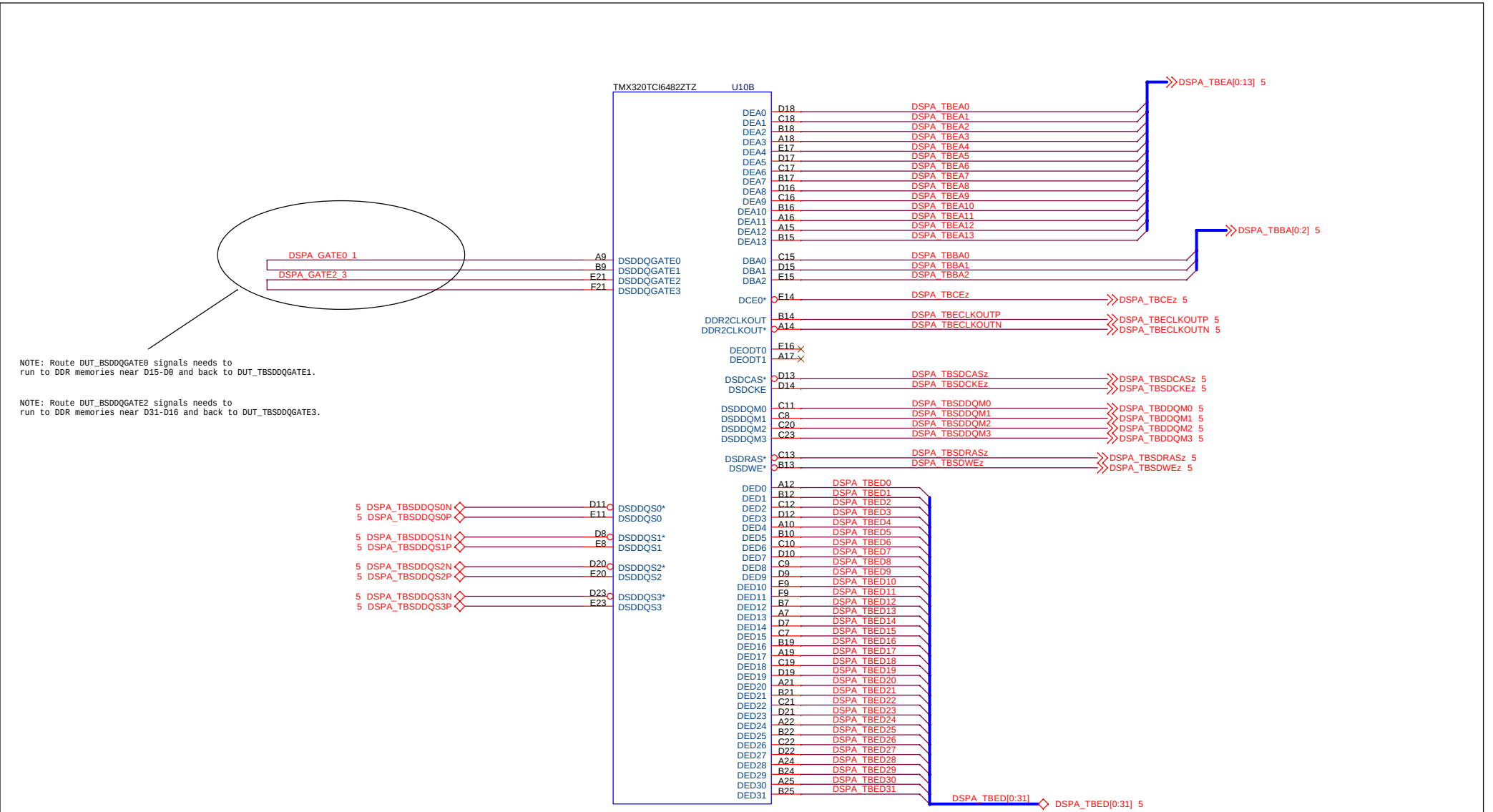
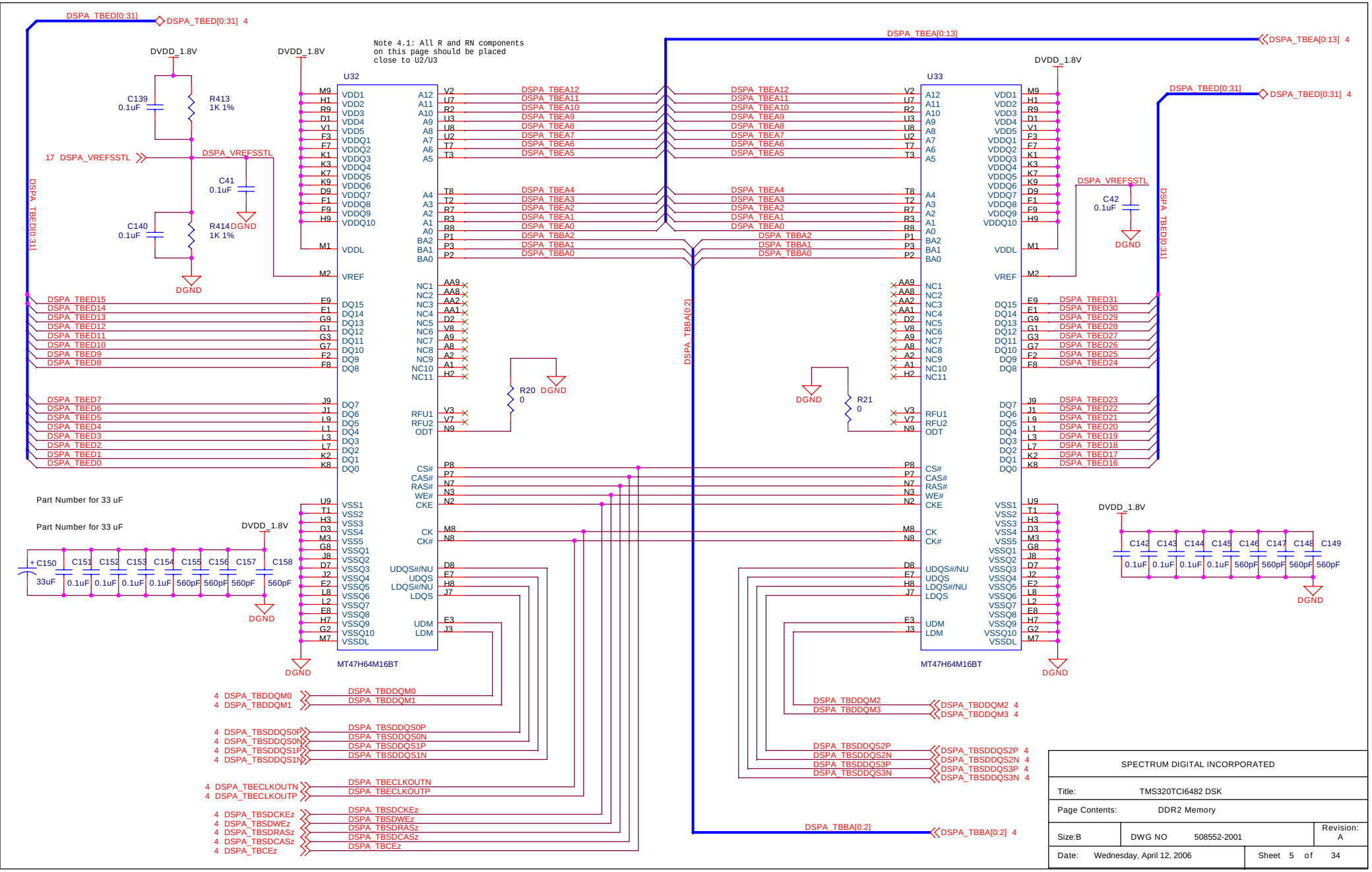


SPECTRUM DIGITAL INCORPORATED		
Title: TMS320TCI6482 DSK		
Page Contents: 6482 DDR Interface		
Size:B	DWG NO 508552-2001	Revision: A
Date: Wednesday, April 12, 2006	Sheet 4 of 34	


DSPA_TBED[0:31]
DSPA_TBED[0:31] 4
DVDD_1.8V
Note 4.1: All R and RN components on this page should be placed close to U2/U3
DSPA_TBEA[0:13]
DSPA_TBEA[0:13] 4
U32
U33
C139 0.1uF
R413 1K 1%
17 DSPA_VREFSSTL
DSPA_VREFSSTL
C41 0.1uF
C140 0.1uF
R414 1K 1%
DGND
C42 0.1uF
DSPA_TBED[0:31] 4
DSPA_TBBA[0:2]
R20 0
R21 0
DSPA_TBED15
DSPA_TBED14
DSPA_TBED13
DSPA_TBED12
DSPA_TBED11
DSPA_TBED10
DSPA_TBED9
DSPA_TBED8
DSPA_TBED7
DSPA_TBED6
DSPA_TBED5
DSPA_TBED4
DSPA_TBED3
DSPA_TBED2
DSPA_TBED1
DSPA_TBED0
DSPA_TBED31
DSPA_TBED30
DSPA_TBED29
DSPA_TBED28
DSPA_TBED27
DSPA_TBED26
DSPA_TBED25
DSPA_TBED24
DSPA_TBED23
DSPA_TBED22
DSPA_TBED21
DSPA_TBED20
DSPA_TBED19
DSPA_TBED18
DSPA_TBED17
DSPA_TBED16
Part Number for 33 uF
Part Number for 33 uF
C150 33uF
C151 0.1uF
C152 0.1uF
C153 0.1uF
C154 0.1uF
C155 560pF
C156 560pF
C157 560pF
C158 560pF
C142 0.1uF
C143 0.1uF
C144 0.1uF
C145 0.1uF
C146 560pF
C147 560pF
C148 560pF
C149 560pF
MT47H64M16BT
MT47H64M16BT
DSPA_TBDDQM0
DSPA_TBDDQM1
DSPA_TBDDQM2
DSPA_TBDDQM3
DSPA_TBSDDQS0P
DSPA_TBSDDQS0N
DSPA_TBSDDQS1P
DSPA_TBSDDQS1N
DSPA_TBSDDQS2P
DSPA_TBSDDQS2N
DSPA_TBSDDQS3P
DSPA_TBSDDQS3N
DSPA_TBECLKOUTN
DSPA_TBECLKOUTP
DSPA_TBSDCKEz
DSPA_TBSDWEz
DSPA_TBSDRASz
DSPA_TBSDCASz
DSPA_TBCEz
SPECTRUM DIGITAL INCORPORATED
Title: TMS320TCI6482 DSK
Page Contents: DDR2 Memory
Size:B
DWG NO 508552-2001
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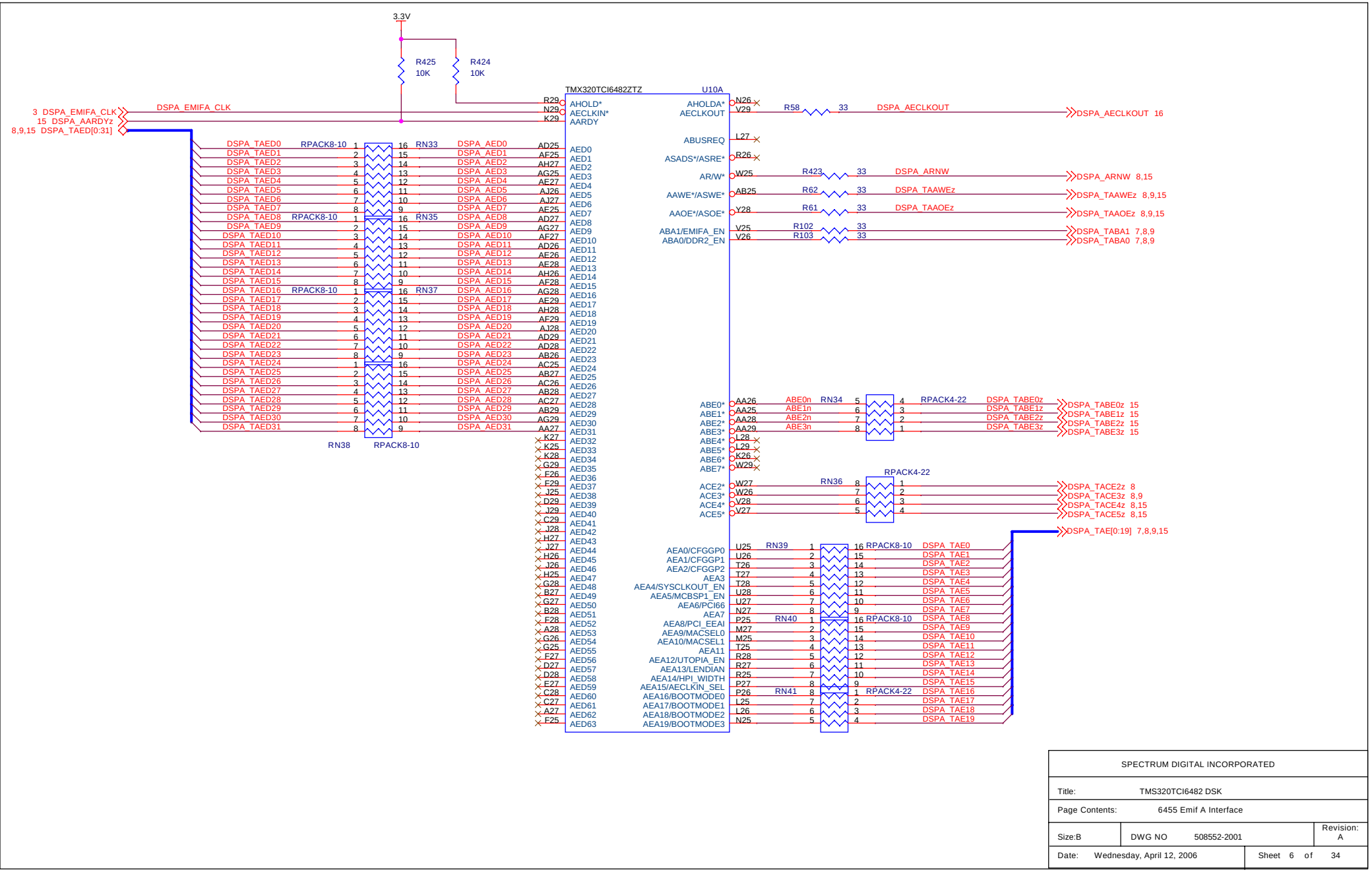
3.3V
R425
10K
R424
10K
TMX320TCI6482ZTZ
U10A
3 DSPA_EMIFA_CLK
15 DSPA_AARDYz
8,9,15 DSPA_TAED[0:31]
DSPA_EMIFA_CLK
R29 AHOLD*
N29 AECLKIN*
K29 AARDY
AHOLDA* N26
AECLKOUT V29
R58 33 DSPA_AECLKOUT
DSPA_AECLKOUT 16
ABUSREQ L27
ASADS*/ASRE* R26
AR/W* W25
R423 33 DSPA_ARNW
DSPA_ARNW 8,15
AAWE*/ASWE* AB25
R62 33 DSPA_TAAWEz
DSPA_TAAWEz 8,9,15
AAOE*/ASOE* Y28
R61 33 DSPA_TAAOEz
DSPA_TAAOEz 8,9,15
ABA1/EMIFA_EN V25
ABA0/DDR2_EN V26
R102 33
R103 33
DSPA_TABA1 7,8,9
DSPA_TABA0 7,8,9
RPACK8-10
RN33
RN35
RN37
RN38
DSPA_TAED0
DSPA_TAED1
DSPA_TAED2
DSPA_TAED3
DSPA_TAED4
DSPA_TAED5
DSPA_TAED6
DSPA_TAED7
DSPA_TAED8
DSPA_TAED9
DSPA_TAED10
DSPA_TAED11
DSPA_TAED12
DSPA_TAED13
DSPA_TAED14
DSPA_TAED15
DSPA_TAED16
DSPA_TAED17
DSPA_TAED18
DSPA_TAED19
DSPA_TAED20
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DSPA_TAED24
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DSPA_TAED26
DSPA_TAED27
DSPA_TAED28
DSPA_TAED29
DSPA_TAED30
DSPA_TAED31
DSPA_AED0 AD25
DSPA_AED1 AF25
DSPA_AED2 AH27
DSPA_AED3 AG25
DSPA_AED4 AE27
DSPA_AED5 AJ26
DSPA_AED6 AJ27
DSPA_AED7 AE25
DSPA_AED8 AD27
DSPA_AED9 AG27
DSPA_AED10 AF27
DSPA_AED11 AD26
DSPA_AED12 AE26
DSPA_AED13 AE28
DSPA_AED14 AH26
DSPA_AED15 AF28
DSPA_AED16 AG28
DSPA_AED17 AE29
DSPA_AED18 AH28
DSPA_AED19 AF29
DSPA_AED20 AJ28
DSPA_AED21 AD29
DSPA_AED22 AD28
DSPA_AED23 AB26
DSPA_AED24 AC25
DSPA_AED25 AB27
DSPA_AED26 AC26
DSPA_AED27 AB28
DSPA_AED28 AC27
DSPA_AED29 AB29
DSPA_AED30 AG29
DSPA_AED31 AA27
AED0
AED1
AED2
AED3
AED4
AED5
AED6
AED7
AED8
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AED10
AED11
AED12
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K25
K28
G29
F26
F29
J25
D29
J29
C29
J28
H27
J27
H26
J26
H25
G28
B27
G27
B28
F28
A28
G26
G25
F27
D27
D28
E27
C28
C27
A27
F25
ABE0* AA26
ABE1* AA25
ABE2* AA28
ABE3* AA29
ABE4* L28
ABE5* L29
ABE6* K26
ABE7* W29
ABE0n
ABE1n
ABE2n
ABE3n
RN34
RPACK4-22
DSPA_TABE0z
DSPA_TABE1z
DSPA_TABE2z
DSPA_TABE3z
DSPA_TABE0z 15
DSPA_TABE1z 15
DSPA_TABE2z 15
DSPA_TABE3z 15
ACE2* W27
ACE3* W26
ACE4* V28
ACE5* V27
RN36
DSPA_TACE2z 8
DSPA_TACE3z 8,9
DSPA_TACE4z 8,15
DSPA_TACE5z 8,15
DSPA_TAE[0:19] 7,8,9,15
AEA0/CFGGP0 U25
AEA1/CFGGP1 U26
AEA2/CFGGP2 T26
AEA3 T27
AEA4/SYSCLKOUT_EN T28
AEA5/MCBSP1_EN U28
AEA6/PCI66 U27
AEA7 N27
AEA8/PCI_EEAI P25
AEA9/MACSEL0 M27
AEA10/MACSEL1 M25
AEA11 T25
AEA12/UTOPIA_EN R28
AEA13/LENDIAN R27
AEA14/HPI_WIDTH R25
AEA15/AECLKIN_SEL P27
AEA16/BOOTMODE0 P26
AEA17/BOOTMODE1 L25
AEA18/BOOTMODE2 L26
AEA19/BOOTMODE3 N25
RN39
RN40
RN41
RPACK8-10
RPACK4-22
DSPA_TAE0
DSPA_TAE1
DSPA_TAE2
DSPA_TAE3
DSPA_TAE4
DSPA_TAE5
DSPA_TAE6
DSPA_TAE7
DSPA_TAE8
DSPA_TAE9
DSPA_TAE10
DSPA_TAE11
DSPA_TAE12
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DSPA_TAE14
DSPA_TAE15
DSPA_TAE16
DSPA_TAE17
DSPA_TAE18
DSPA_TAE19
SPECTRUM DIGITAL INCORPORATED
Title: TMS320TCI6482 DSK
Page Contents: 6455 Emif A Interface
Size:B
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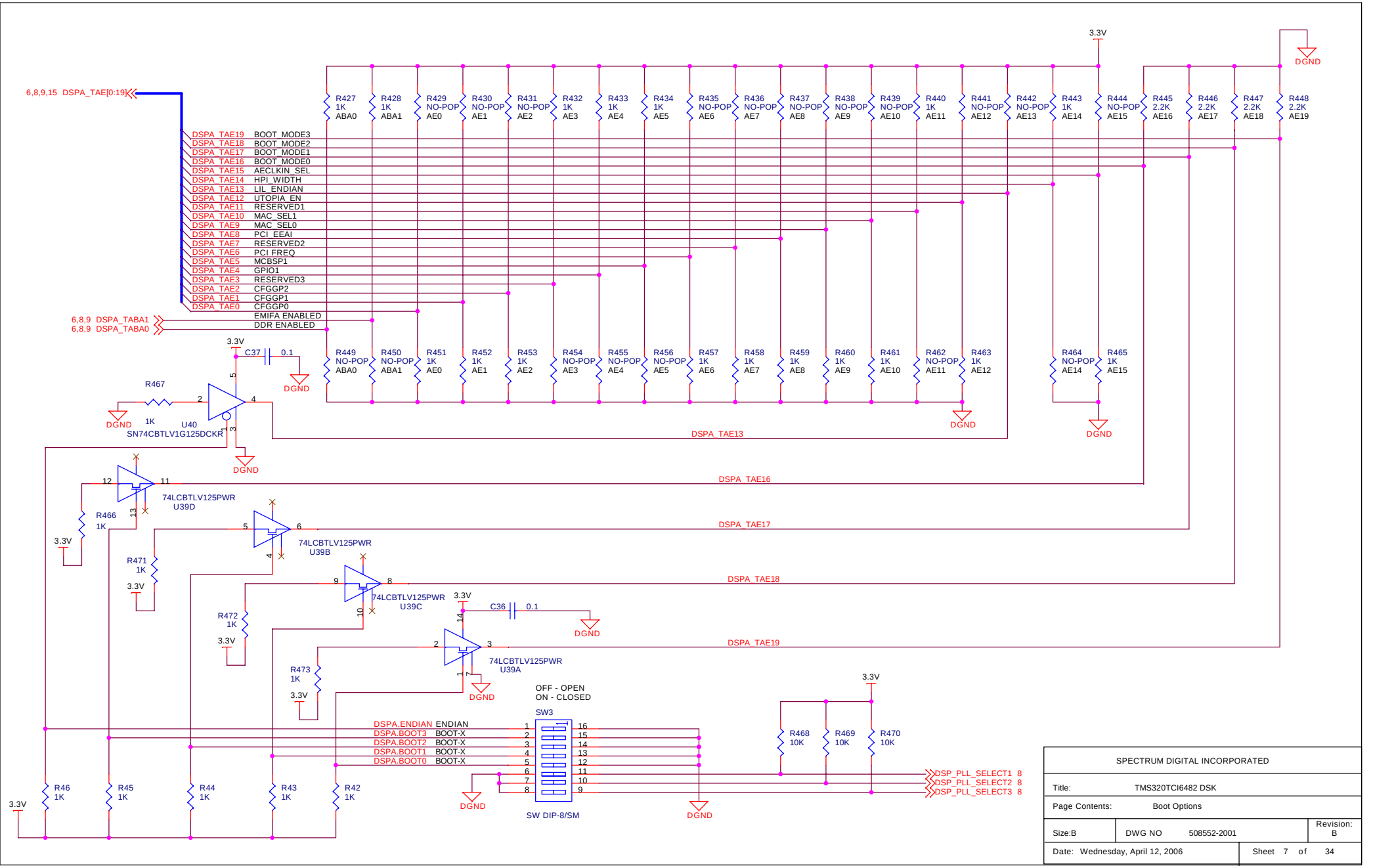

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Size:B	DWG NO 508552-2001	Revision: B
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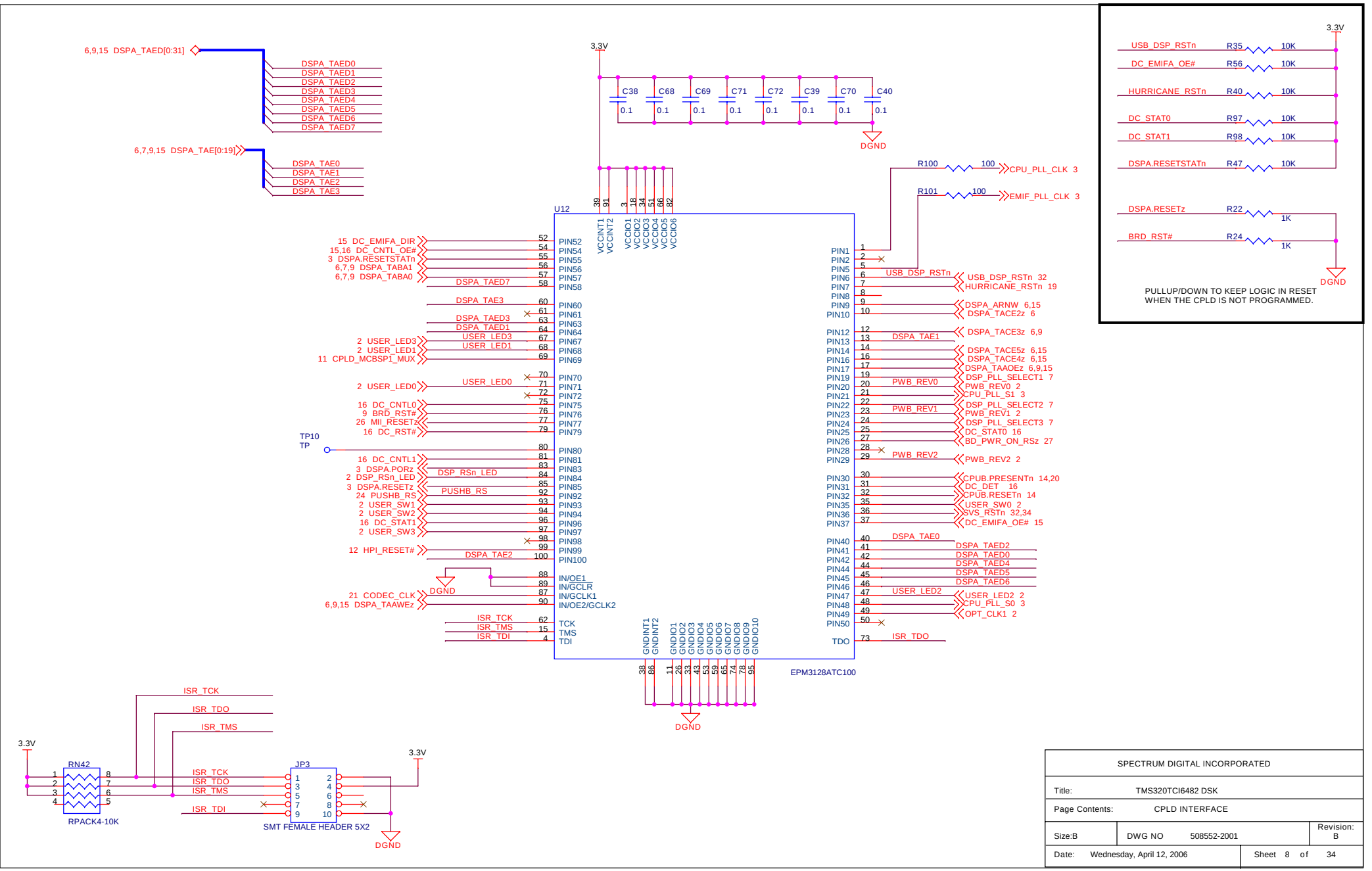

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Page Contents: CPLD INTERFACE		
Size:B	DWG NO 508552-2001	Revision: B
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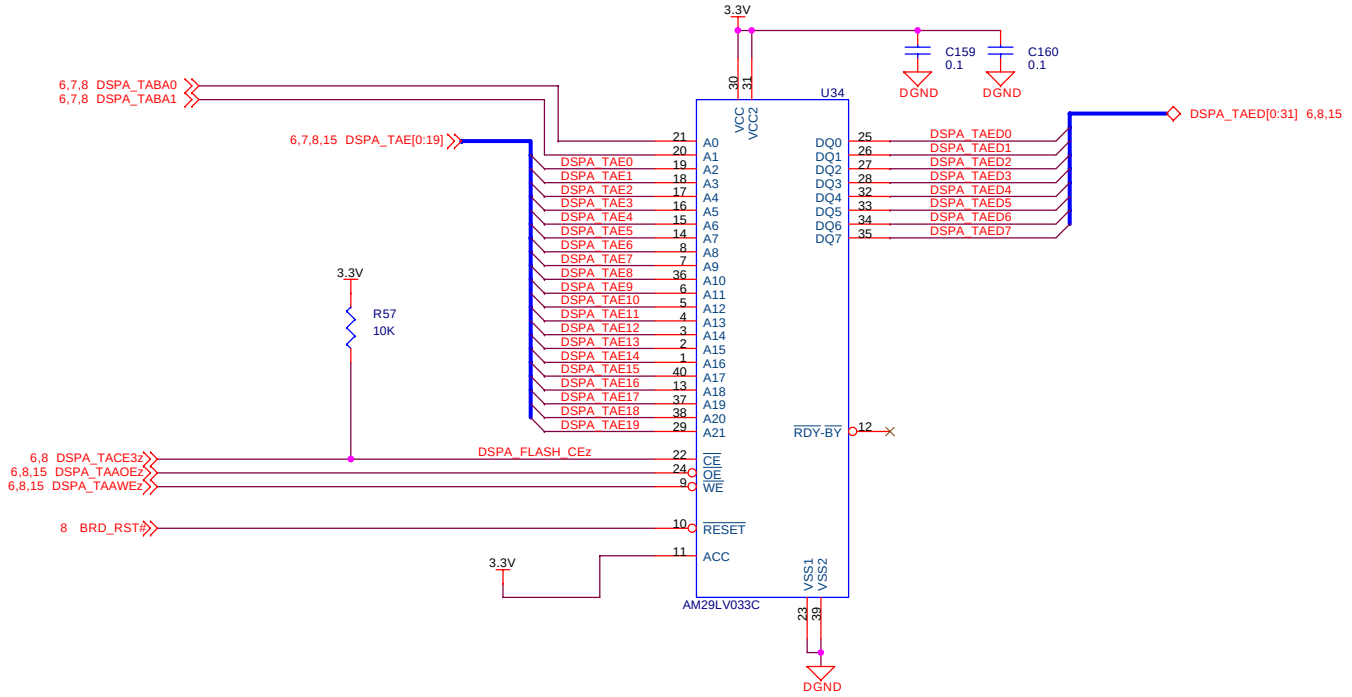

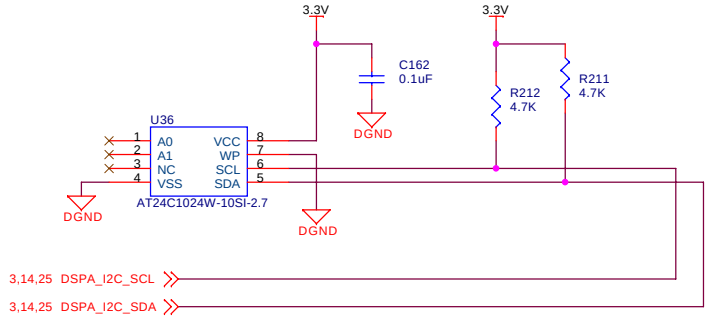

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Size:B	DWG NO 508552-2001	Revision: A
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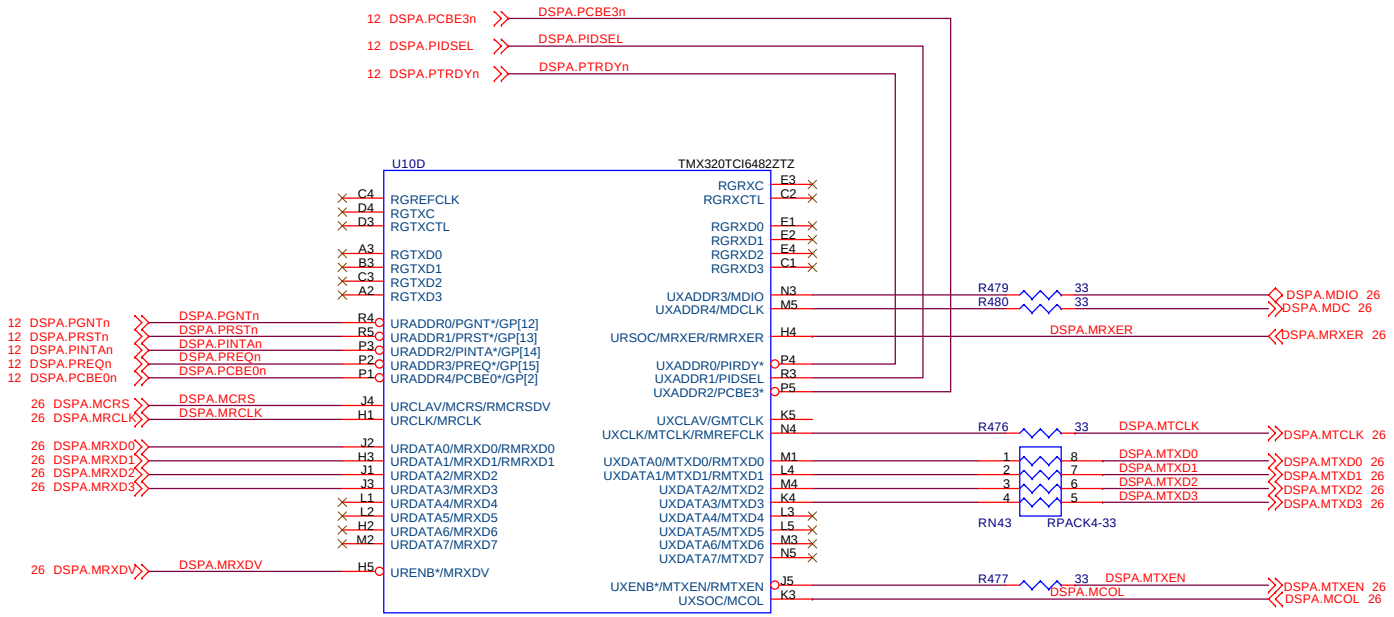

SPECTRUM DIGITAL INCORPORATED		
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Page Contents: UTOPIA INTERFACE		
Size:B	DWG NO 508552-2001	Revision: A
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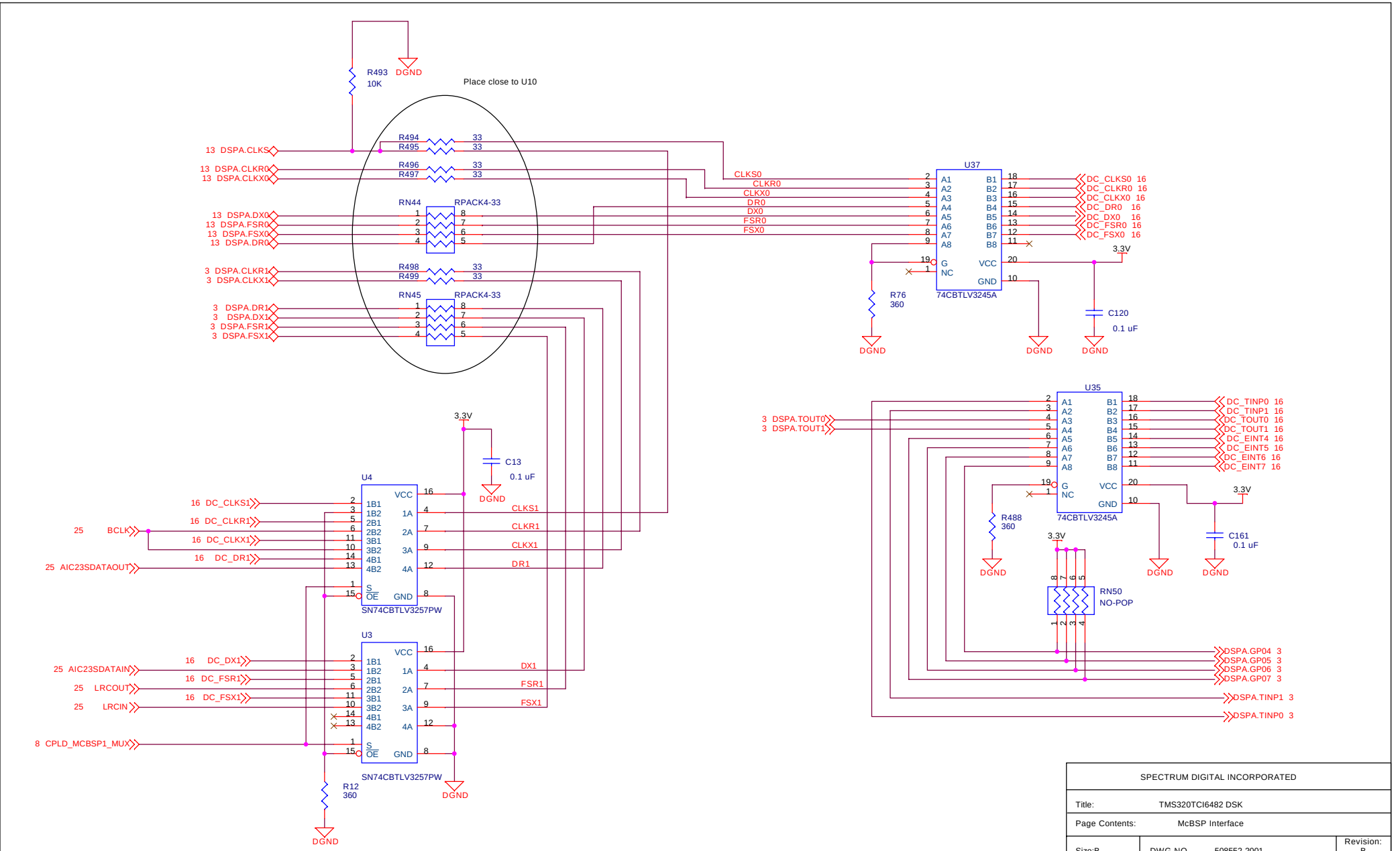

SPECTRUM DIGITAL INCORPORATED		
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Page Contents: McBSP Interface		
Size:B	DWG NO 508552-2001	Revision: B
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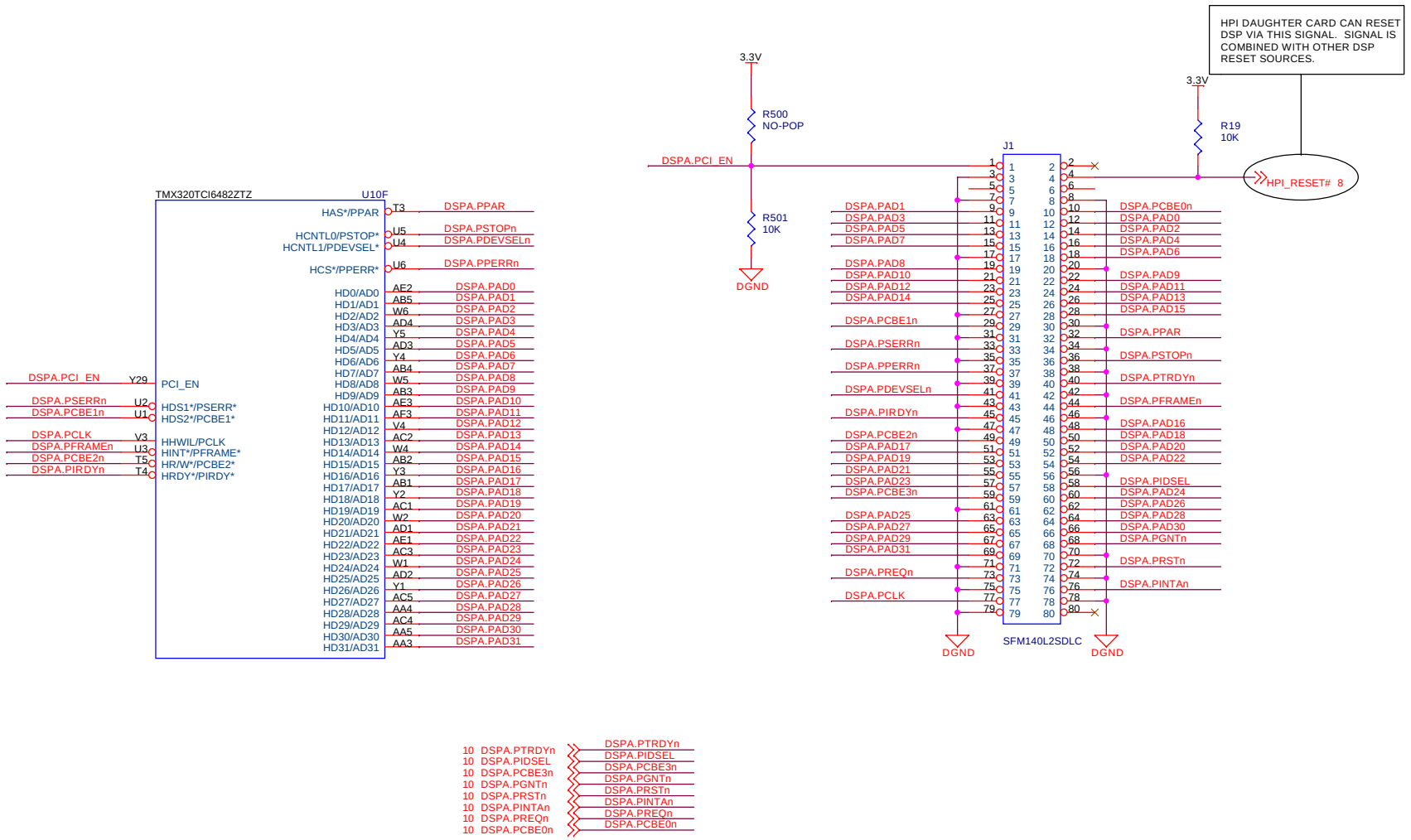

SPECTRUM DIGITAL INCORPORATED		
Title: TMS320TCI6482 DSK		
Page Contents: PCI/HOST PORT INTERFACE		
Size:B	DWG NO 508552-2001	Revision: A
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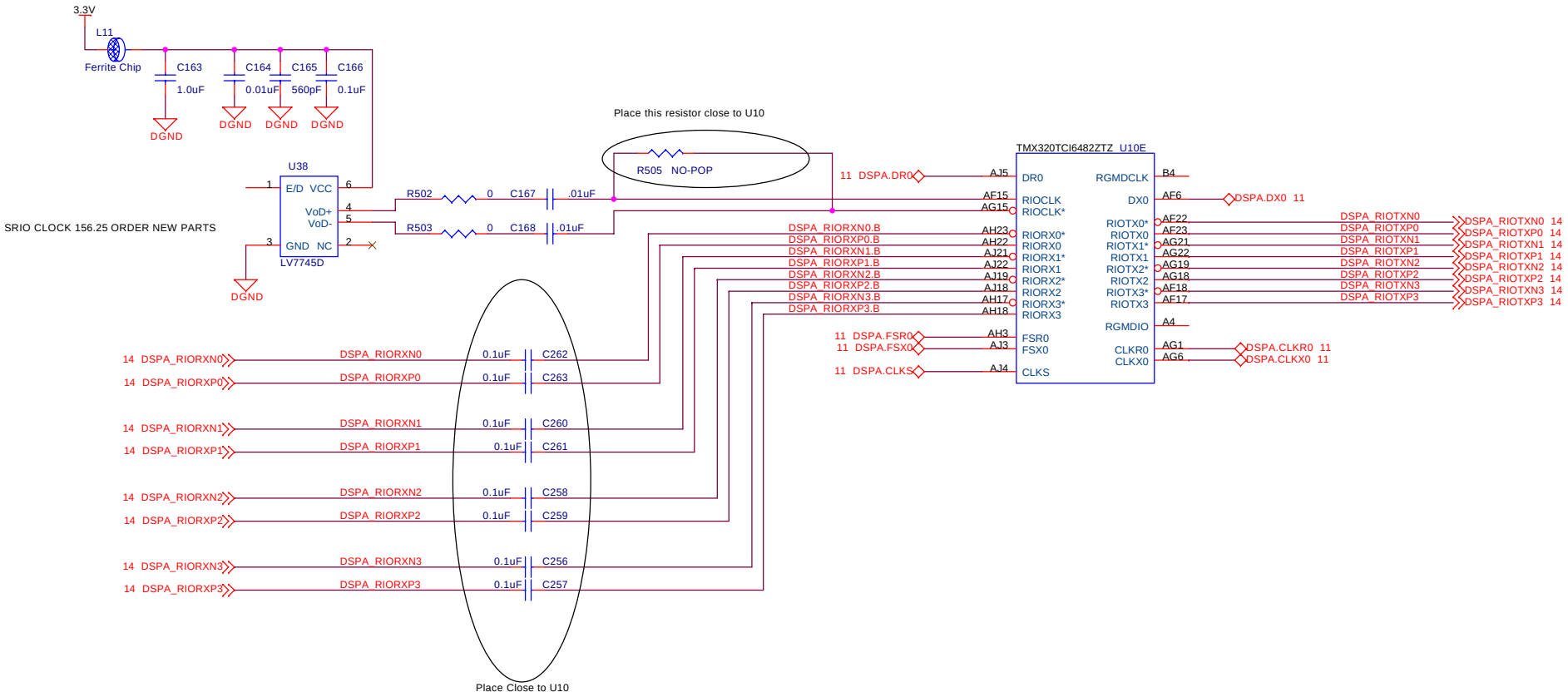

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Size:B	DWG NO 508552-2001	Revision: A
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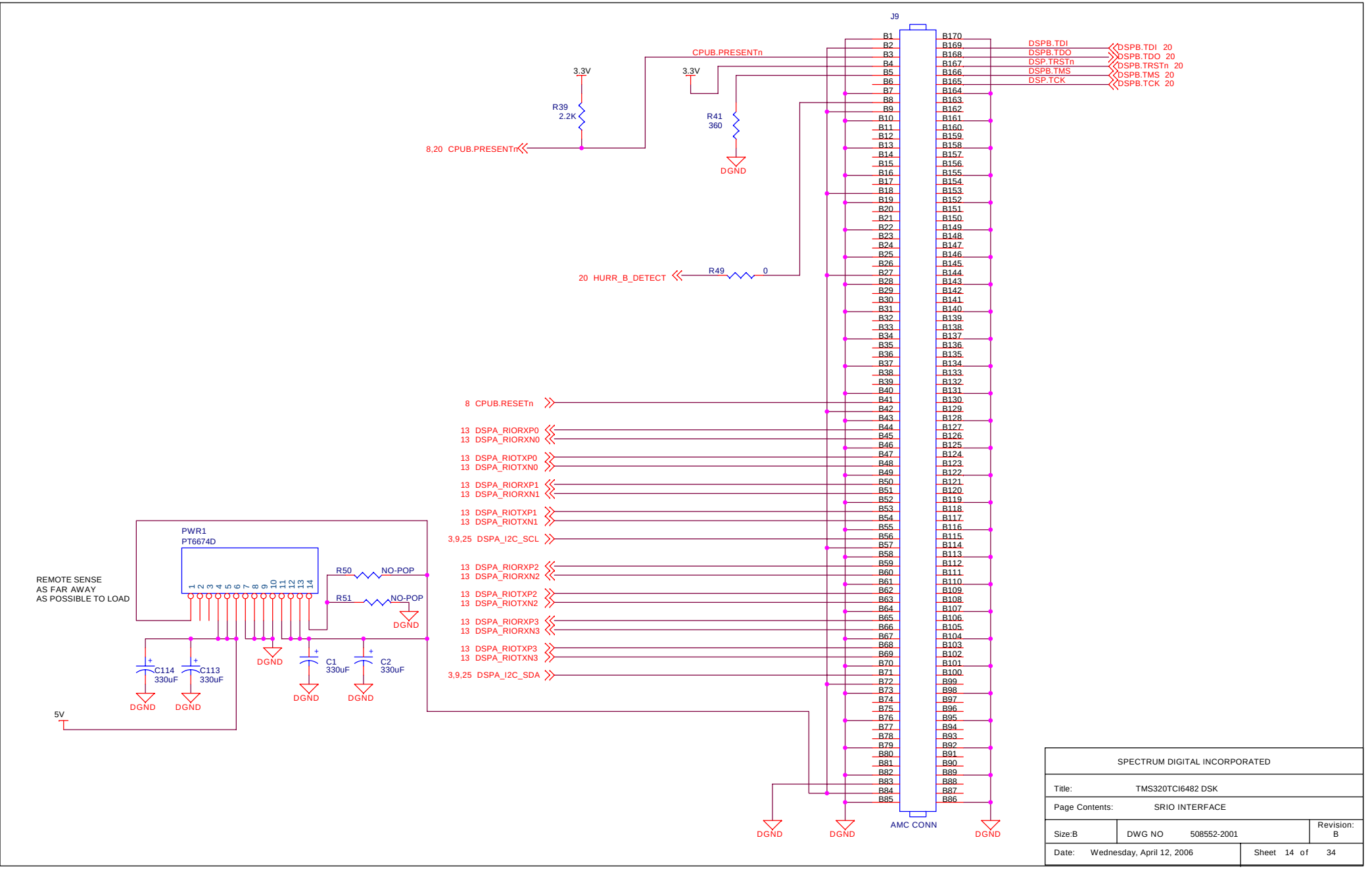

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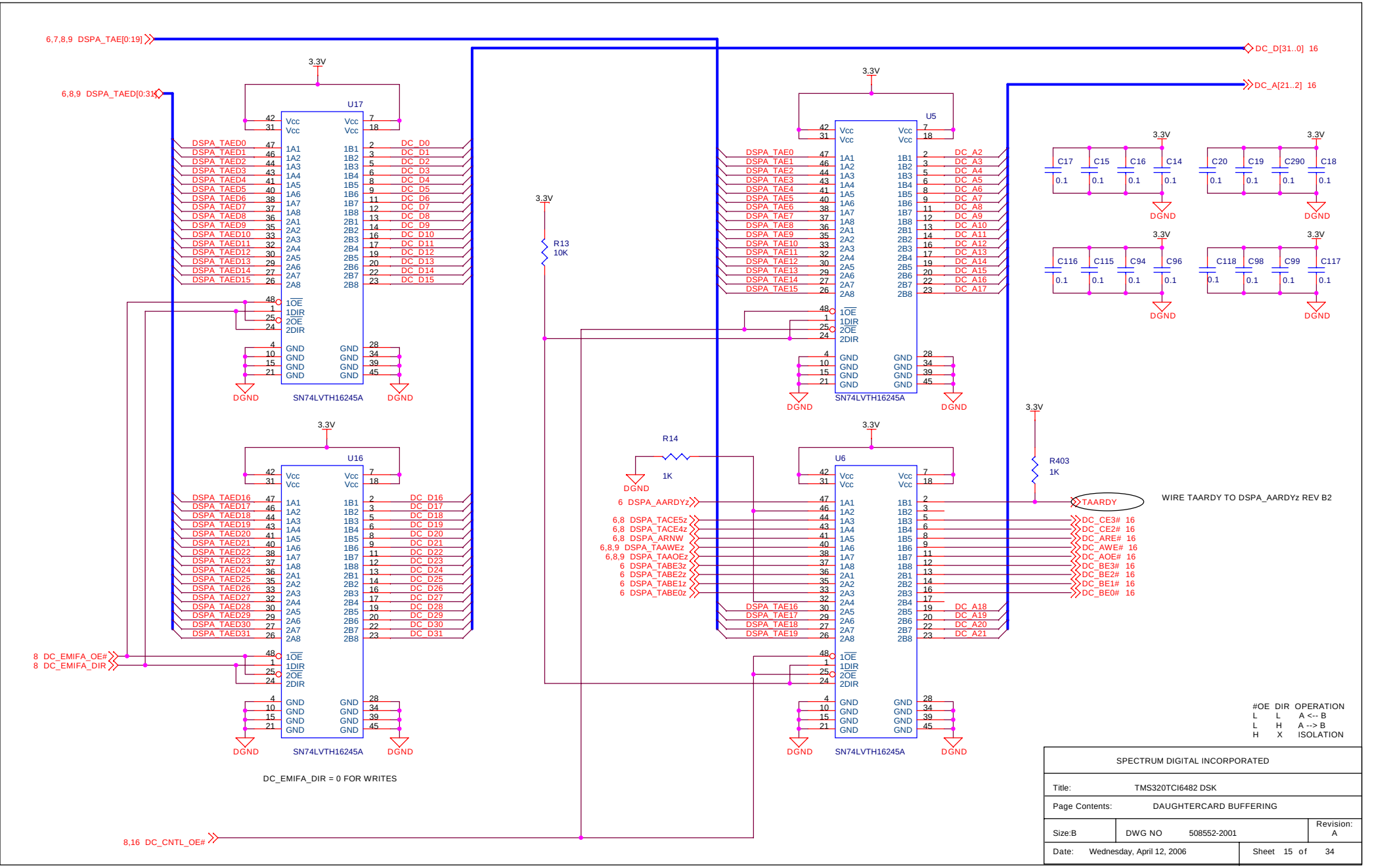
6,7,8,9 DSPA_TAE[0:19]
6,8,9 DSPA_TAED[0:31]
DC_D[31..0] 16
DC_A[21..2] 16
3.3V
U17
U5
U16
U6
SN74LVTH16245A
DSPA_TAED0
DSPA_TAED1
DSPA_TAED2
DSPA_TAED3
DSPA_TAED4
DSPA_TAED5
DSPA_TAED6
DSPA_TAED7
DSPA_TAED8
DSPA_TAED9
DSPA_TAED10
DSPA_TAED11
DSPA_TAED12
DSPA_TAED13
DSPA_TAED14
DSPA_TAED15
DC_D0
DC_D1
DC_D2
DC_D3
DC_D4
DC_D5
DC_D6
DC_D7
DC_D8
DC_D9
DC_D10
DC_D11
DC_D12
DC_D13
DC_D14
DC_D15
DSPA_TAED16
DSPA_TAED17
DSPA_TAED18
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DSPA_TAED25
DSPA_TAED26
DSPA_TAED27
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DC_D30
DC_D31
DSPA_TAE0
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DSPA_TAE2
DSPA_TAE3
DSPA_TAE4
DSPA_TAE5
DSPA_TAE6
DSPA_TAE7
DSPA_TAE8
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DSPA_TAE18
DSPA_TAE19
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DC_A20
DC_A21
1OE
1DIR
2OE
2DIR
GND
DGND
R13
10K
R14
1K
R403
1K
6 DSPA_AARDYz
TAARDY
WIRE TAARDY TO DSPA_AARDYz REV B2
6,8 DSPA_TACE5z
6,8 DSPA_TACE4z
6,8 DSPA_ARNW
6,8,9 DSPA_TAAWEz
6,8,9 DSPA_TAAOEz
6 DSPA_TABE3z
6 DSPA_TABE2z
6 DSPA_TABE1z
6 DSPA_TABE0z
DC_CE3# 16
DC_CE2# 16
DC_ARE# 16
DC_AWE# 16
DC_AOE# 16
DC_BE3# 16
DC_BE2# 16
DC_BE1# 16
DC_BE0# 16
8 DC_EMIFA_OE#
8 DC_EMIFA_DIR
8,16 DC_CNTL_OE#
C17
C15
C16
C14
C20
C19
C290
C18
C116
C115
C94
C96
C118
C98
C99
C117
0.1
DC_EMIFA_DIR = 0 FOR WRITES
#OE DIR OPERATION
L L A <-- B
L H A --> B
H X ISOLATION
SPECTRUM DIGITAL INCORPORATED
Title: TMS320TCI6482 DSK
Page Contents: DAUGHTERCARD BUFFERING
Size:B
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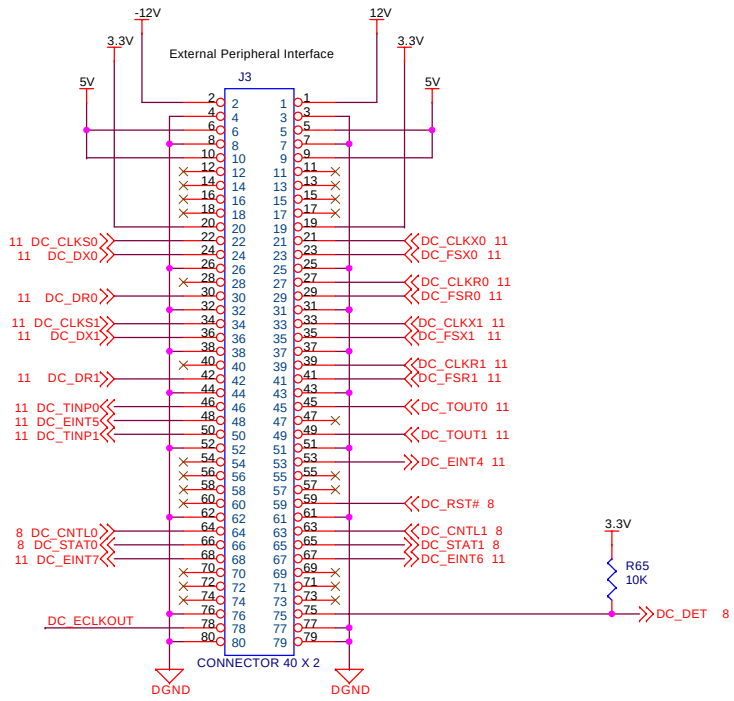

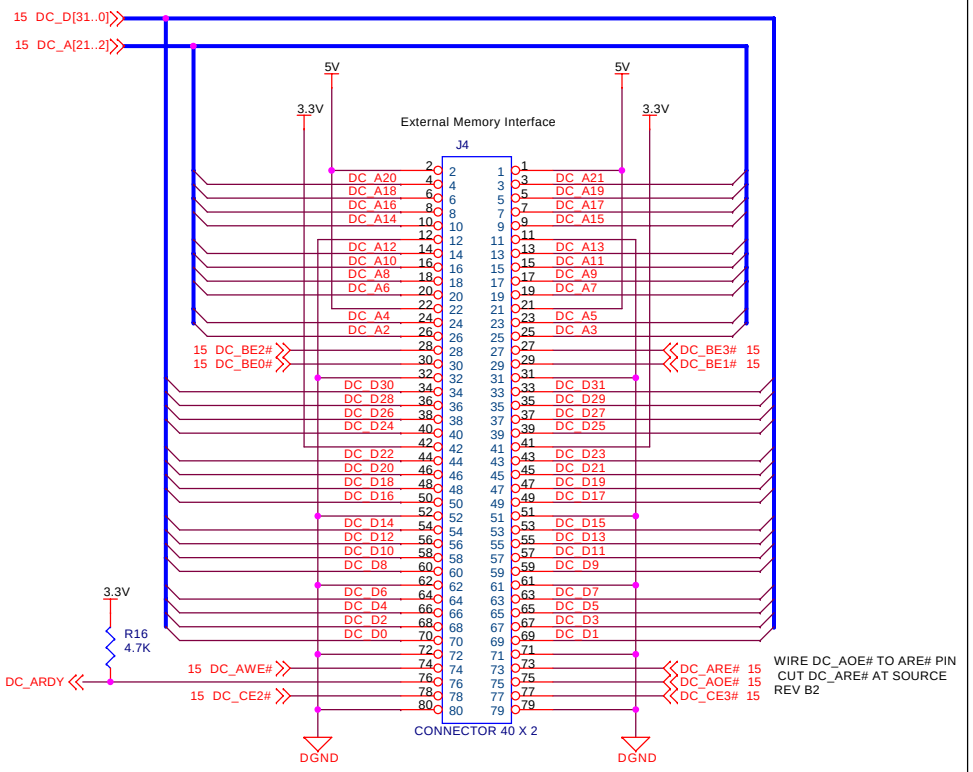

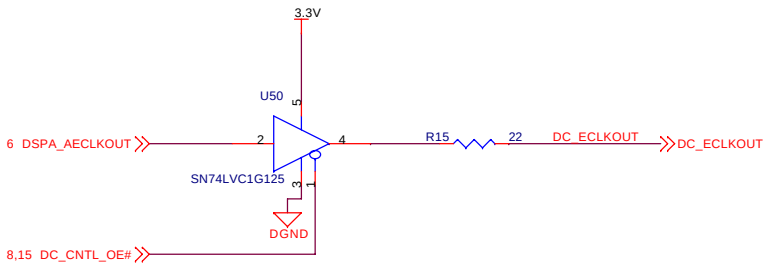

SPECTRUM DIGITAL INCORPORATED		
Title: TMS320TCI6482 DSK		
Page Contents: DAUGHTERCARD I/F		
Size:B	DWG NO 508552-2001	Revision: A
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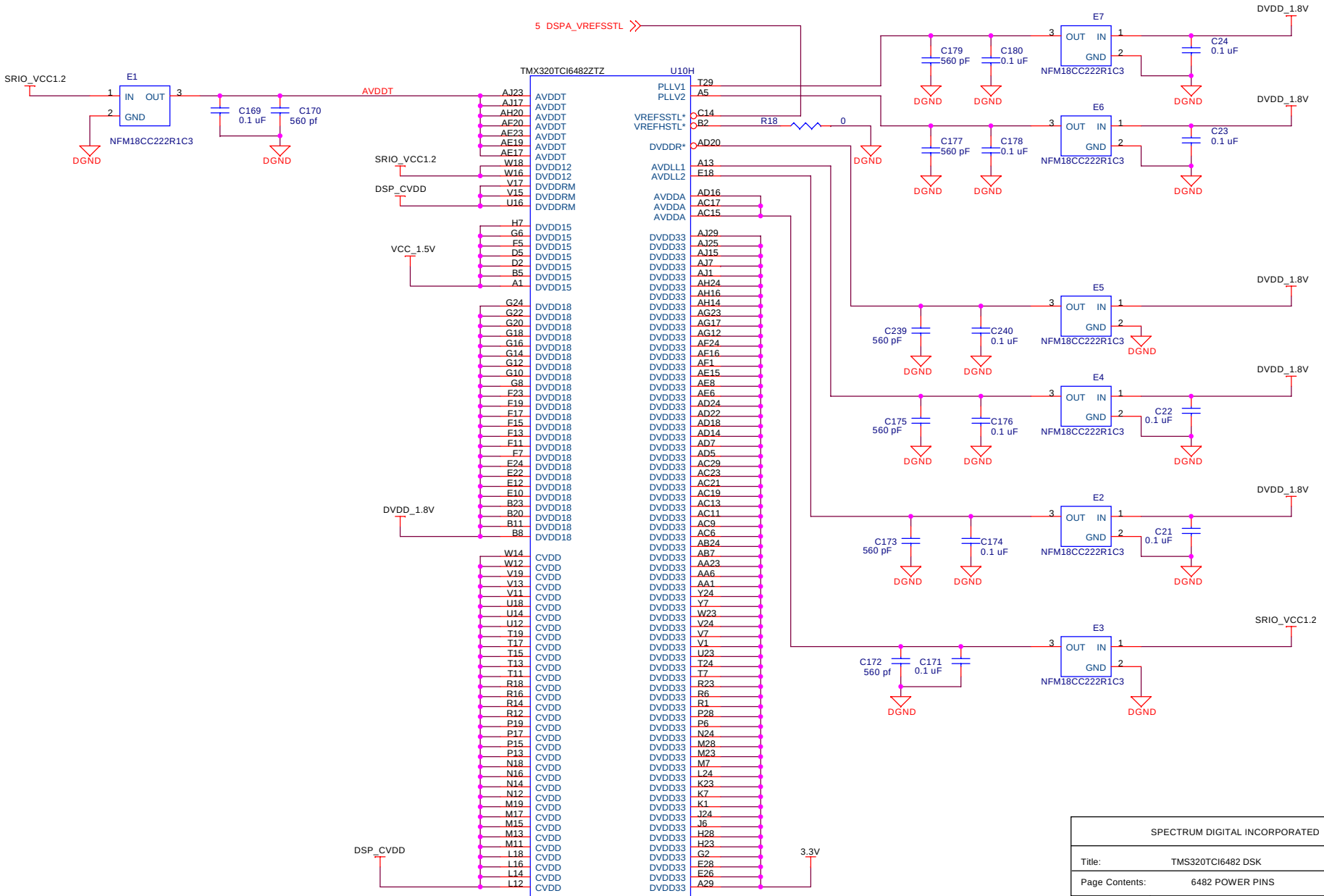
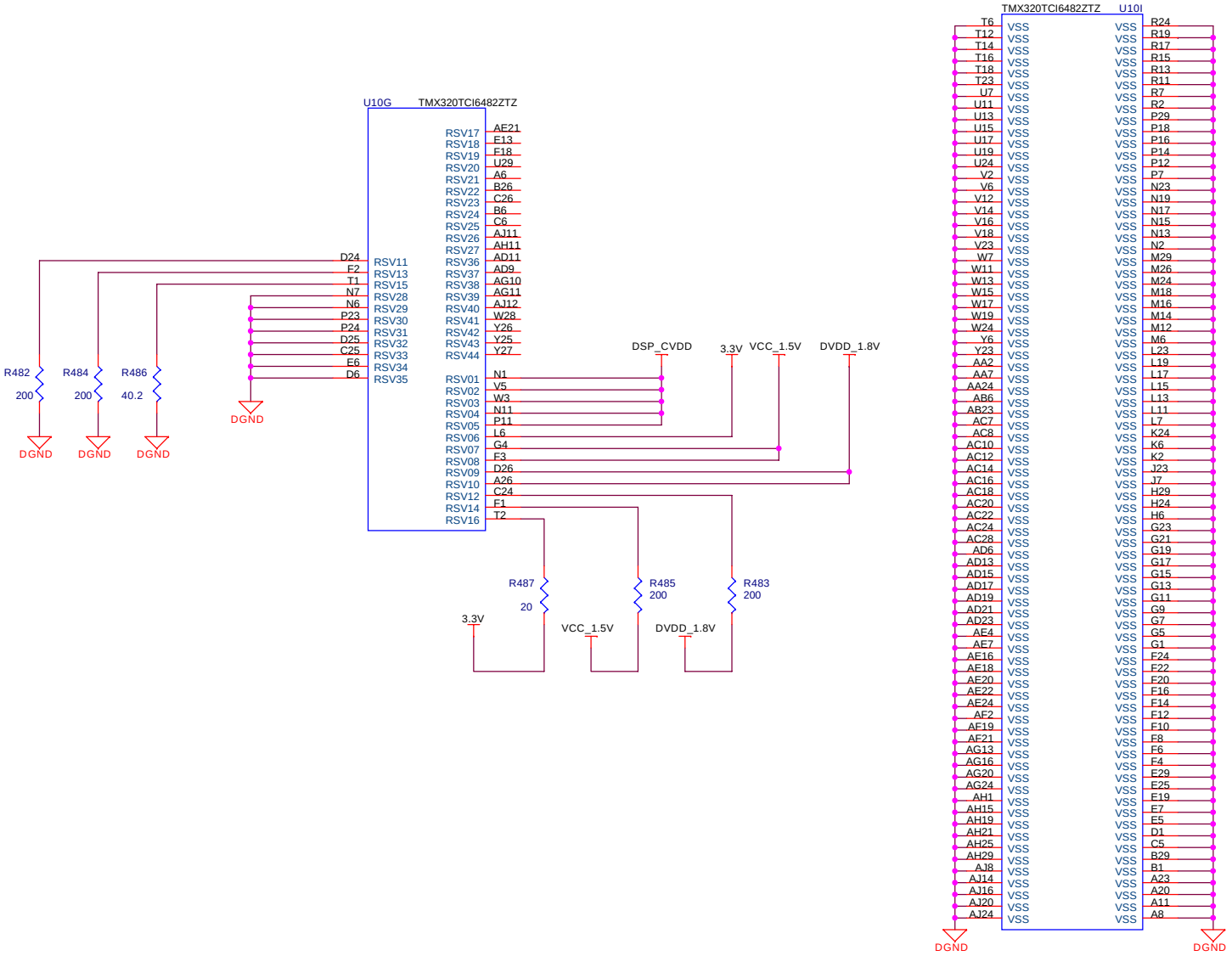


SPECTRUM DIGITAL INCORPORATED		
Title: TMS320TCI6482 DSK		
Page Contents: 6482 POWER PINS		
Size:B	DWG NO 508552-2001	Revision: A
Date: Wednesday, April 12, 2006	Sheet 17 of 34	



SPECTRUM DIGITAL INCORPORATED		
Title: TMS320TCI6482 DSK		
Page Contents: 6482 POWER PINS		
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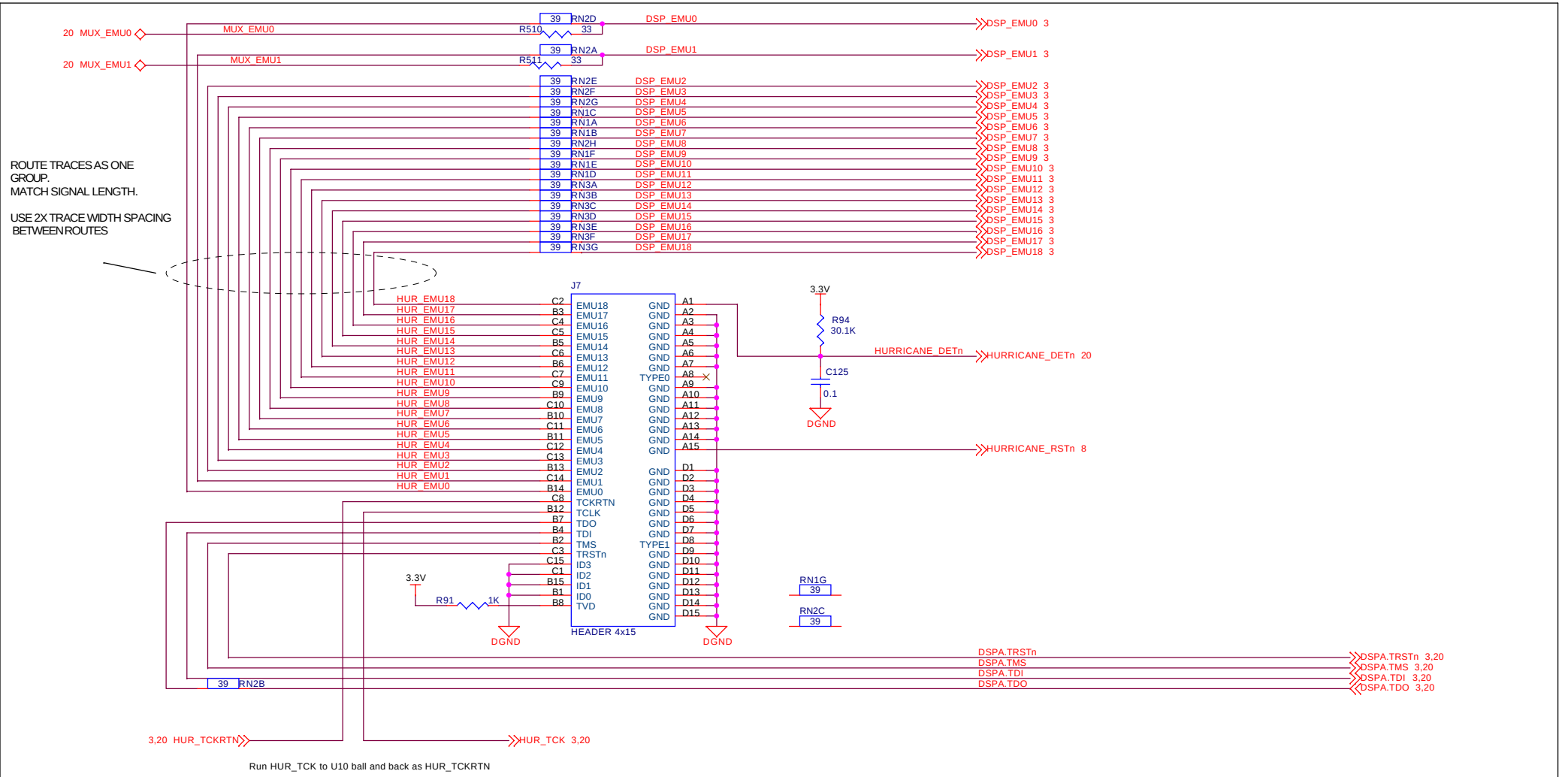

SPECTRUM DIGITAL INCORPORATED		
Title: TMS320TCI6482 DSK		
Page Contents: Emulation Interface		
Size:B	DWG NO 508552-2001	Revision: A
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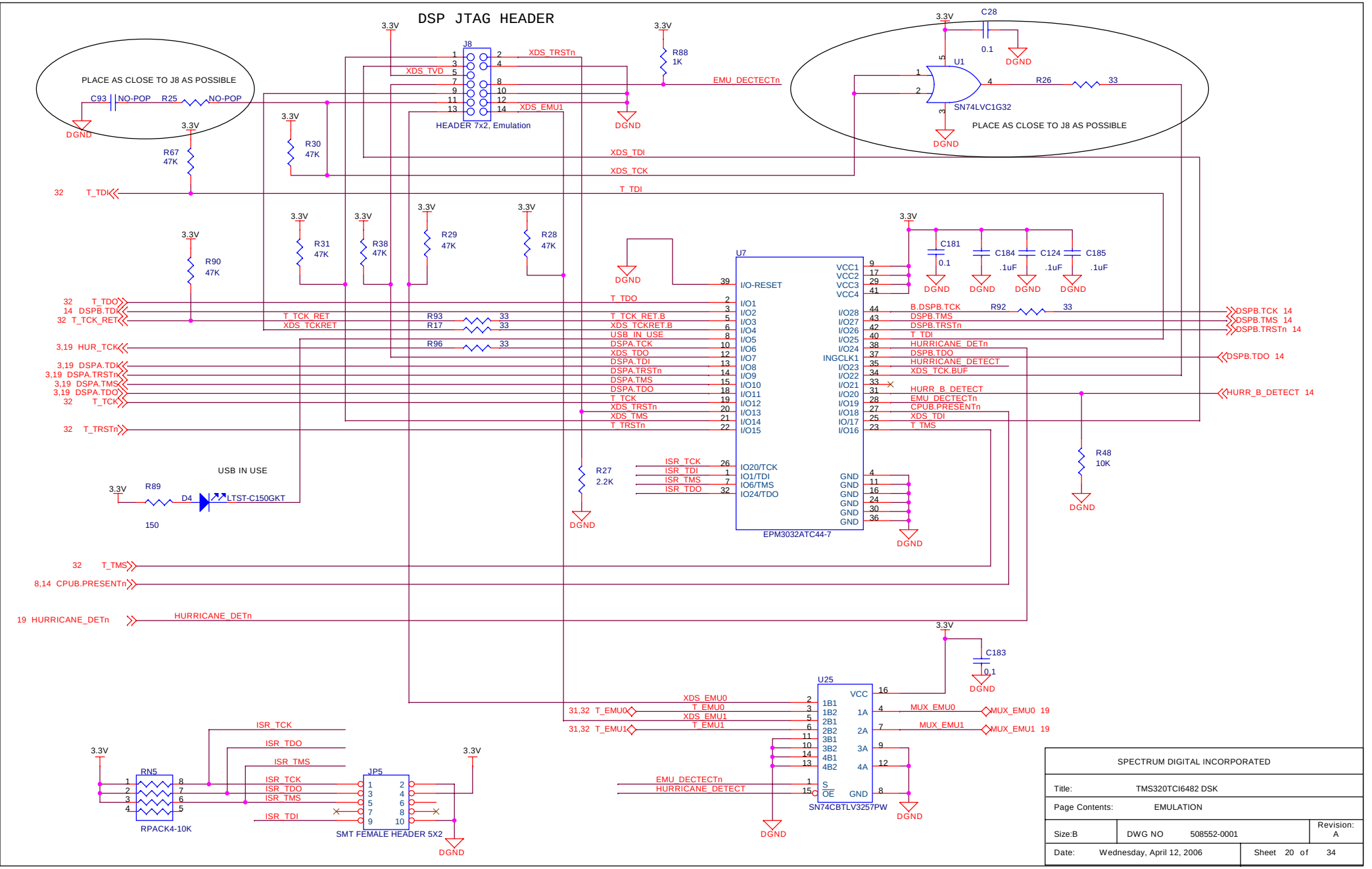

SPECTRUM DIGITAL INCORPORATED		
Title: TMS320TCI6482 DSK		
Page Contents: EMULATION		
Size:B	DWG NO 508552-0001	Revision: A
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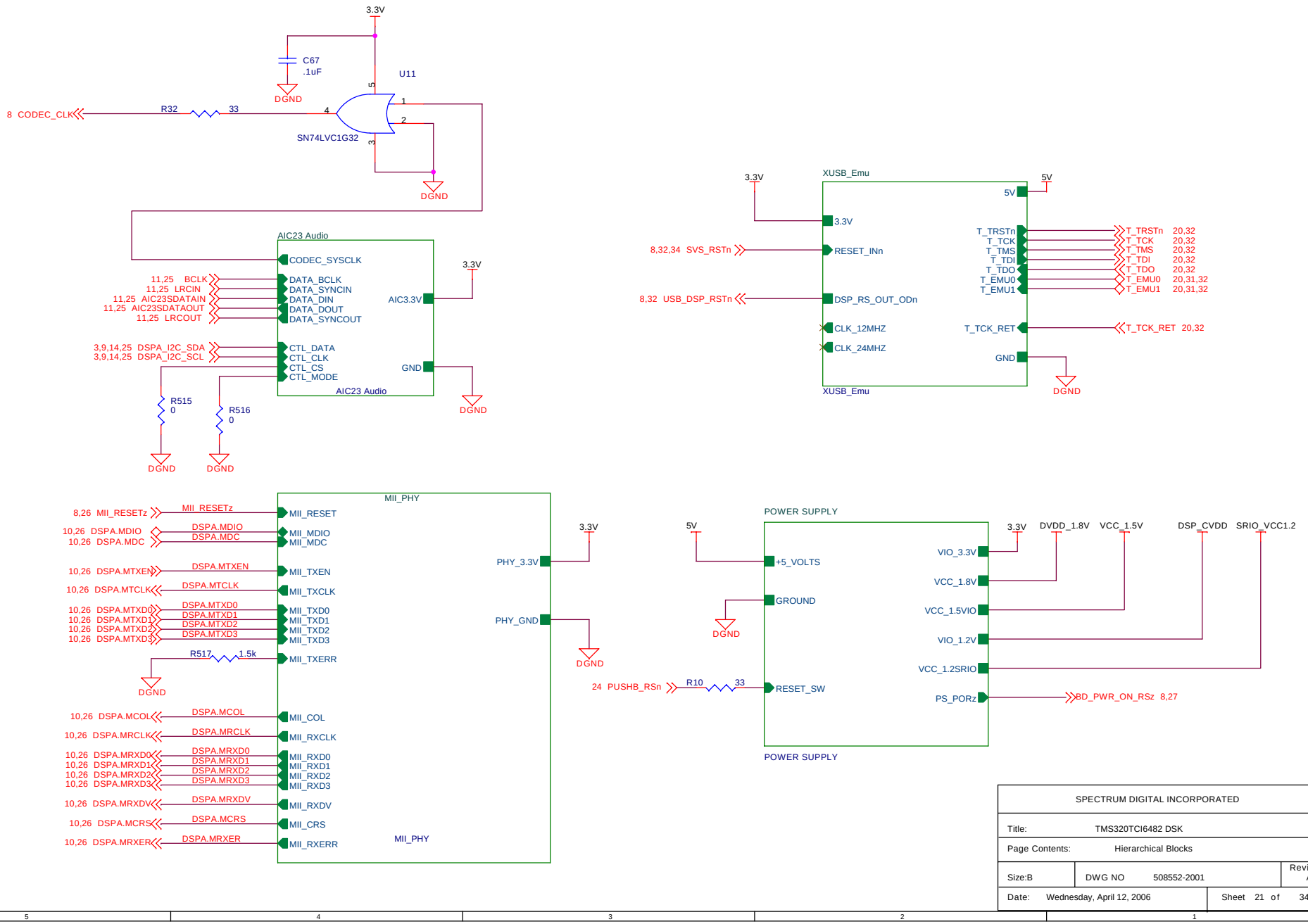
3.3V
C67
.1uF
DGND
U11
8 CODEC_CLK
R32
33
SN74LVC1G32
DGND
AIC23 Audio
CODEC_SYSCLK
11,25 BCLK
11,25 LRCIN
11,25 AIC23SDATAIN
11,25 AIC23SDATAOUT
11,25 LRCOUT
DATA_BCLK
DATA_SYNCIN
DATA_DIN
DATA_DOUT
DATA_SYNCOUT
AIC3.3V
3.3V
3,9,14,25 DSPA_I2C_SDA
3,9,14,25 DSPA_I2C_SCL
CTL_DATA
CTL_CLK
CTL_CS
CTL_MODE
GND
AIC23 Audio
DGND
R515
0
R516
0
DGND
DGND
XUSB_Emu
3.3V
5V
8,32,34 SVS_RSTn
RESET_INn
8,32 USB_DSP_RSTn
DSP_RS_OUT_ODn
CLK_12MHZ
CLK_24MHZ
T_TRSTn
T_TCK
T_TMS
T_TDI
T_TDO
T_EMU0
T_EMU1
T_TRSTn 20,32
T_TCK 20,32
T_TMS 20,32
T_TDI 20,32
T_TDO 20,32
T_EMU0 20,31,32
T_EMU1 20,31,32
T_TCK_RET
T_TCK_RET 20,32
GND
DGND
XUSB_Emu
MII_PHY
8,26 MII_RESETz
MII_RESETz
MII_RESET
10,26 DSPA.MDIO
10,26 DSPA.MDC
DSPA.MDIO
DSPA.MDC
MII_MDIO
MII_MDC
10,26 DSPA.MTXEN
DSPA.MTXEN
MII_TXEN
10,26 DSPA.MTCLK
DSPA.MTCLK
MII_TXCLK
10,26 DSPA.MTXD0
10,26 DSPA.MTXD1
10,26 DSPA.MTXD2
10,26 DSPA.MTXD3
DSPA.MTXD0
DSPA.MTXD1
DSPA.MTXD2
DSPA.MTXD3
MII_TXD0
MII_TXD1
MII_TXD2
MII_TXD3
R517
1.5k
MII_TXERR
DGND
10,26 DSPA.MCOL
10,26 DSPA.MRCLK
DSPA.MCOL
DSPA.MRCLK
MII_COL
MII_RXCLK
10,26 DSPA.MRXD0
10,26 DSPA.MRXD1
10,26 DSPA.MRXD2
10,26 DSPA.MRXD3
DSPA.MRXD0
DSPA.MRXD1
DSPA.MRXD2
DSPA.MRXD3
MII_RXD0
MII_RXD1
MII_RXD2
MII_RXD3
10,26 DSPA.MRXDV
DSPA.MRXDV
MII_RXDV
10,26 DSPA.MCRS
DSPA.MCRS
MII_CRS
10,26 DSPA.MRXER
DSPA.MRXER
MII_RXERR
MII_PHY
PHY_3.3V
PHY_GND
3.3V
DGND
POWER SUPPLY
5V
+5_VOLTS
GROUND
DGND
24 PUSHB_RSn
R10
33
RESET_SW
VIO_3.3V
VCC_1.8V
VCC_1.5VIO
VIO_1.2V
VCC_1.2SRIO
PS_PORz
3.3V
DVDD_1.8V
VCC_1.5V
DSP_CVDD
SRIO_VCC1.2
BD_PWR_ON_RSz 8,27
POWER SUPPLY
SPECTRUM DIGITAL INCORPORATED
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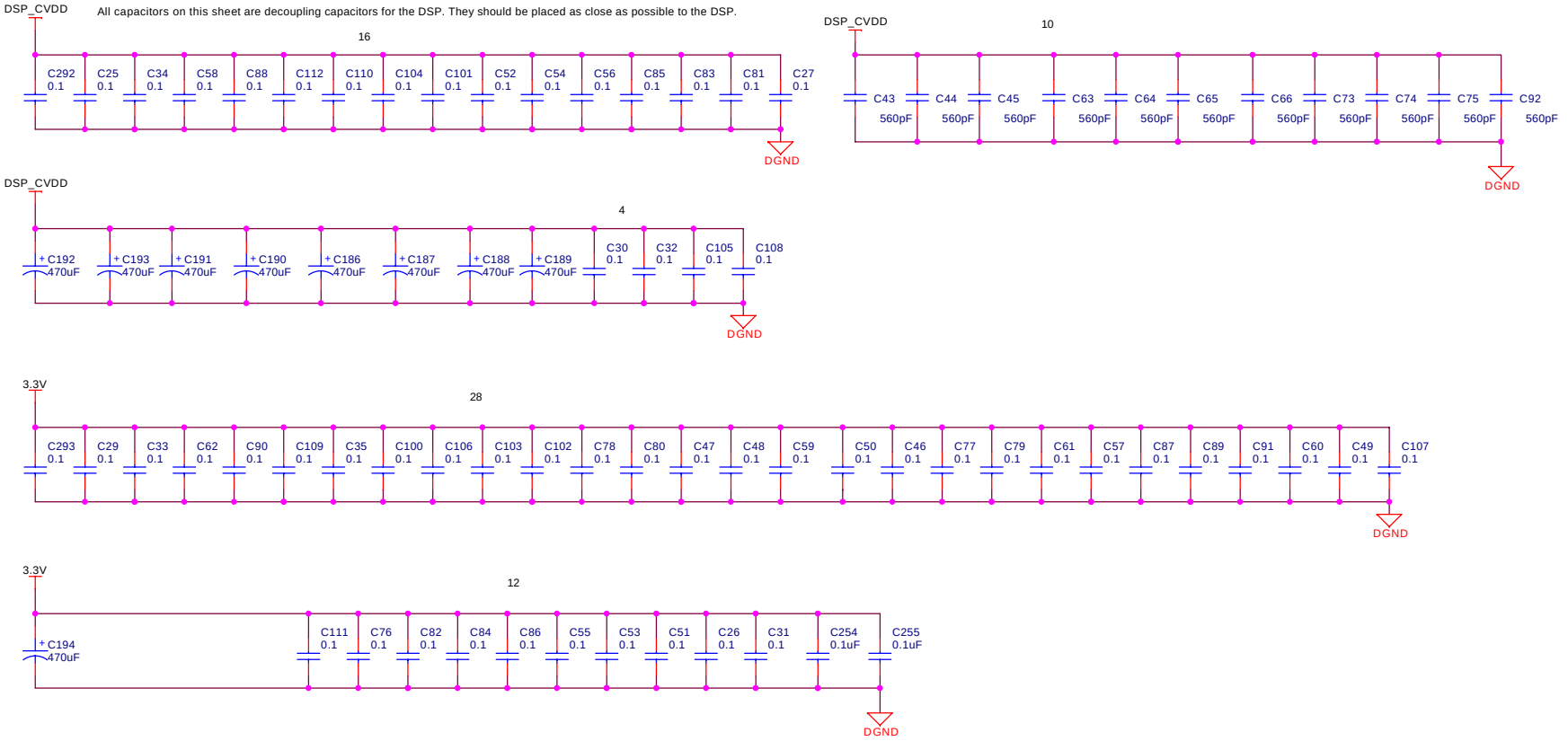
All capacitors on this sheet are decoupling capacitors for the DSP. They should be placed as close as possible to the DSP.



SPECTRUM DIGITAL INCORPORATED		
Title: TMS320TCI6482 DSK		
Page Contents: Decoupling Capacitors I		
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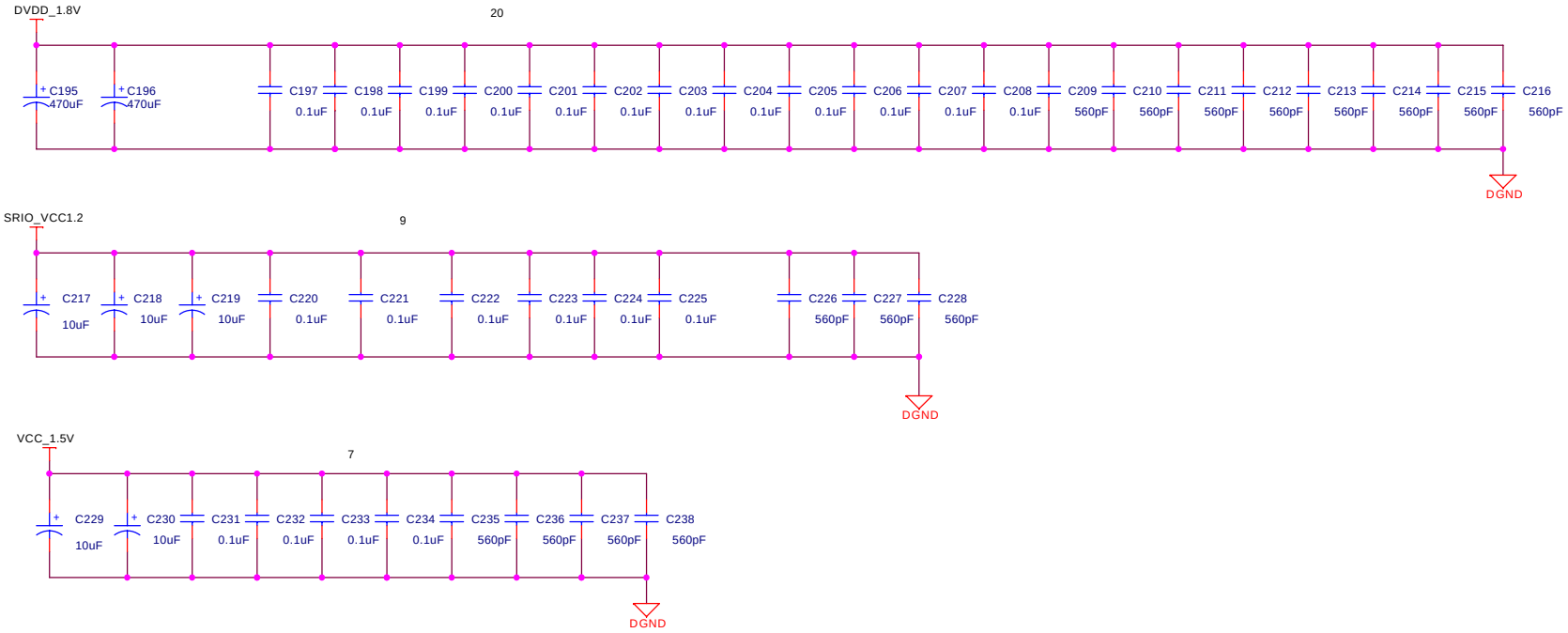

SPECTRUM DIGITAL INCORPORATED		
Title: TMS320TCI6482 DSK		
Page Contents: Decoupling Capacitors II		
Size:B	DWG NO 508552-2001	Revision: A
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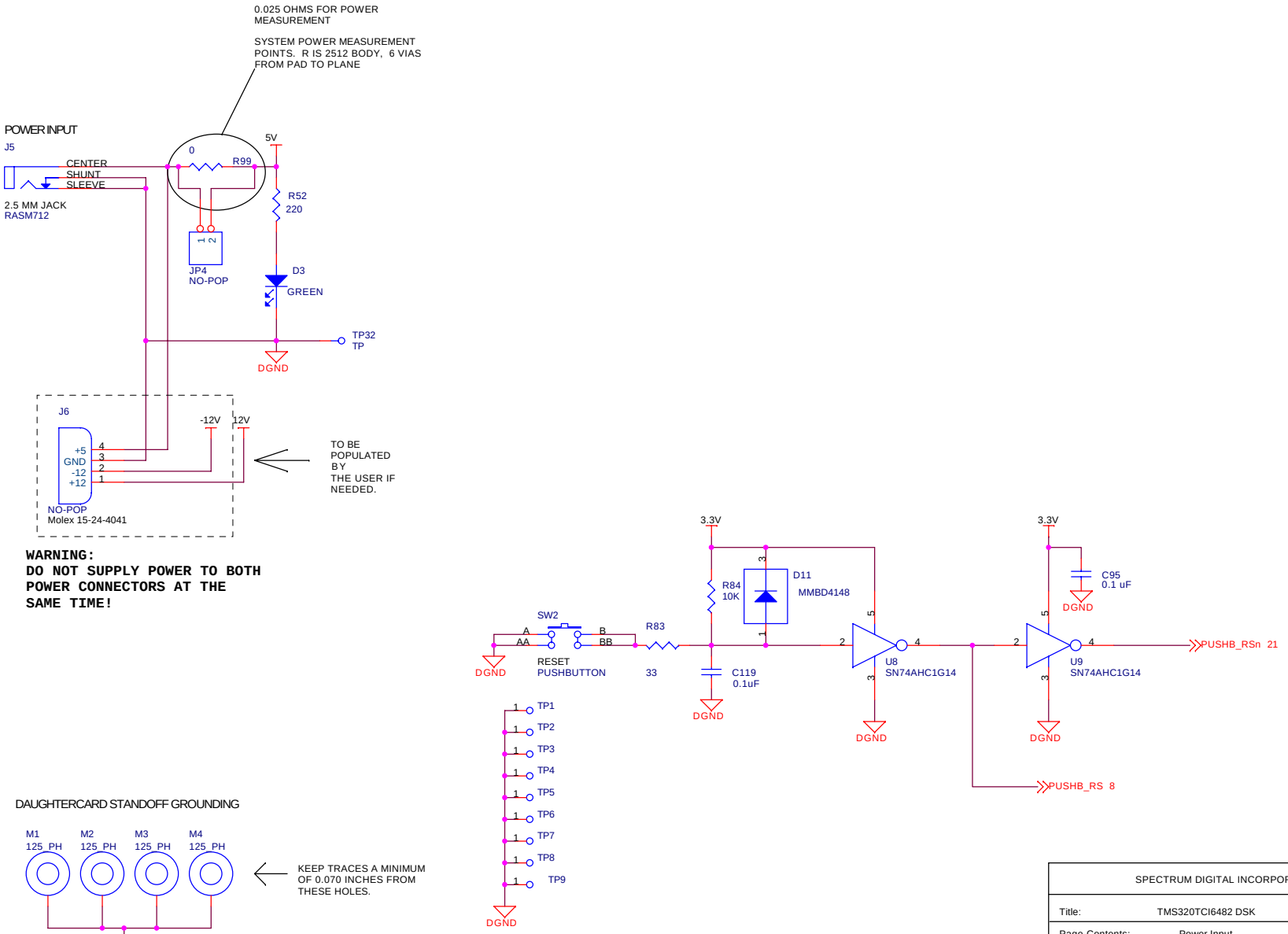

SPECTRUM DIGITAL INCORPORATED		
Title: TMS320TCI6482 DSK		
Page Contents: Power Input		
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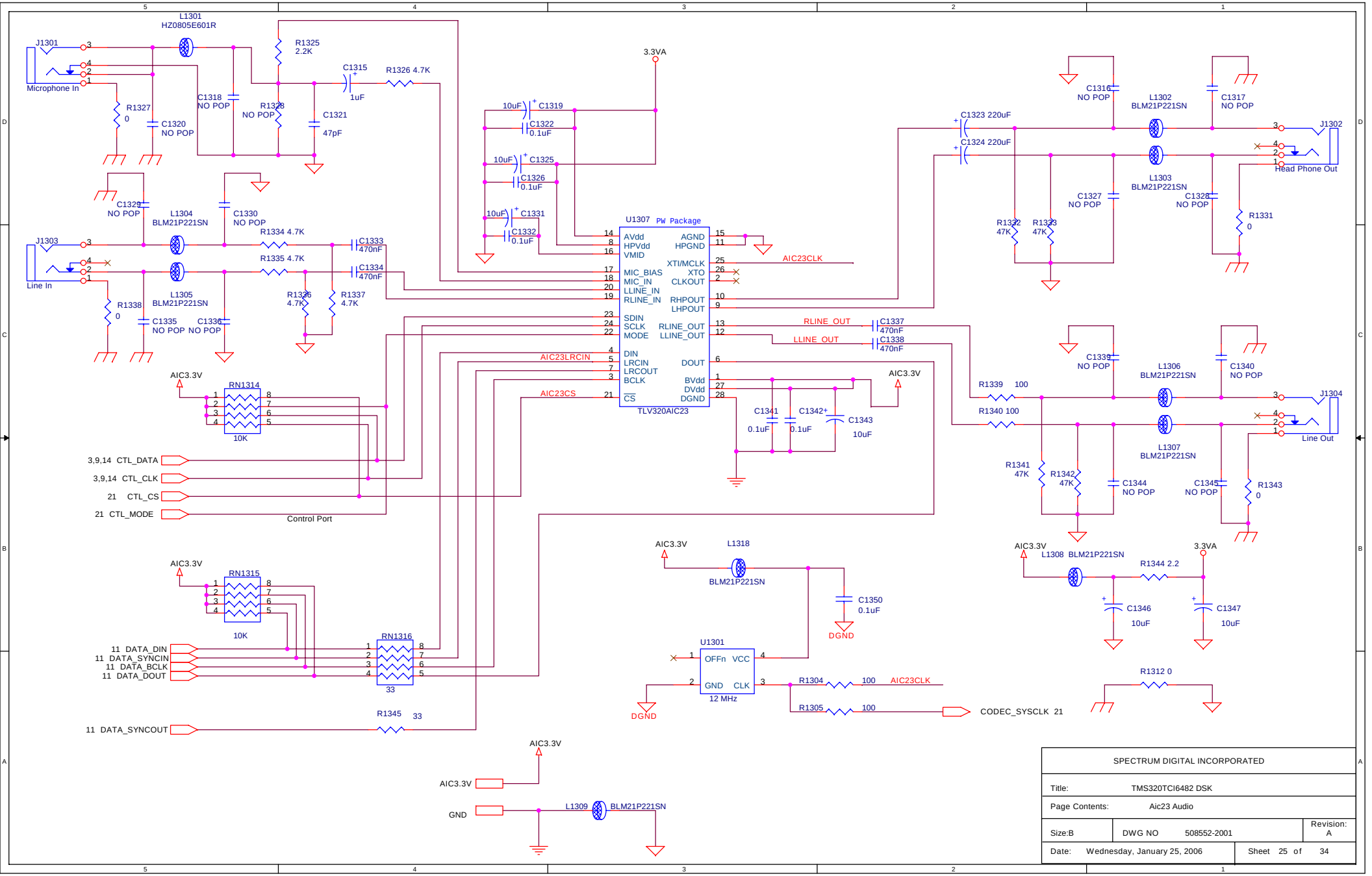
L1301
HZ0805E601R
J1301
Microphone In
R1325
2.2K
C1315
1uF
R1326 4.7K
C1318
NO POP
R1328
NO POP
C1321
47pF
R1327
0
C1320
NO POP
C1329
NO POP
L1304
BLM21P221SN
C1330
NO POP
J1303
Line In
R1334 4.7K
R1335 4.7K
C1333
470nF
C1334
470nF
L1305
BLM21P221SN
R1336
4.7K
R1337
4.7K
R1338
0
C1335
NO POP
C1336
NO POP
3.3VA
10uF C1319
C1322
0.1uF
10uF C1325
C1326
0.1uF
10uF C1331
C1332
0.1uF
U1307 PW Package
AVdd
HPVdd
VMID
MIC_BIAS
MIC_IN
LLINE_IN
RLINE_IN
SDIN
SCLK
MODE
DIN
LRCIN
LRCOUT
BCLK
CS
AGND
HPGND
XTI/MCLK
XTO
CLKOUT
RHPOUT
LHPOUT
RLINE_OUT
LLINE_OUT
DOUT
BVdd
DVdd
DGND
TLV320AIC23
AIC23CLK
AIC23LRCIN
AIC23CS
RLINE_OUT
LLINE_OUT
C1337
470nF
C1338
470nF
C1341
0.1uF
C1342
0.1uF
C1343
10uF
AIC3.3V
RN1314
10K
3,9,14 CTL_DATA
3,9,14 CTL_CLK
21 CTL_CS
21 CTL_MODE
Control Port
RN1315
10K
RN1316
33
11 DATA_DIN
11 DATA_SYNCIN
11 DATA_BCLK
11 DATA_DOUT
R1345 33
11 DATA_SYNCOUT
L1318
BLM21P221SN
C1350
0.1uF
DGND
U1301
OFFn
VCC
GND
CLK
12 MHz
R1304 100 AIC23CLK
R1305 100
CODEC_SYSCLK 21
C1323 220uF
C1324 220uF
C1316
NO POP
L1302
BLM21P221SN
C1317
NO POP
J1302
Head Phone Out
L1303
BLM21P221SN
C1327
NO POP
C1328
NO POP
R1331
0
R1332
47K
R1333
47K
C1339
NO POP
L1306
BLM21P221SN
C1340
NO POP
J1304
Line Out
R1339 100
R1340 100
L1307
BLM21P221SN
R1341
47K
R1342
47K
C1344
NO POP
C1345
NO POP
R1343
0
L1308 BLM21P221SN
R1344 2.2
C1346
10uF
C1347
10uF
R1312 0
L1309
BLM21P221SN
GND
SPECTRUM DIGITAL INCORPORATED
Title: TMS320TCI6482 DSK
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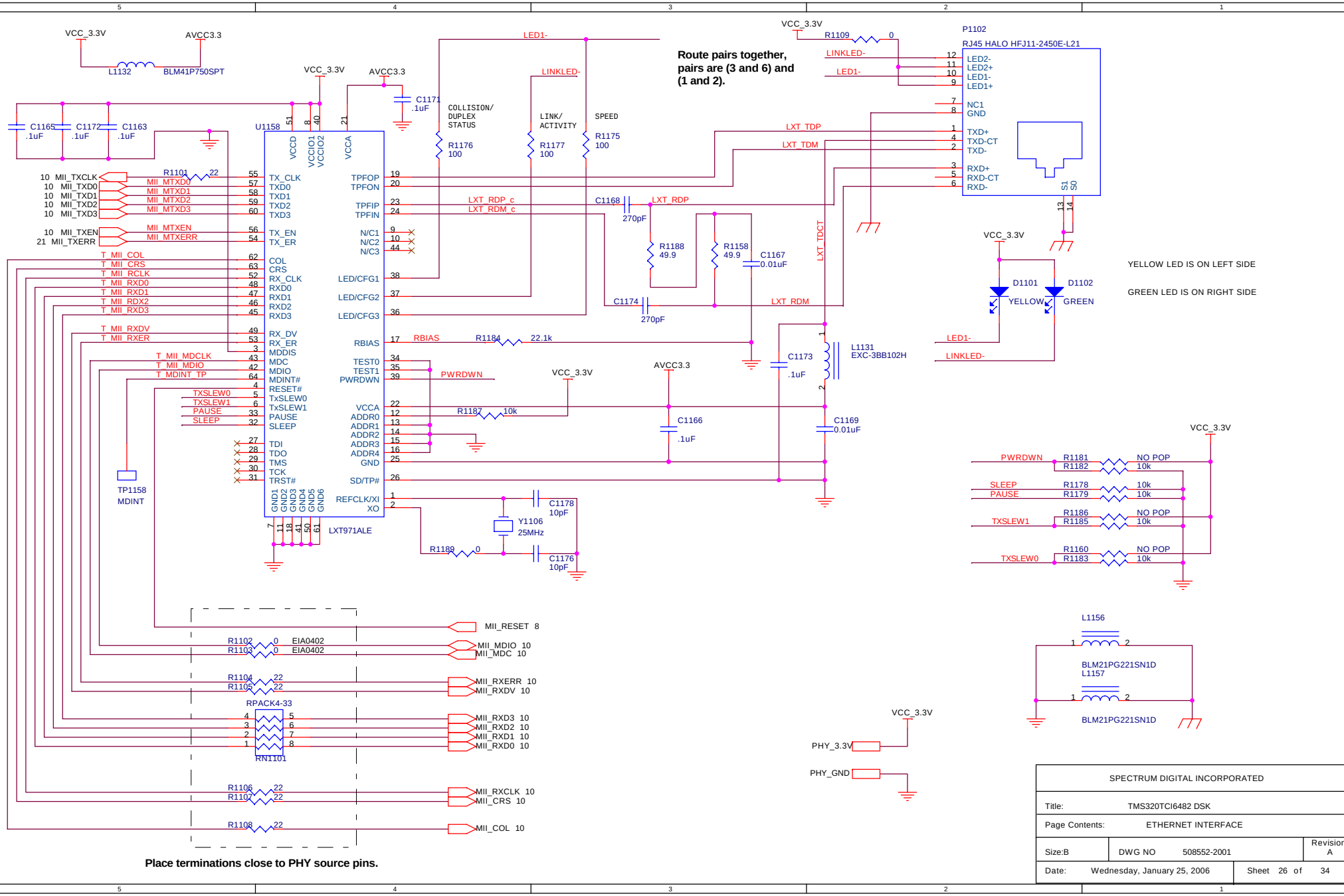
Route pairs together, pairs are (3 and 6) and (1 and 2).
Place terminations close to PHY source pins.
YELLOW LED IS ON LEFT SIDE
GREEN LED IS ON RIGHT SIDE
U1158
LXT971ALE
P1102
RJ45 HALO HFJ11-2450E-L21
L1131
EXC-3BB102H
L1156
L1157
BLM21PG221SN1D
RPACK4-33
RN1101
Y1106
25MHz
TP1158
MDINT
SPECTRUM DIGITAL INCORPORATED
Title: TMS320TCI6482 DSK
Page Contents: ETHERNET INTERFACE
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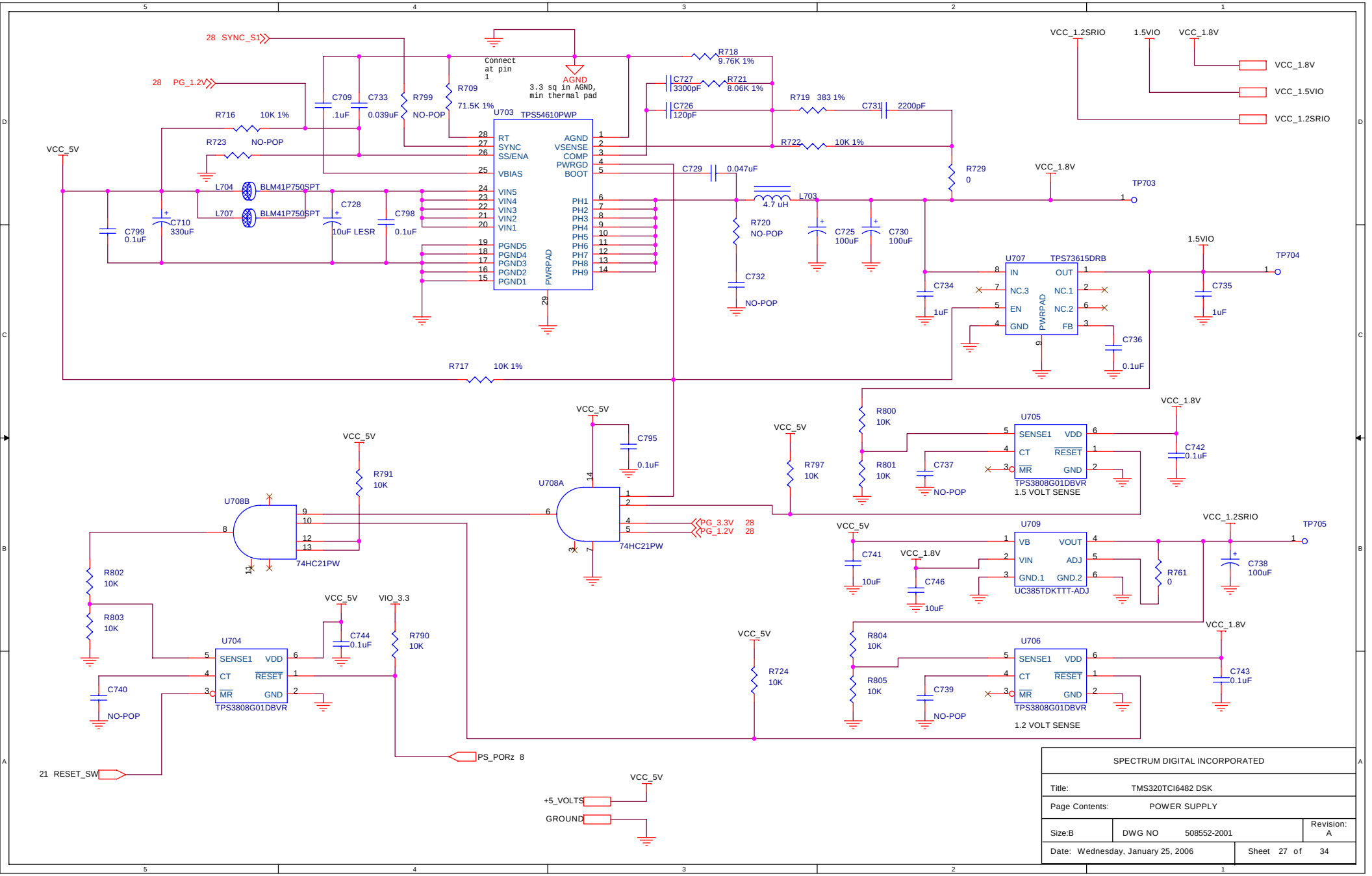

SPECTRUM DIGITAL INCORPORATED		
Title: TMS320TCI6482 DSK		
Page Contents: POWER SUPPLY		
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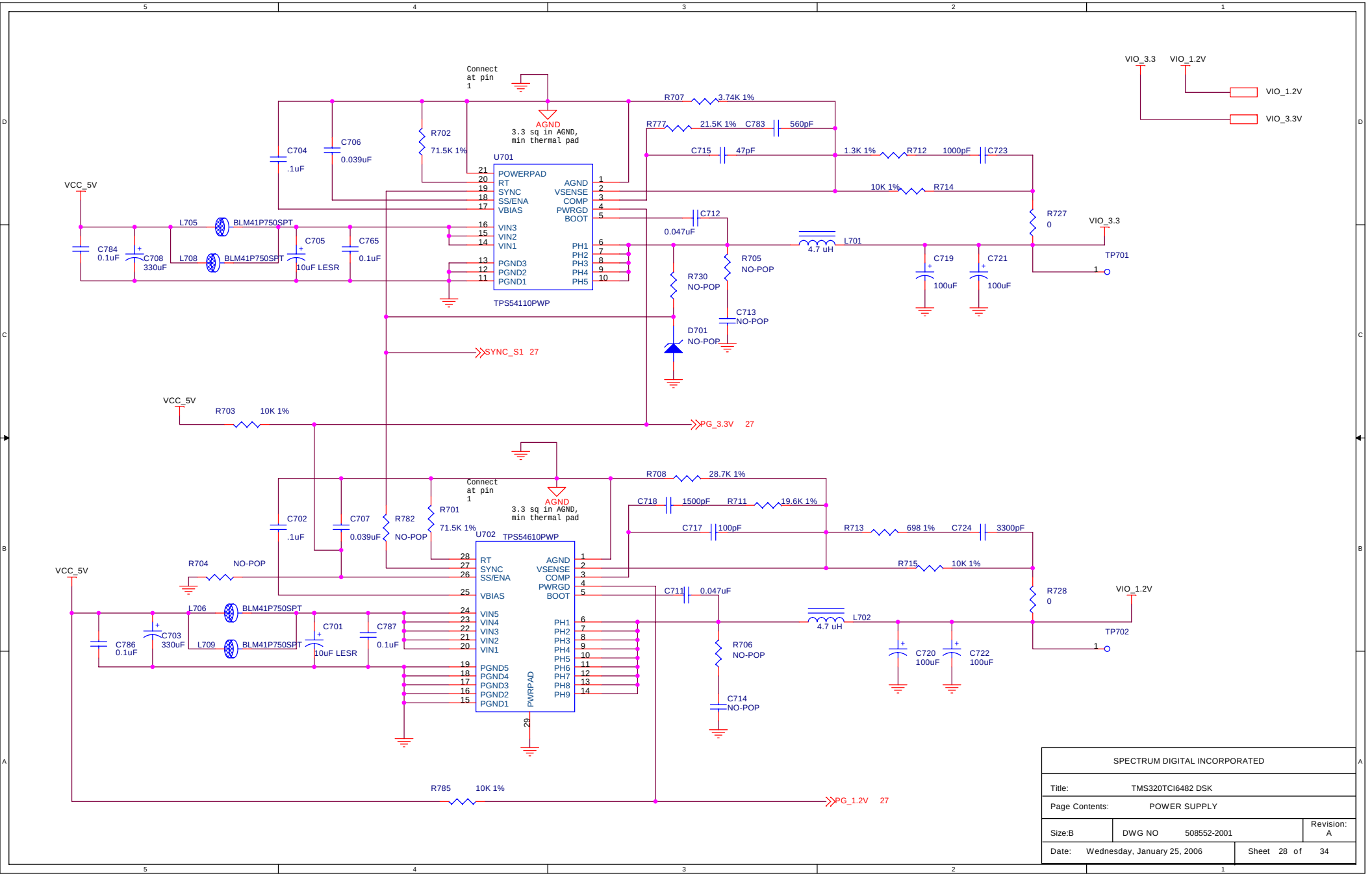

SPECTRUM DIGITAL INCORPORATED		
Title: TMS320TCI6482 DSK		
Page Contents: POWER SUPPLY		
Size:B	DWG NO 508552-2001	Revision: A
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