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REVISION STATUS OF SHEETS

REV	A	A	A										
SH	21	22	23										
REV	A	A	A	A	A	A	A	A	A	A			
SH	11	12	13	14	15	16	17	18	19	20			
REV	B	A	A	A	A	A	A	A	A	A			
SH	1	2	3	4	5	6	7	8	9	10			

		DWN	DATE
		R.R.P.	AUG 01,2005
		CHK	R.R.P. AUG 01,2005
		ENGR	J.T.C. AUG 01,2005
		ENGR-MGR	R.R.P. AUG 01,2005
		QA	C.M.D. AUG 01,2005
		MFG	C.M.D. AUG 01,2005
		ELSE	T.M.K. AUG 01,2005

SPECTRUM DIGITAL INCORPORATED

Title: TMS320C6482 Mezzanine Card

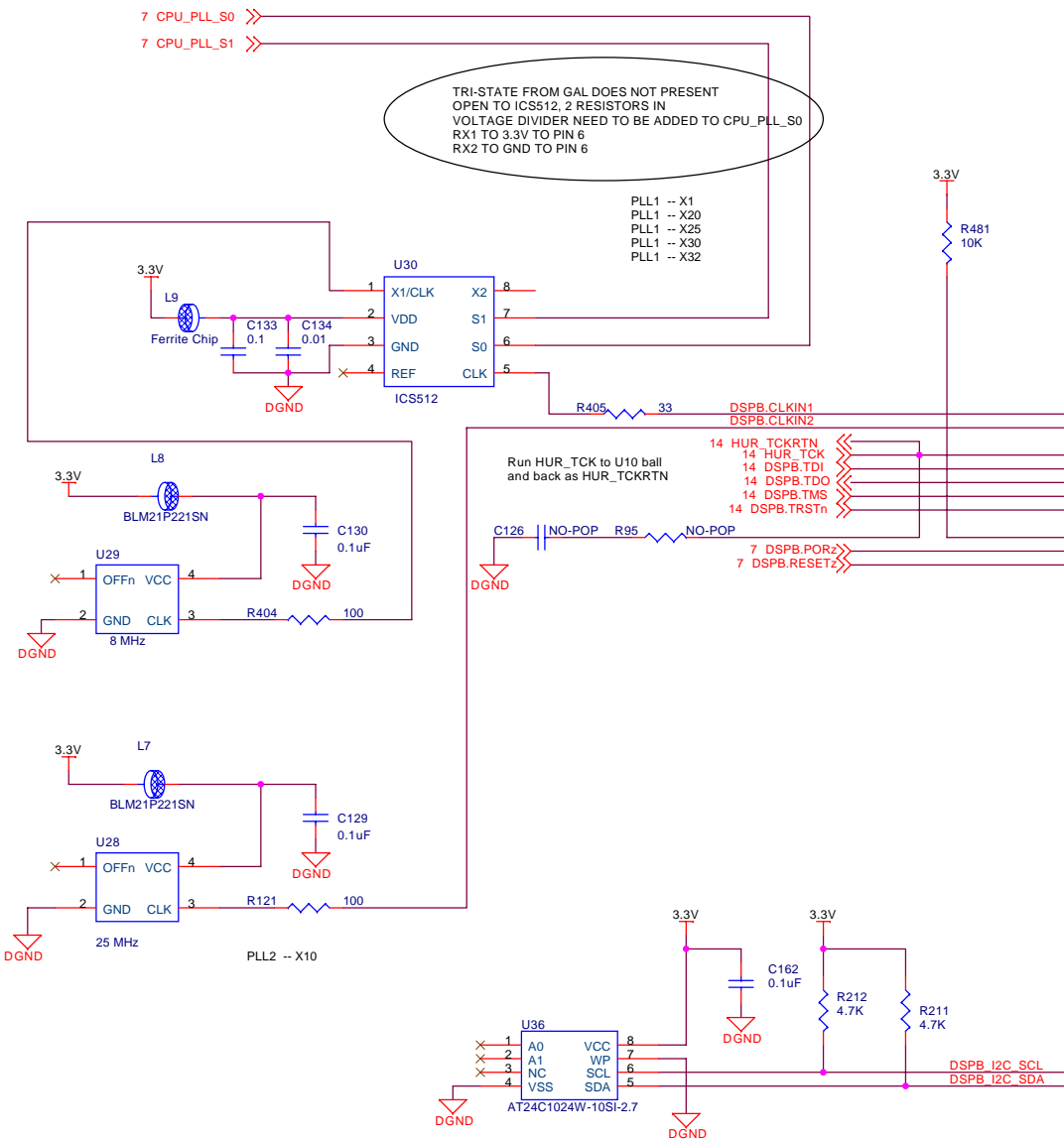
Page Contents: Title Block

Size:B DWG NO 508632-2001

Revision: B

Date: Friday, January 27, 2006

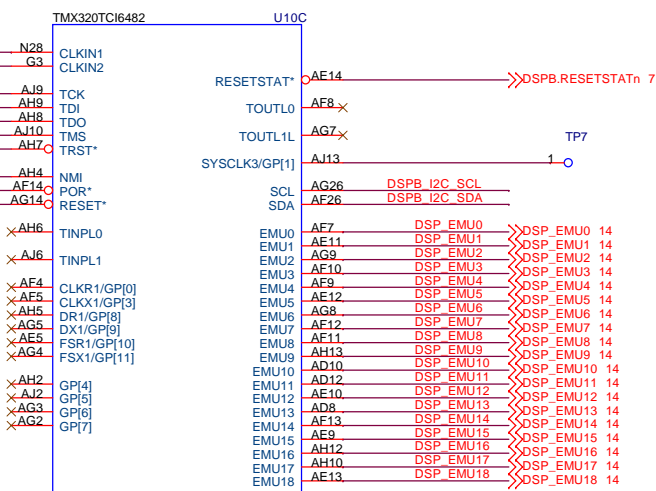
Sheet 1 of 22



8 MHZ INPUT CLOCK

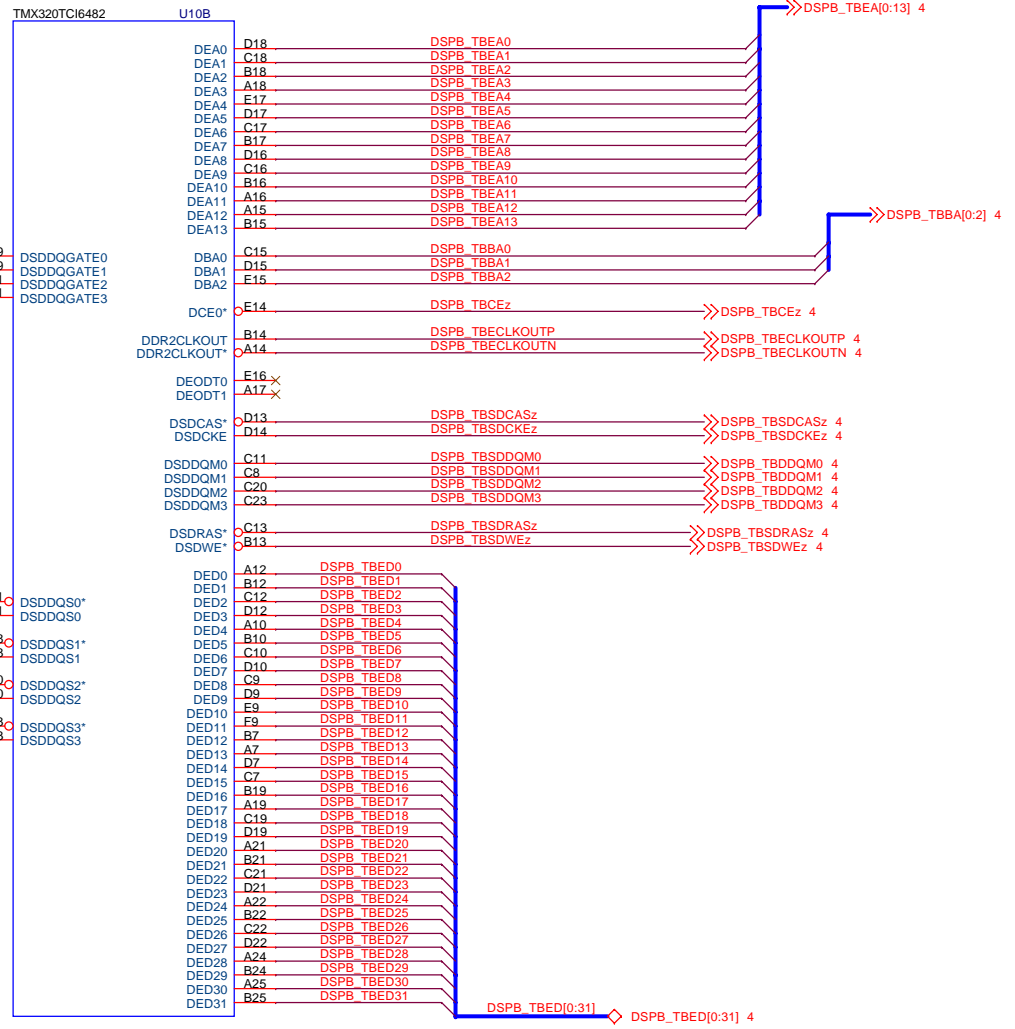
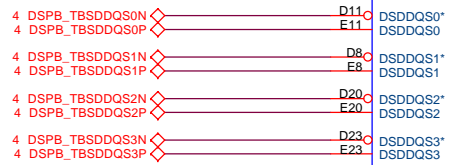
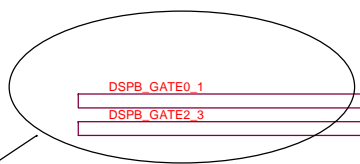
6482 INTERNAL PLL

S1	S0	MULTIPLY	OUTPUT	PLL1 -- X1	PLL1 -- X20	PLL1 -- X25	PLL1 -- X30	PLL1 -- X32
0	0	4X	32	32	640	800	960	1024
0	OPEN	5.33X	42.64	42.64	853	1066	1279	1365
0	1	5X	40	40	800	1000	1200	1280
OPEN	0	2.5X	20	20	400	500	600	640
OPEN	OPEN	2X	16	16	320	400	480	512
OPEN	1	3.33X	26.4	26.4	528	660	792	845
1	0	6X	48	48	960	1200	1440	1536
1	OPEN	3X	24	24	480	600	720	768
1	1	8X	64	64	1280	1600	1920	2048

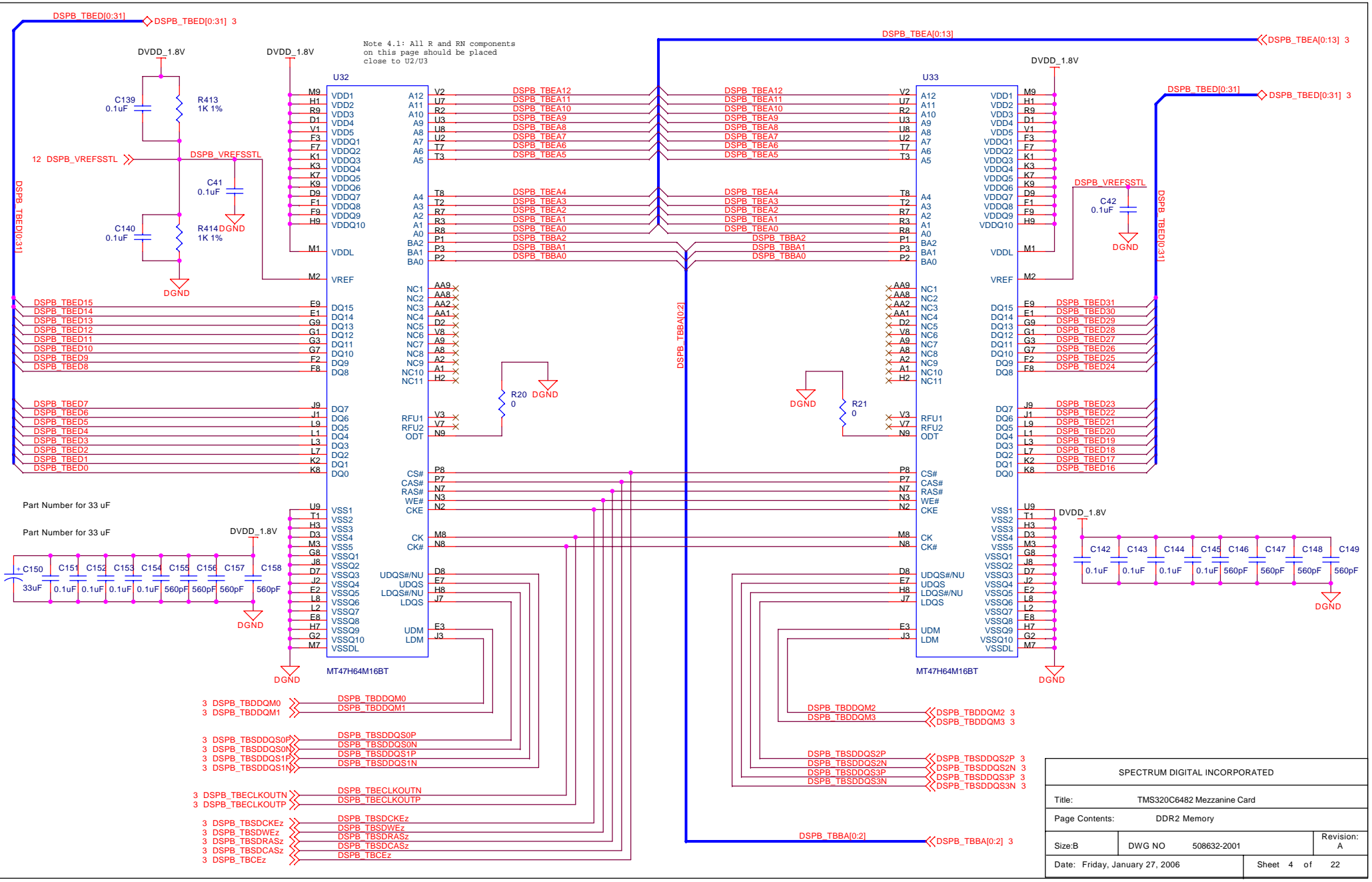


NOTE: Route DSDDQGATE0 signals needs to run to DDR memories near D15-D0 and back to DSDDQGATE1.

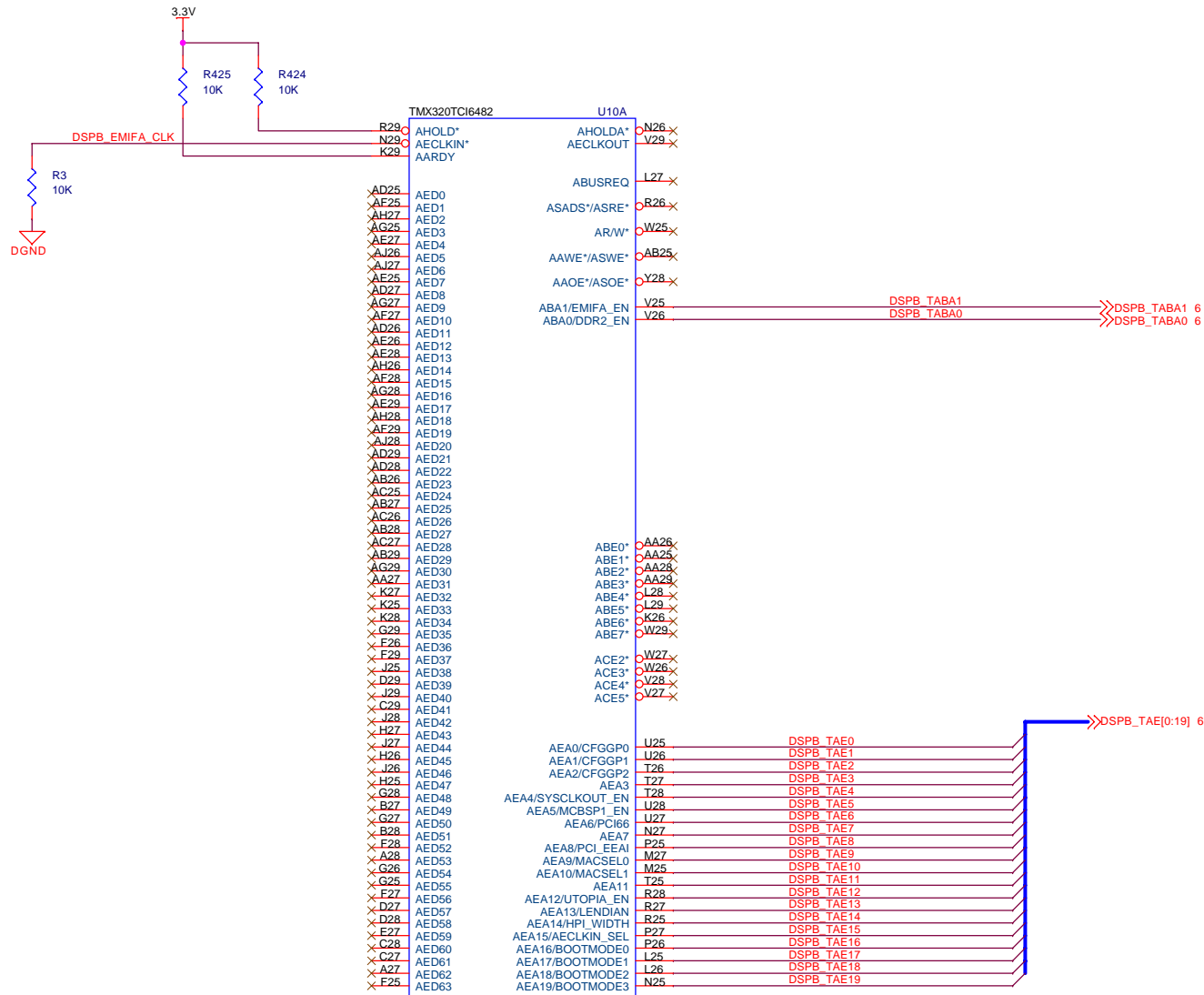
NOTE: Route DSDDQGATE2 signals needs to run to DDR memories near D31-D16 and back to DSDDQGATE3.



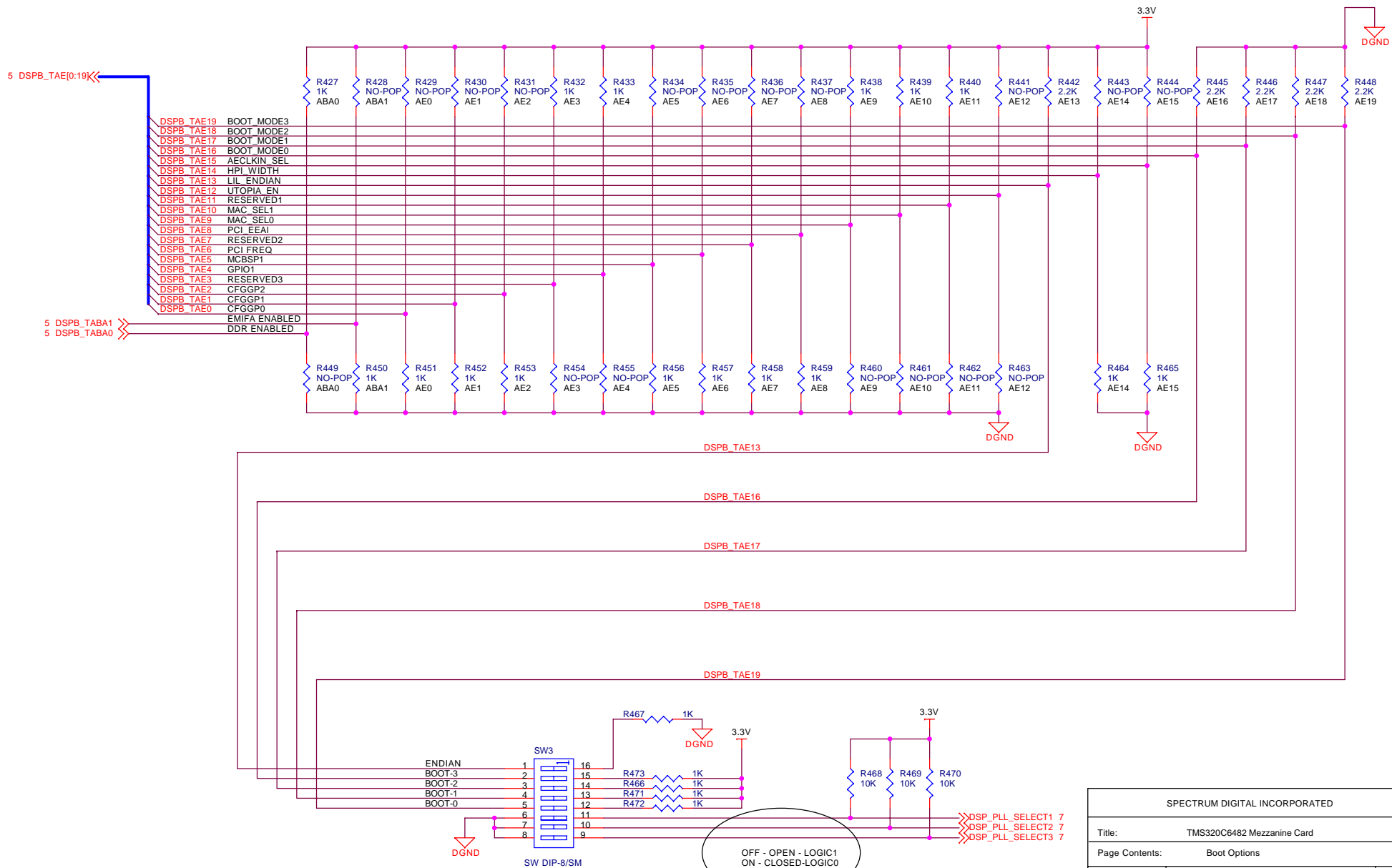
SPECTRUM DIGITAL INCORPORATED			
Title: TMS320C6482 Mezzanine Card			
Page Contents: 6455 DDR Interface			
Size: B	DWG NO	508632-2001	Revision: A
Date: Friday, January 27, 2006		Sheet 3 of 22	



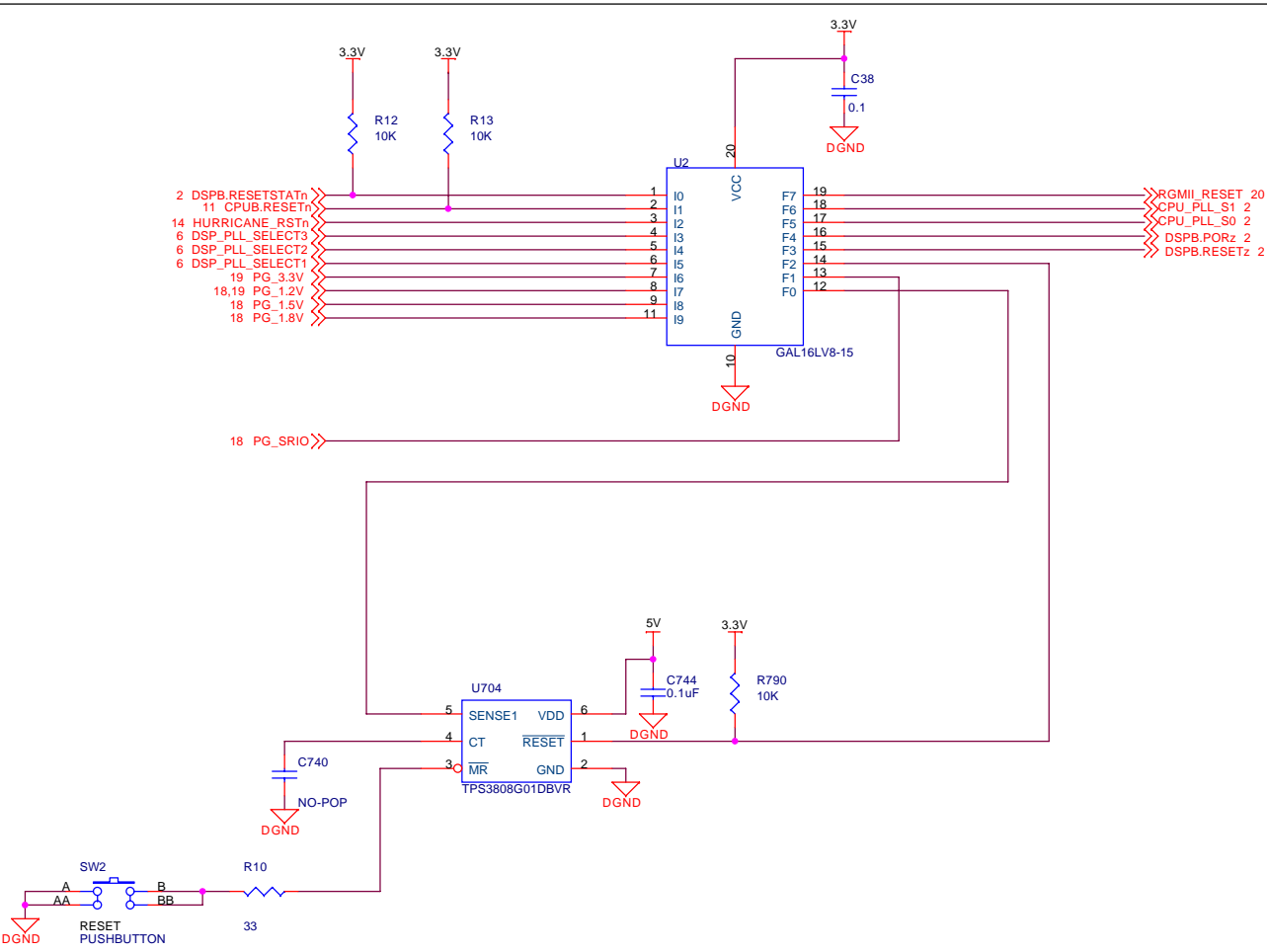
SPECTRUM DIGITAL INCORPORATED			
Title: TMS320C6482 Mezzanine Card			
Page Contents: DDR2 Memory			
Size: B	DWG NO	508632-2001	Revision: A
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SPECTRUM DIGITAL INCORPORATED			
Title:		TMS320C6482 Mezzanine Card	
Page Contents:		6482 Emif A Interface	
Size: B	DWG NO	508632-2001	Revision: A
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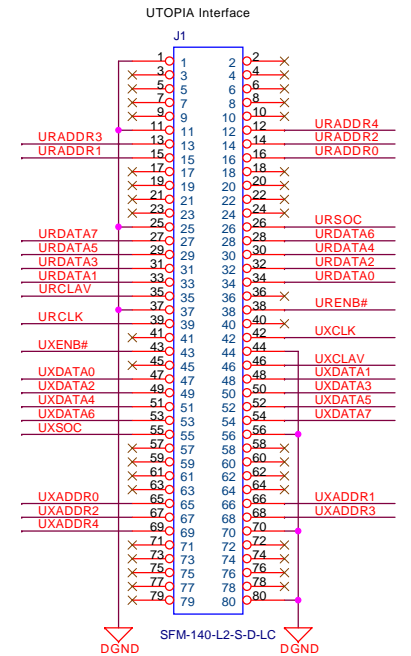
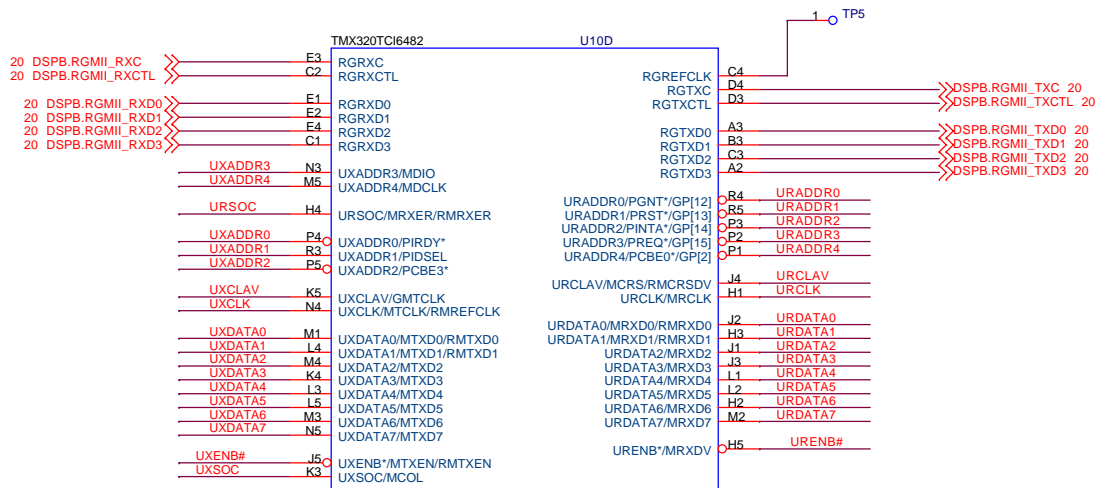


SPECTRUM DIGITAL INCORPORATED		
Title: TMS320C6482 Mezzanine Card		
Page Contents: Boot Options		
Size: B	DWG NO 508632-2001	Revision: A
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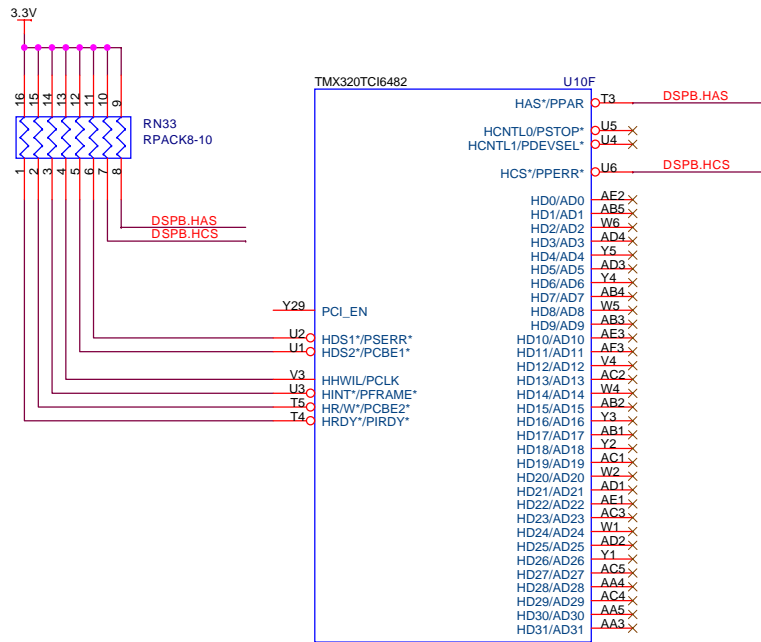


FROM USER SWITCH			CODE TO ICS512		6482 INTERNAL PLL						
PLL_SEL3	PLL_SEL2	PLL_SEL0	CPU_PLL_S0	CPU_PLL_S0	ICS MULTIPLY	DSP_IN_CLK	PLL1 -- X1	PLL1 -- X20	PLL1 -- X25	PLL1 -- X30	PLL1 -- X32
0	0	0	0	1	5	40	40	800	1000	1200	1280
0	0	1	0	1	5	40	40	800	1000	1200	1280
0	1	0	0	1	5	40	40	800	1000	1200	1280
0	1	1	0	1	8	64	64				
1	0	0	0	OPEN	5.33	42.64	42.64	853	1066	1279	1365
1	0	1	0	OPEN	5.33	42.64	42.64	853	1066	1279	1365
1	1	0	0	OPEN	5.33	42.64	42.64	853	1066	1279	1365
1	1	1	1	OPEN	3	24	24	480	600	720	768

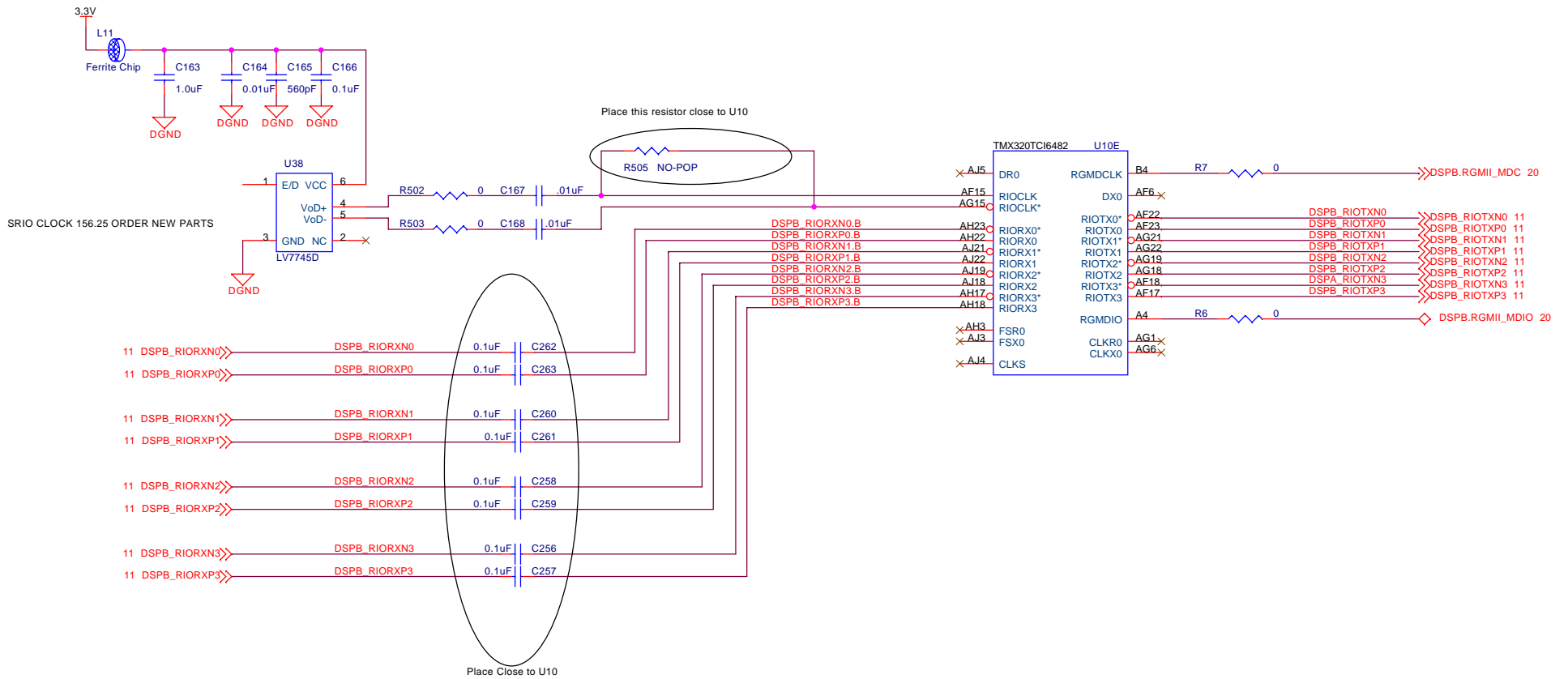
SPECTRUM DIGITAL INCORPORATED		
Title: TMS320C6482 Mezzanine Card		
Page Contents: CPLD INTERFACE		
Size: B	DWG NO 508632-2001	Revision: A
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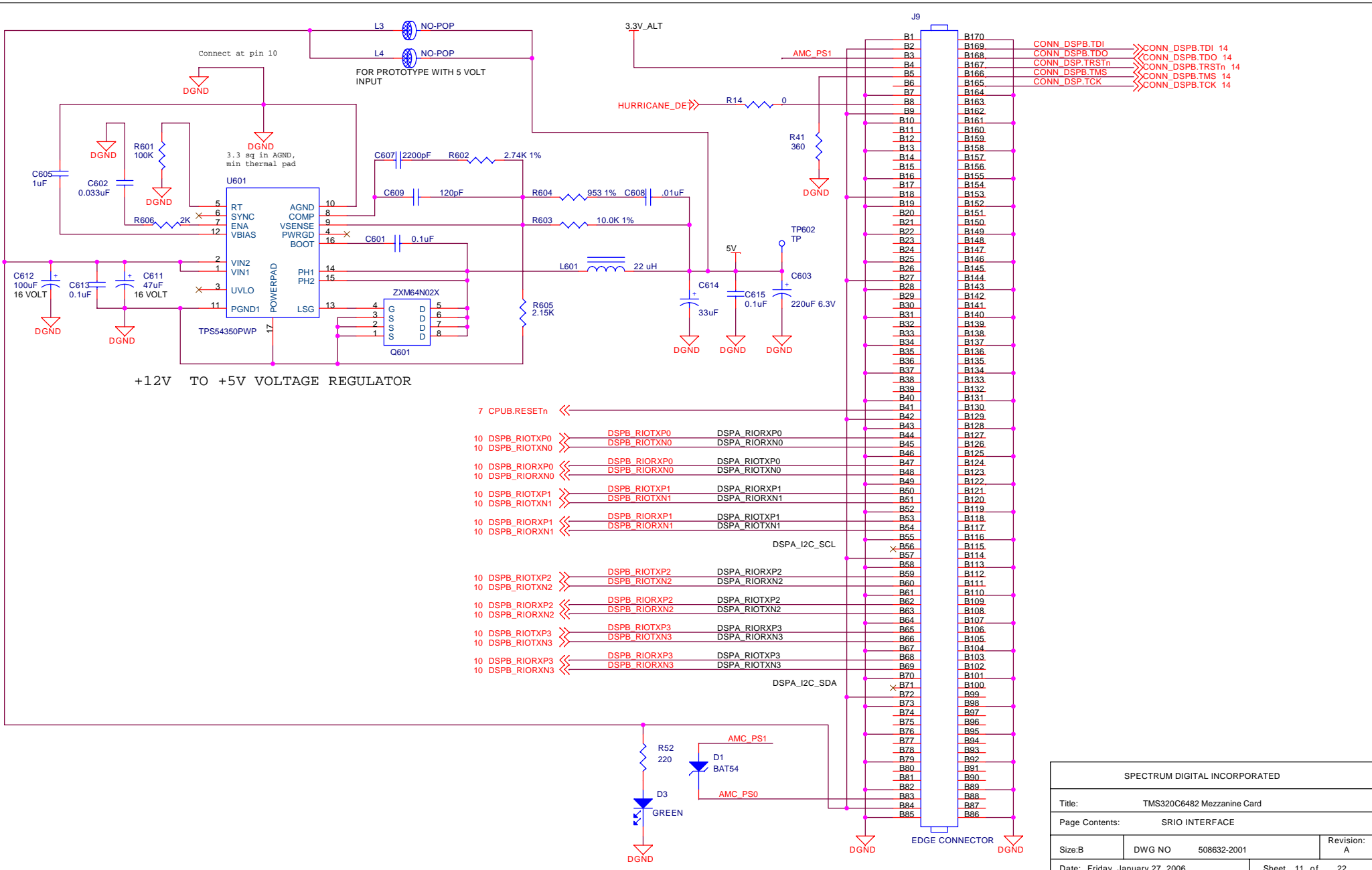
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Title: TMS320C6482 Mezzanine Card			
Page Contents: UTOPIA Interface			
Size: B	DWG NO	508632-2001	Revision: A
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SPECTRUM DIGITAL INCORPORATED			
Title:		TMS320C6482 Mezzanine Card	
Page Contents:		PCI/HOST PORT INTERFACE	
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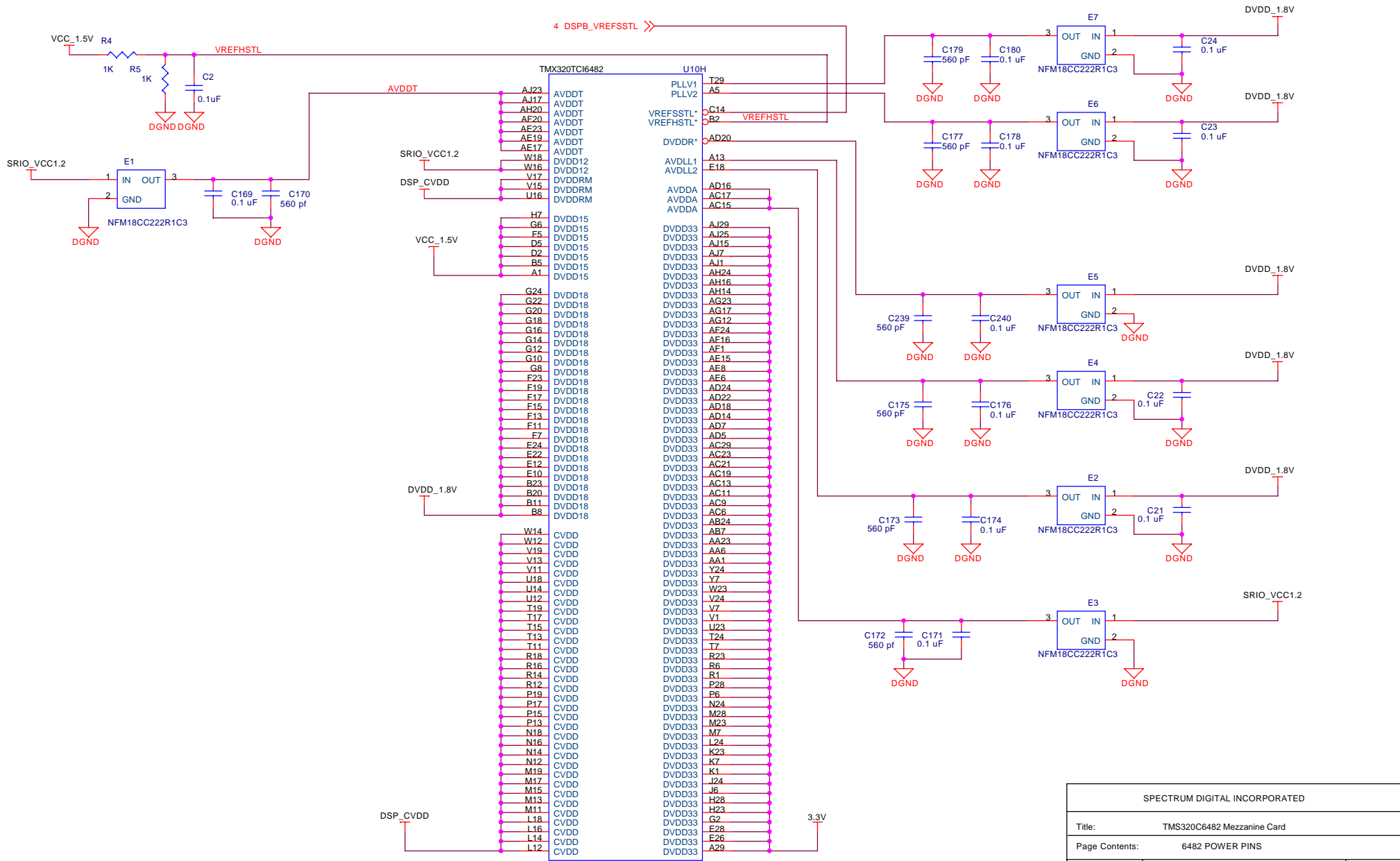


SPECTRUM DIGITAL INCORPORATED			
Title: TMS320C6482 Mezzanine Card			
Page Contents: SRIO INTERFACE			
Size: B	DWG NO	508632-2001	Revision: A
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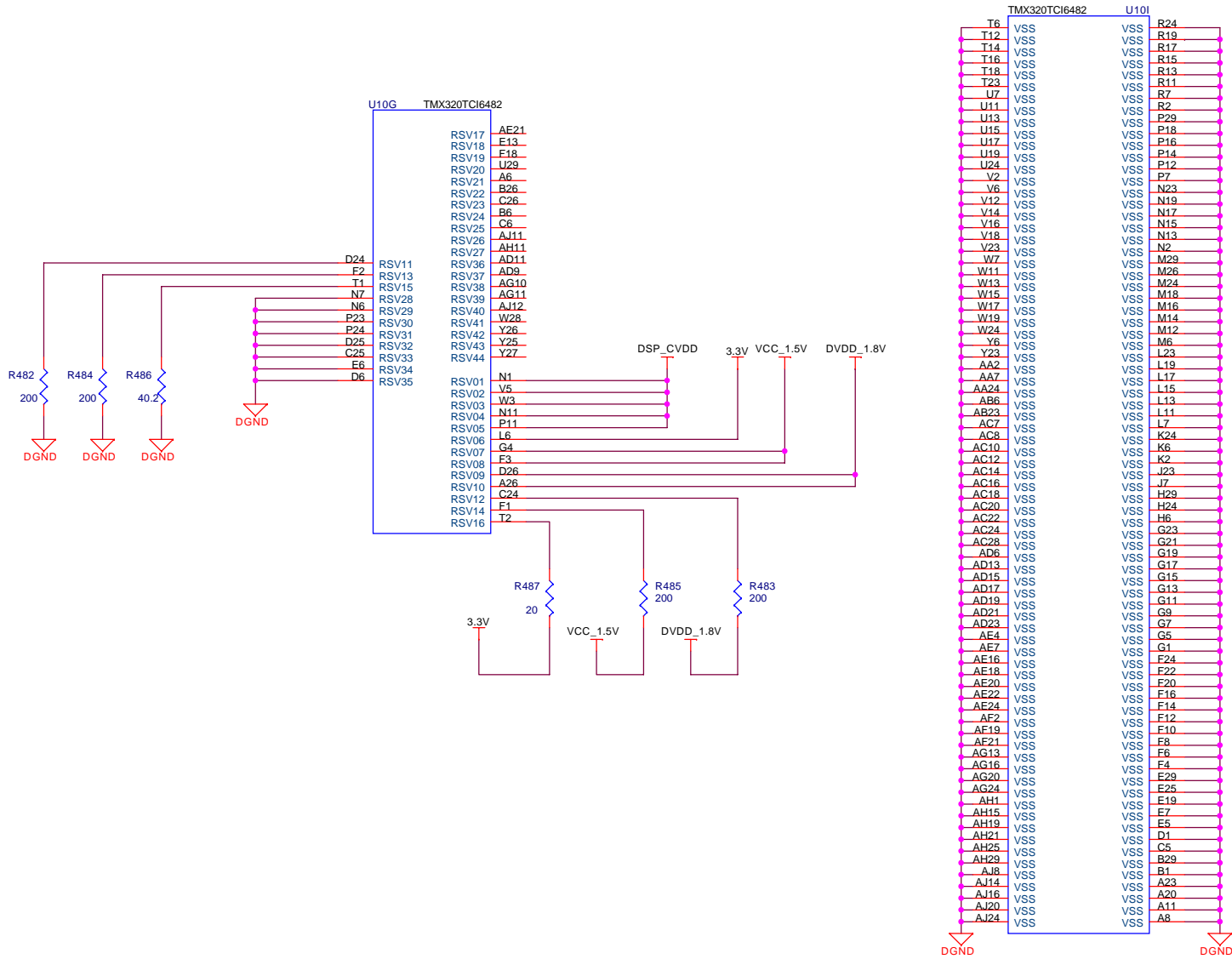


CONN_DSPB.TDI >>> CONN_DSPB.TDI 14
 CONN_DSPB.TDO >>> CONN_DSPB.TDO 14
 CONN_DSP.TRSTn >>> CONN_DSP.TRSTn 14
 CONN_DSPB.TMS >>> CONN_DSPB.TMS 14
 CONN_DSP.TCK >>> CONN_DSP.TCK 14

SPECTRUM DIGITAL INCORPORATED		
Title: TMS320C6482 Mezzanine Card		
Page Contents: SRIO INTERFACE		
Size: B	DWG NO 508632-2001	Revision: A
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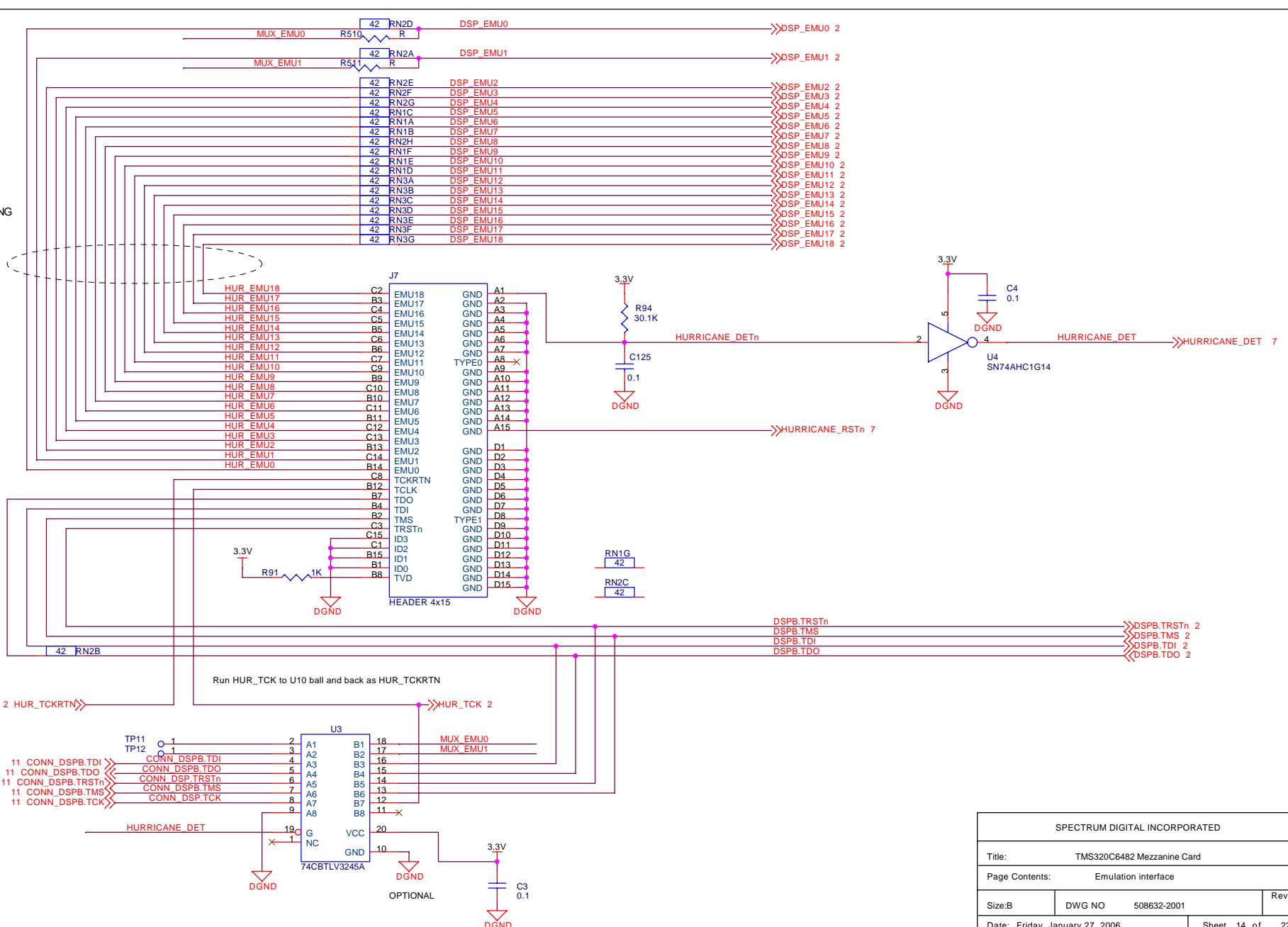


SPECTRUM DIGITAL INCORPORATED			
Title: TMS320C6482 Mezzanine Card			
Page Contents: 6482 POWER PINS			
Size: B	DWG NO	508632-2001	Revision: A
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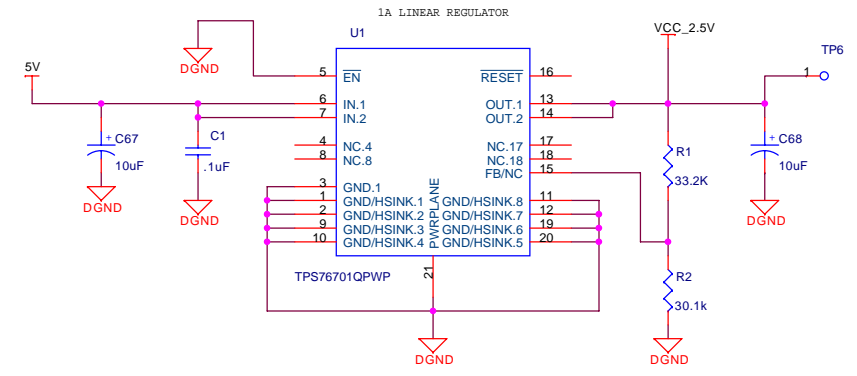
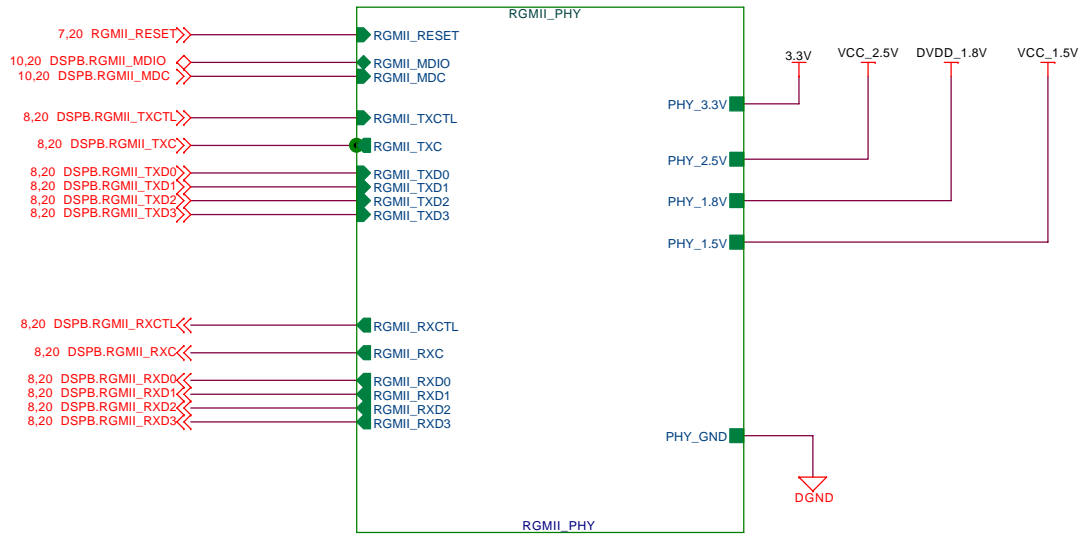


SPECTRUM DIGITAL INCORPORATED			
Title: TMS320C6482 Mezzanine Card			
Page Contents: 6482 POWER PINS			
Size: B	DWG NO	508632-2001	Revision: A
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ROUTE TRACES AS ONE GROUP.
MATCH SIGNAL LENGTH.
USE 2X TRACE WIDTH SPACING BETWEEN ROUTES



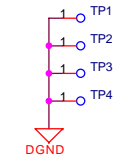
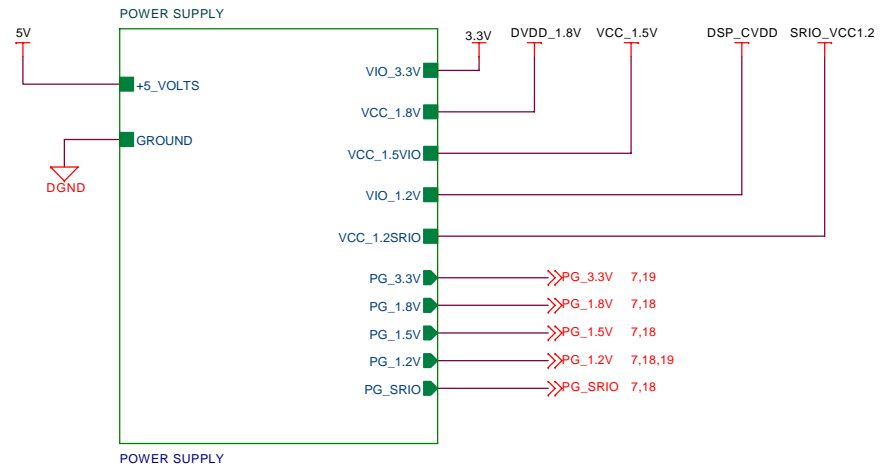
SPECTRUM DIGITAL INCORPORATED			
Title: TMS320C6482 Mezzanine Card			
Page Contents: Emulation interface			
Size: B	DWG NO	508632-2001	Revision: A
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$$V_{out} = V_{REF} * (1 + R1/R2)$$

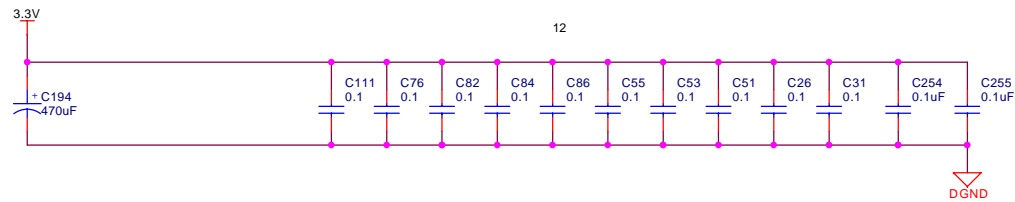
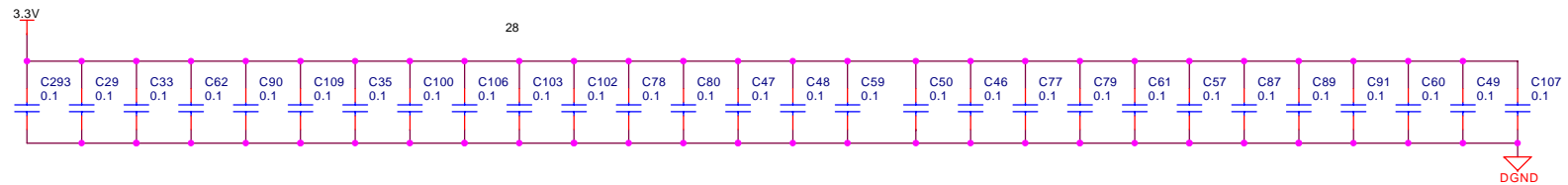
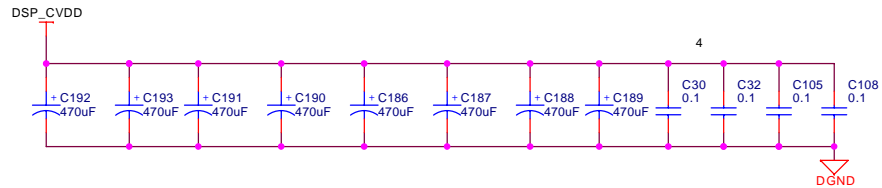
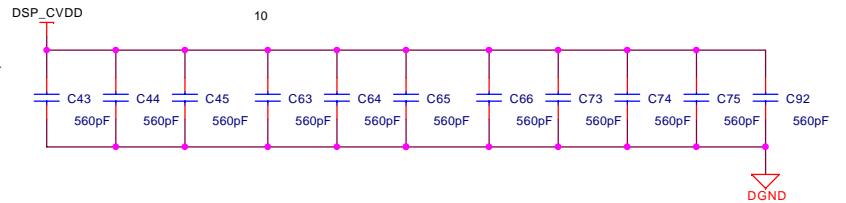
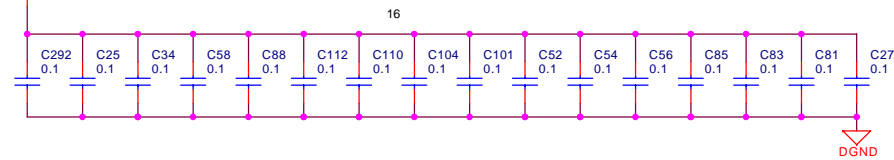
$$V_{REF} = 1.1834$$

$$V_{out} = 2.5V$$

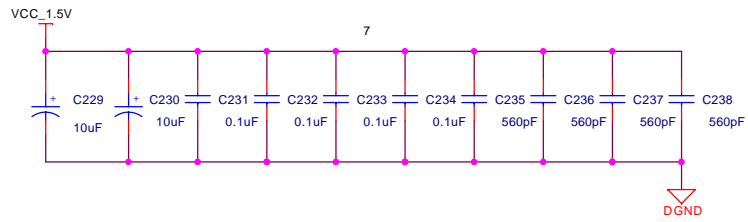
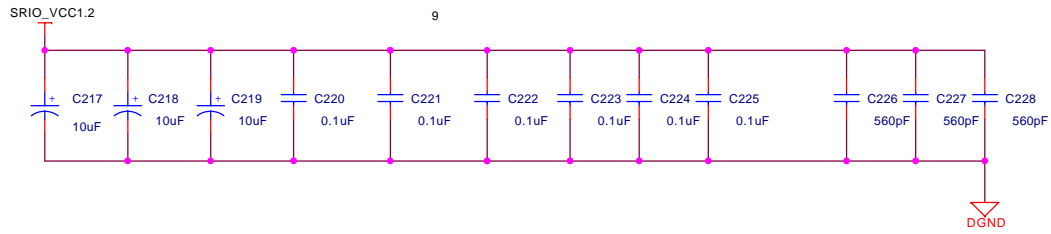
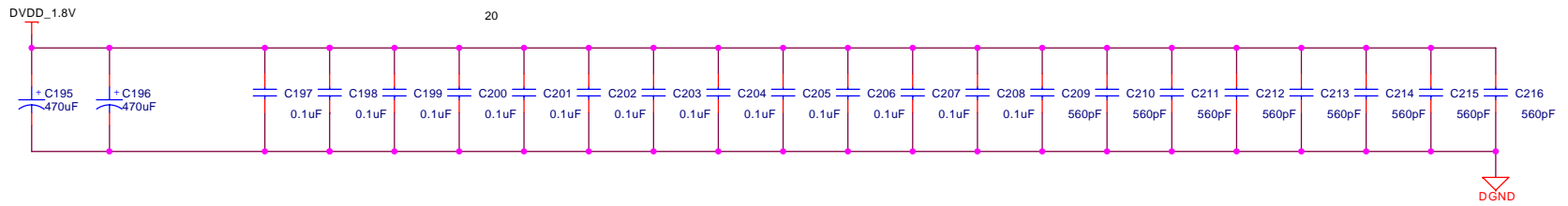


SPECTRUM DIGITAL INCORPORATED			
Title: TMS320C6482 Mezzanine Card			
Page Contents: Hierarchical Blocks			
Size: B	DWG NO: 508632-2001	Revision: A	
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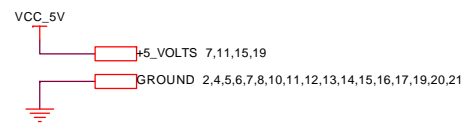
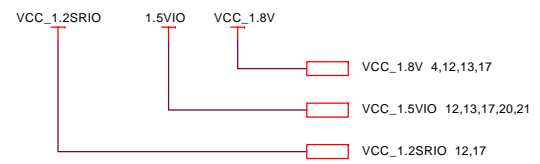
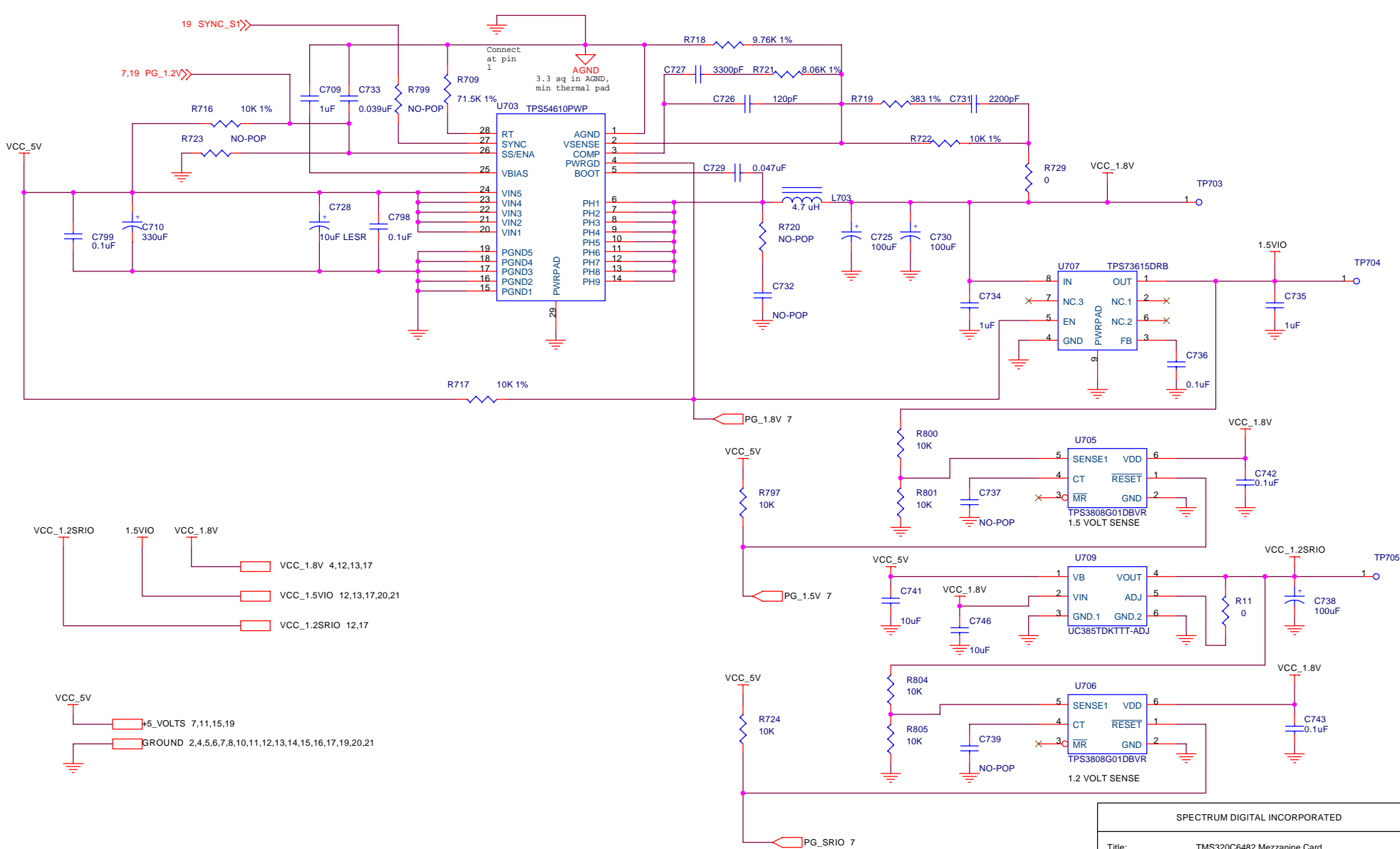
DSP_CVDD All capacitors on this sheet are decoupling capacitors for the DSP. They should be placed as close as possible to the DSP.



SPECTRUM DIGITAL INCORPORATED			
Title:		TMS320C6482 Mezzanine Card	
Page Contents:		Decoupling Capacitors	
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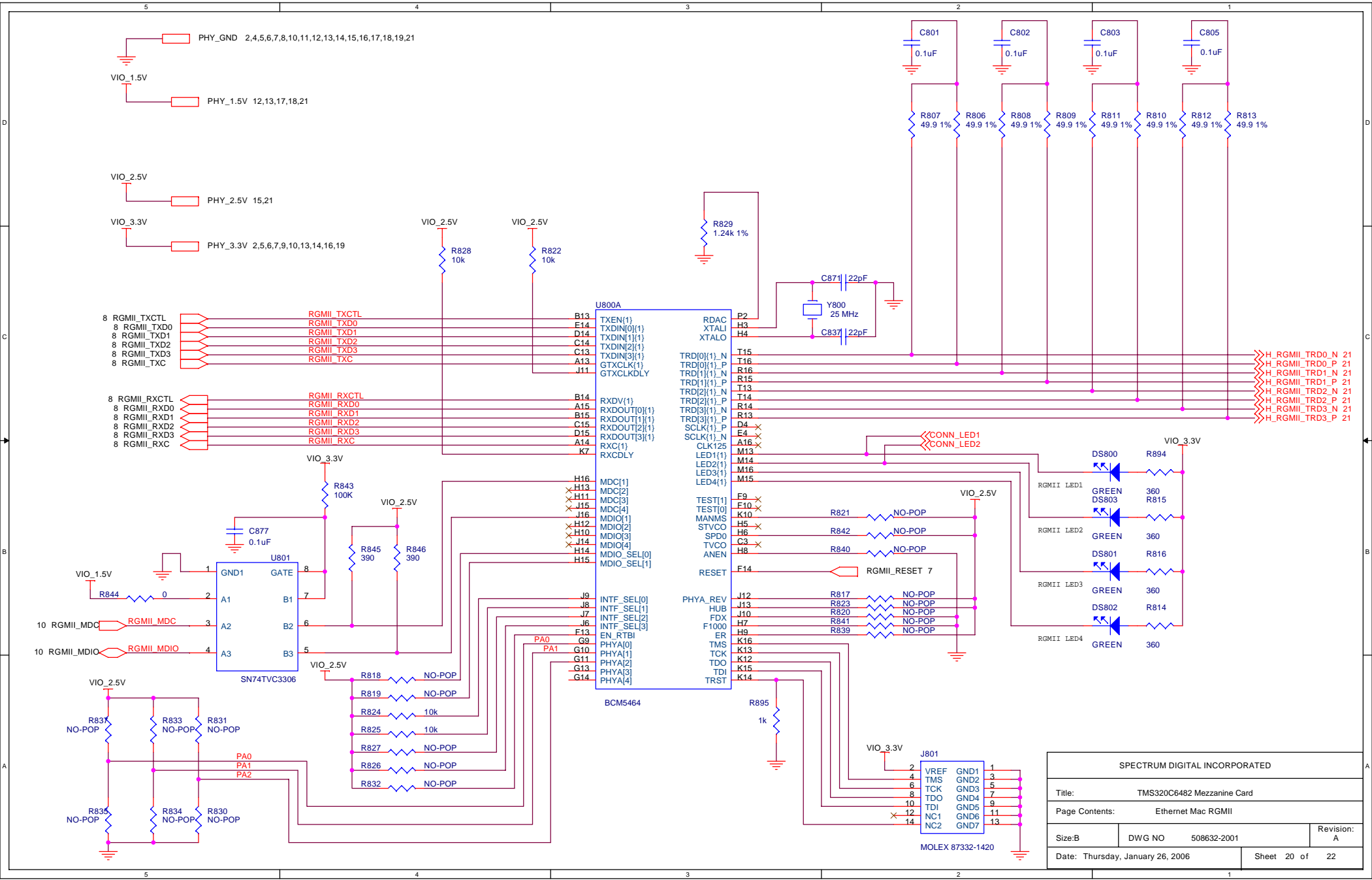
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Title:		TMS320C6482 Mezzanine Card	
Page Contents:		Decoupling Capacitors	
Size: B	DWG NO	508632-2001	Revision: A
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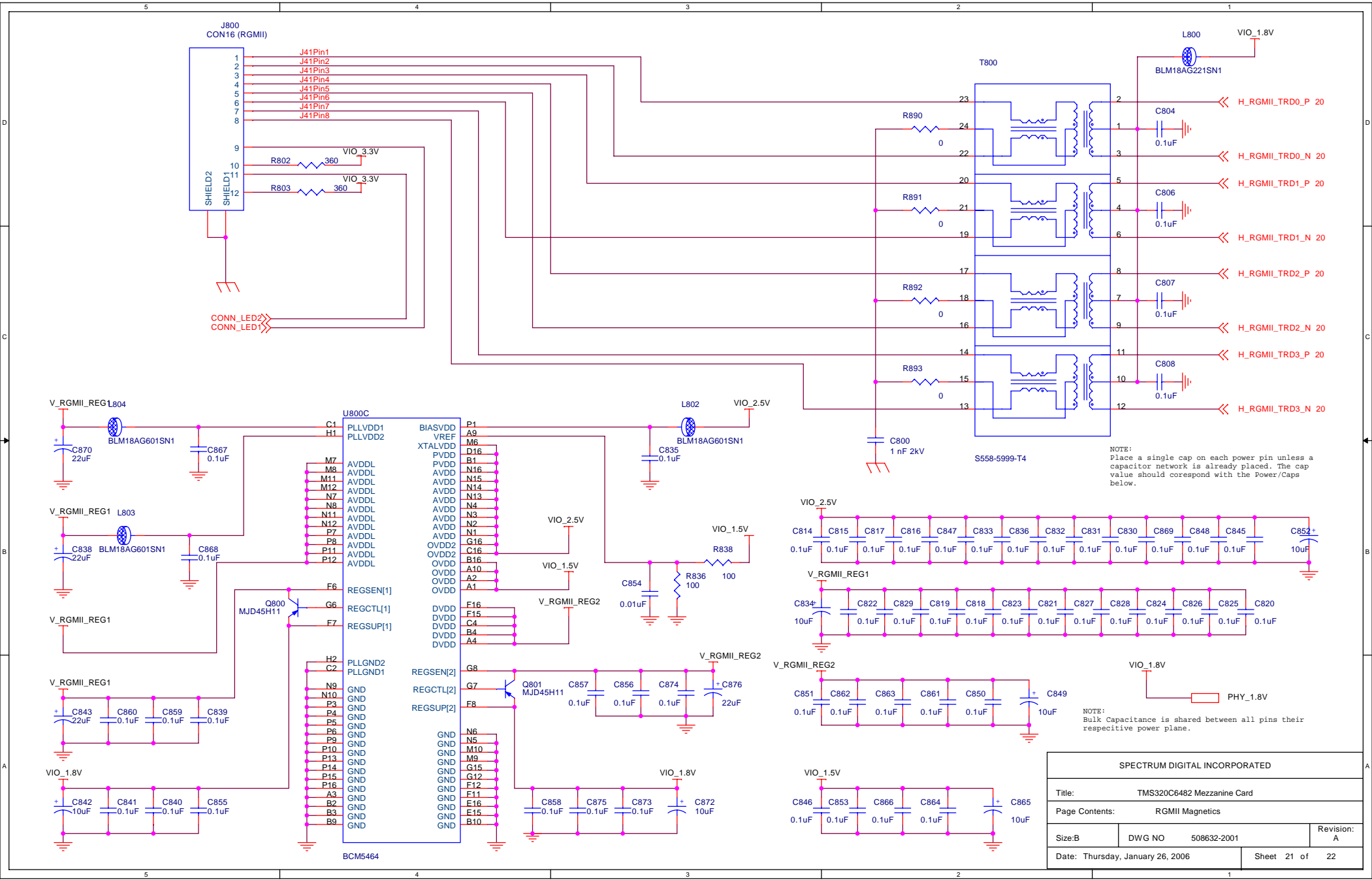
SPECTRUM DIGITAL INCORPORATED			
Title: TMS320C6482 Mezzanine Card			
Page Contents: POWER SUPPLY			
Size: B	DWG NO	508632-2001	Revision: A
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SPECTRUM DIGITAL INCORPORATED			
Title: TMS320C6482 Mezzanine Card			
Page Contents: POWER SUPPLY			
Size: B	DWG NO	508632-2001	Revision: A
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SPECTRUM DIGITAL INCORPORATED			
Title: TMS320C6482 Mezzanine Card			
Page Contents: Ethernet Mac RGMII			
Size: B	DWG NO	508632-2001	Revision: A
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SPECTRUM DIGITAL INCORPORATED			
Title: TMS320C6482 Mezzanine Card			
Page Contents: RGMII Magnetics			
Size: B	DWG NO: 508632-2001	Revision: A	
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U800B			
A7	GTCLK(3)	TRD(0)(2)_N	R10
A11	GTCLK(2)	TRD(0)(2)_P	R9
A5	GTCLK(4)	TRD(0)(3)_N	T7
A12	RXC(2)	TRD(0)(3)_P	T8
A8	RXC(3)	TRD(0)(4)_P	R2
A6	RXC(4)	TRD(1)(2)_N	R1
D13	RXD(0)(2)	TRD(1)(2)_P	T9
C10	RXD(0)(3)	TRD(1)(3)_N	T10
E6	RXD(0)(4)	TRD(1)(3)_P	R8
E13	RXD(1)(2)	TRD(1)(4)_N	R7
D16	RXD(1)(3)	TRD(2)(2)_N	T1
E7	RXD(1)(4)	TRD(2)(2)_P	T2
D12	RXD(2)(2)	TRD(2)(3)_N	R12
E10	RXD(2)(3)	TRD(2)(3)_P	R11
D7	RXD(2)(4)	TRD(2)(4)_N	T5
C12	RXD(3)(2)	TRD(2)(4)_P	T6
D9	RXD(3)(3)	TRD(3)(2)_N	R4
C7	RXD(3)(4)	TRD(3)(2)_P	R3
B12	RXD(4)	TRD(3)(3)_N	T11
C9	TXD(1)(2)	TRD(3)(3)_P	T12
B7	TXD(1)(3)	TRD(3)(4)_N	R6
E12	TXD(1)(4)	TRD(3)(4)_P	R5
E9	TXD(2)(2)	SGIN(1)+	T3
B5	TXD(2)(3)	SGIN(1)-	T4
E11	TXD(2)(4)	SGIN(2)+	D1
E8	TXD(3)(2)	SGIN(2)-	F1
C5	TXD(3)(3)	SGIN(3)+	F1
D11	TXD(3)(4)	SGIN(3)-	G1
D8	TXD(4)	SGIN(4)+	K1
D6	TXD(4)+	SGIN(4)-	J1
C11	TXD(4)+	SGOUT(1)-	M1
C8	TXEN(2)	SGOUT(2)+	L1
B6	TXEN(3)	SGOUT(2)-	F5
B11	TXEN(4)	SGOUT(3)+	D5
B8	SCLK(4)_P	SGOUT(3)-	G5
L4	SCLK(4)_N	SGOUT(4)+	F5
M4	SCLK(3)_P	SGOUT(4)-	K5
K4	SCLK(3)_N	DNC	J5
F4	SCLK(2)_P	DNC	M5
G4	SCLK(2)_N	DNC	L5
L9	LED1(2)	DNC	F2
L15	LED1(3)	DNC	E3
K6	LED1(4)	DNC	F2
L10	LED2(2)	DNC	K8
L13	LED2(3)	DNC	K9
L18	LED2(4)	DNC	K11
L11	LED3(2)	DNC	D2
L16	LED3(3)	DNC	D3
L7	LED3(4)	DNC	F3
L12	LED4(2)	DNC	G2
L14	LED4(3)	DNC	G3
L8	LED4(4)	DNC	J2
M3	DNC	DNC	J3
M2	DNC	DNC	K2
L3	DNC	DNC	K3
			L2

BCM5464

SPECTRUM DIGITAL INCORPORATED			
Title: TMS320C6482 Mezzanine Card			
Page Contents: Ethernet Mac RGMII- Not used			
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