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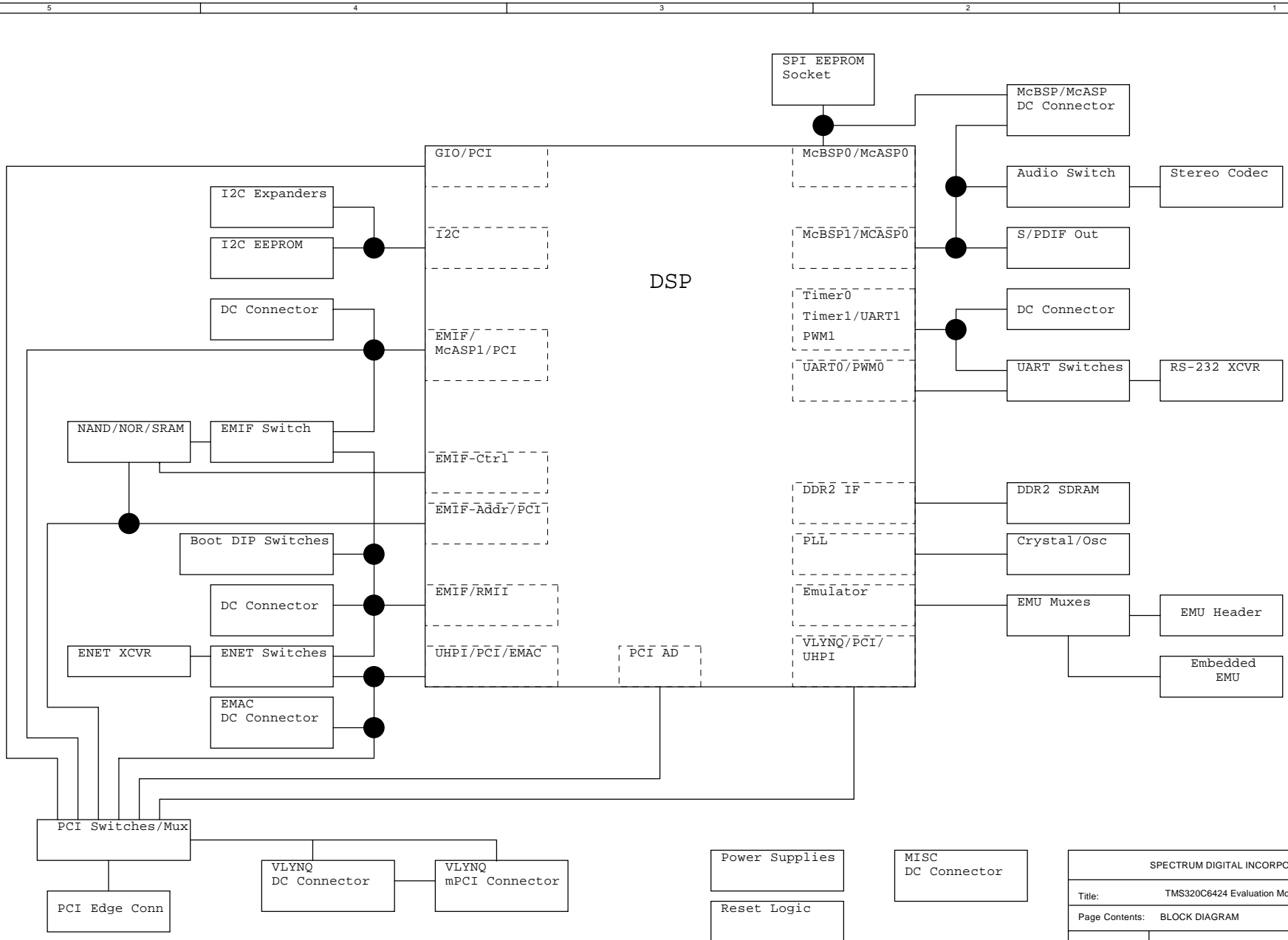
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I2C Address Table			
ADDRESS		DEVICE	FUNCTION
HEX	BINARY		
0x38	00111000B	PCF8574	USER INPUT Expander - 0111(A2)(A1)(A0)
0x39	00111001B	PCF8574	LED Expander - 0111(A2)(A1)(A0)
0x3A	00111010B	PCF8574	IO Expander - 0111(A2)(A1)(A0)
0x3B	00111011B	PCF8574	IO Expander - 0111(A2)(A1)(A0)
0x50	01010000B	CAT24C256	EEPROM - 1010(A2)(A1)(A0)
0x1B	00011011B	AIC33	AUDIO CODEC - 00110(MFP1)(MFP0)

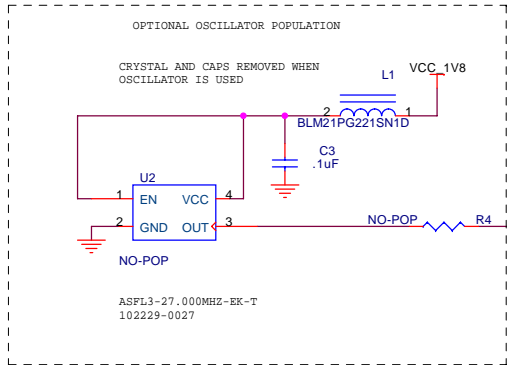
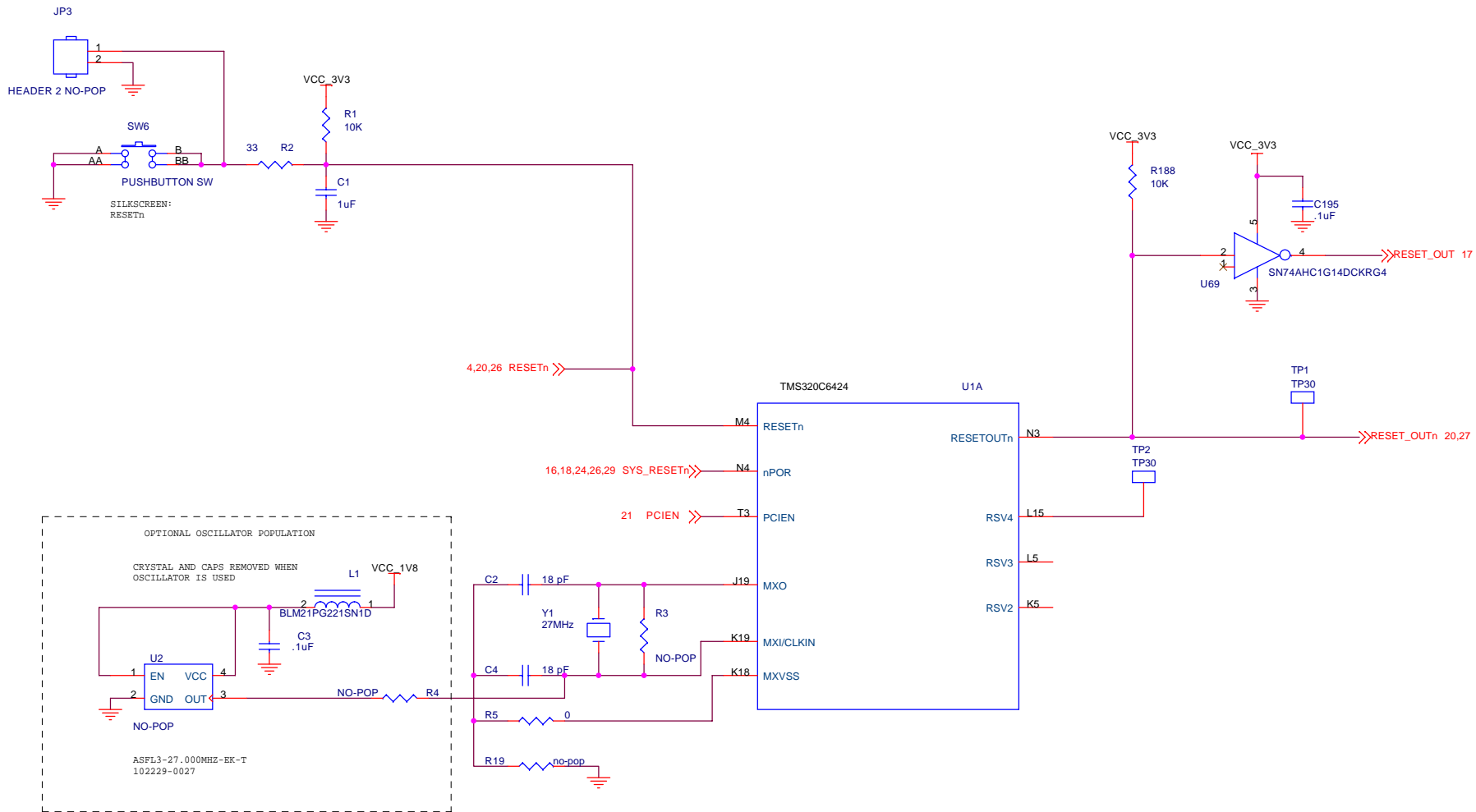
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REV										
SH										
REV	A	A	A	A	A	A	A	A	A	A
SH	21	22	23	24	25	26	27	28	29	30
REV	A	A	A	A	A	A	A	A	A	A
SH	11	12	13	14	15	16	17	18	19	20
REV	A	A	A	A	A	A	A	A	A	A
SH	1	2	3	4	5	6	7	8	9	10

REV	SH	DATE	BY	APP	DESCRIPTION
		06/01/2006	R.R.P.	DWN	
		06/01/2006	T.W.K.	CHK	
		06/01/2006	R.R.P.	ENGR	
		06/01/2006	R.R.P.	ENGR-MGR	
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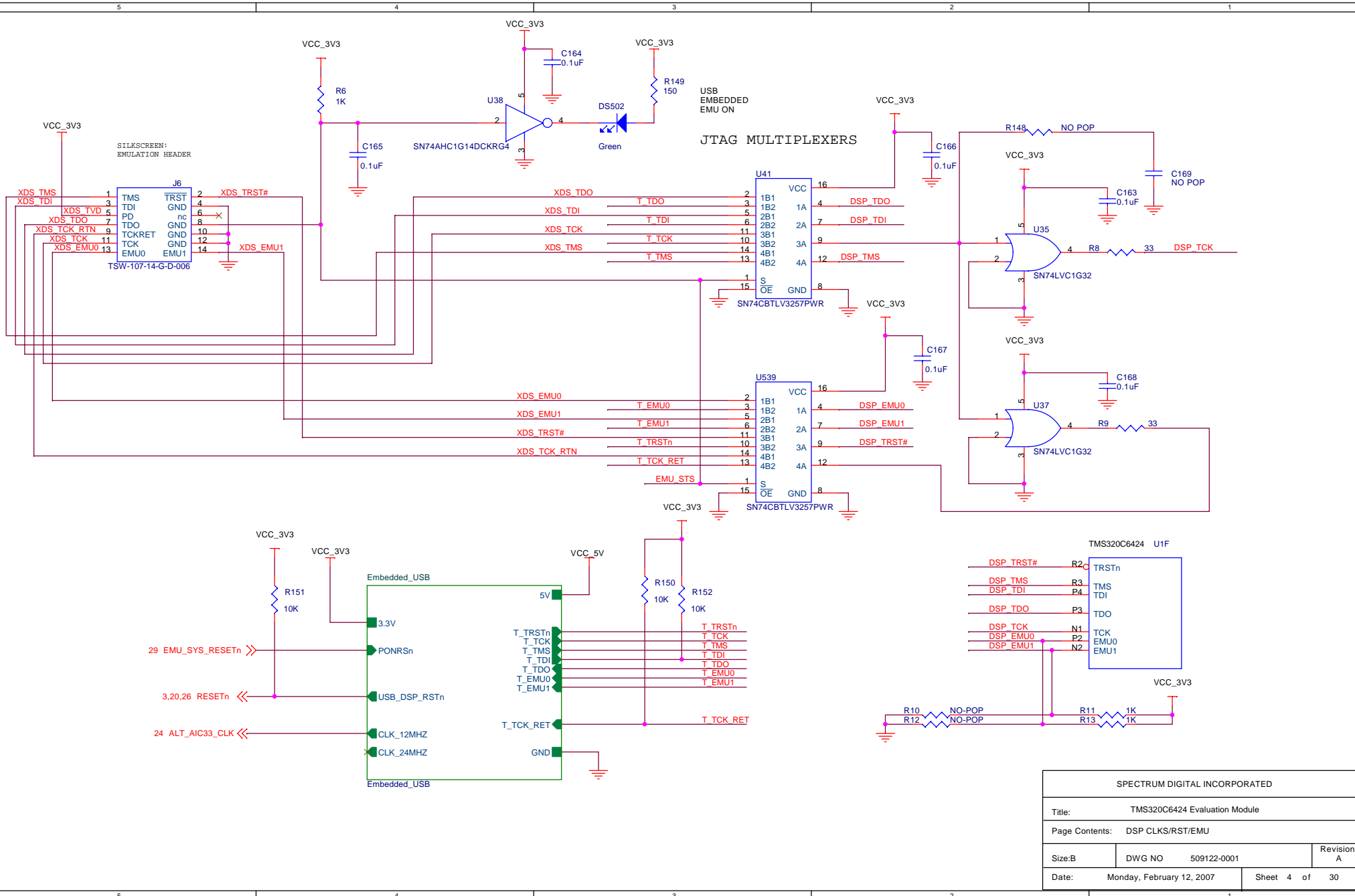
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Page Contents: TITLE SHEET			
Size: B	DWG NO	509122-0001	Revision: A
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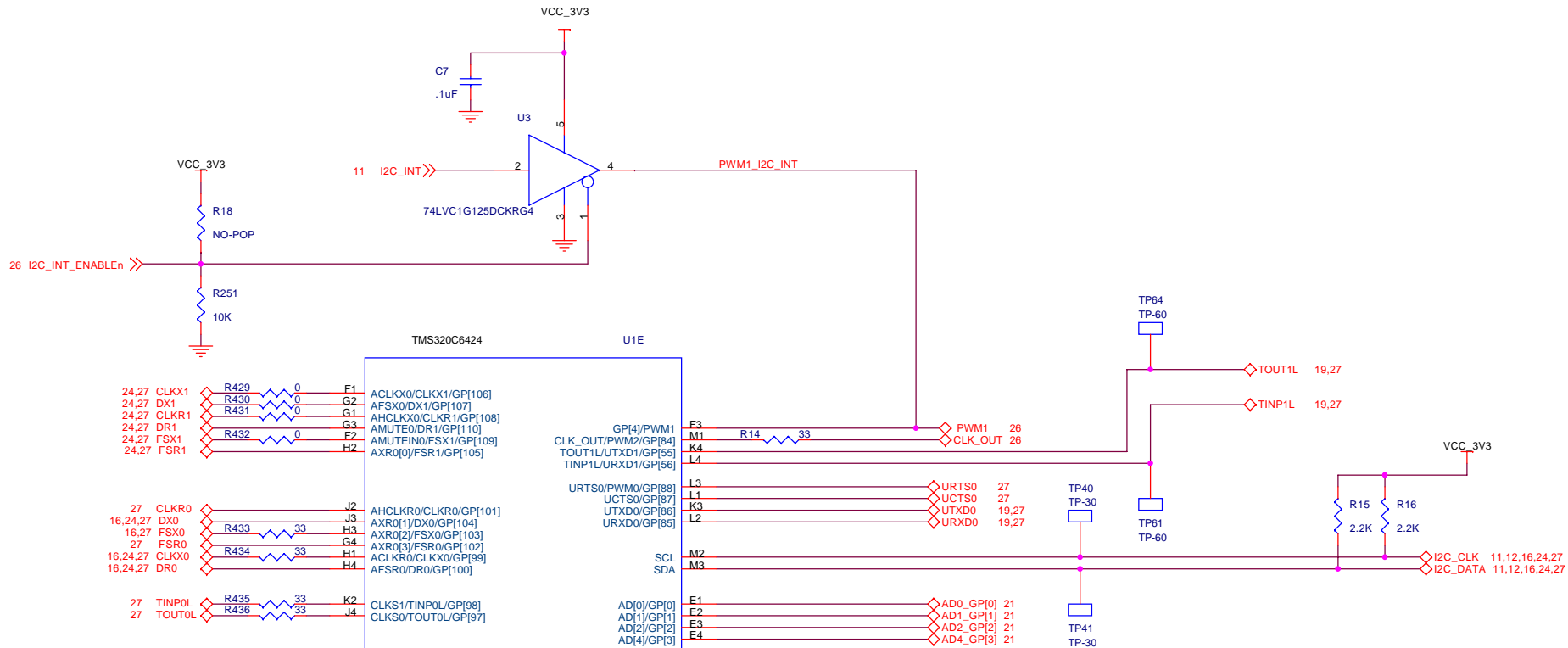
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Page Contents: BLOCK DIAGRAM			
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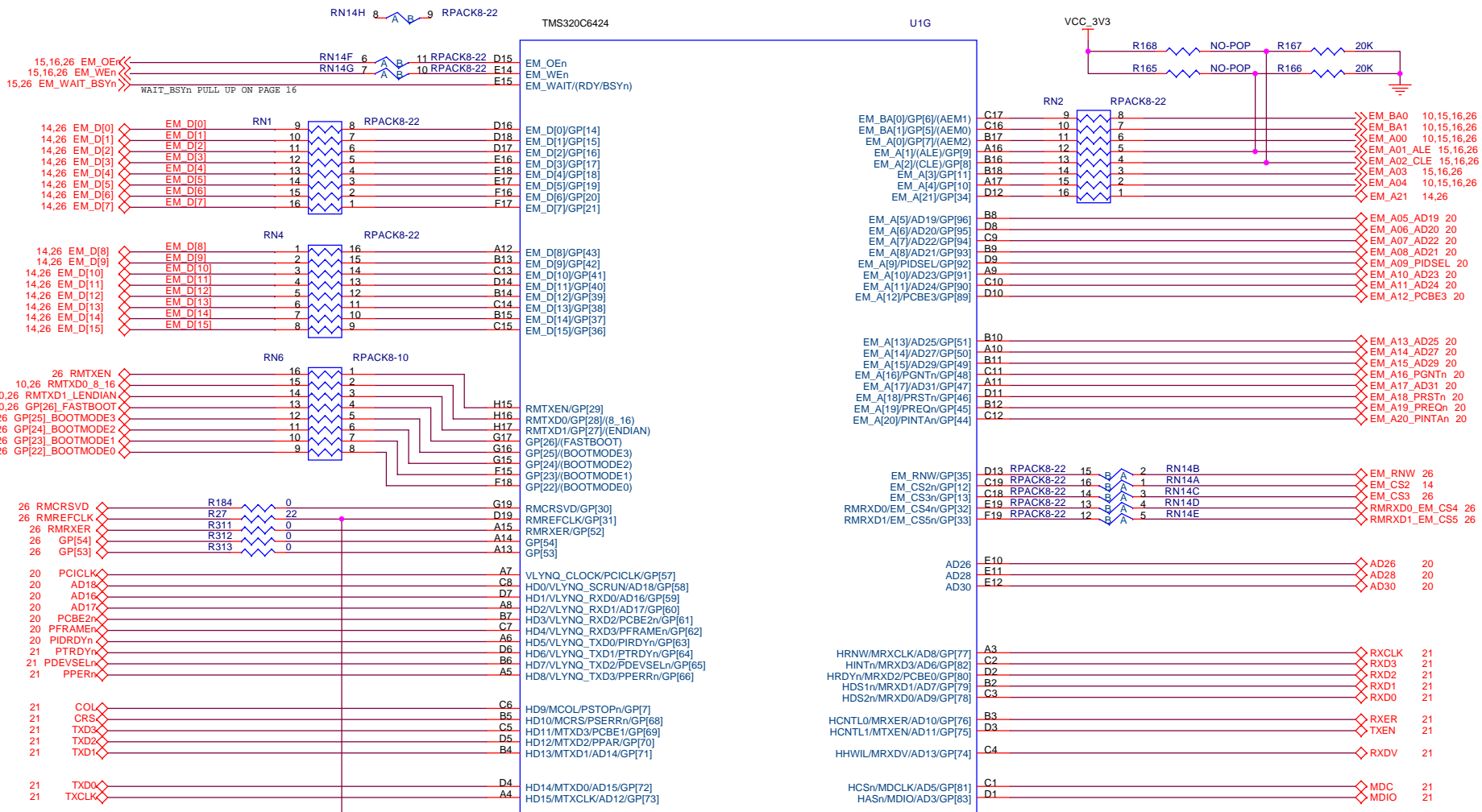
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Page Contents: DSP CLKS/RST/EMU			
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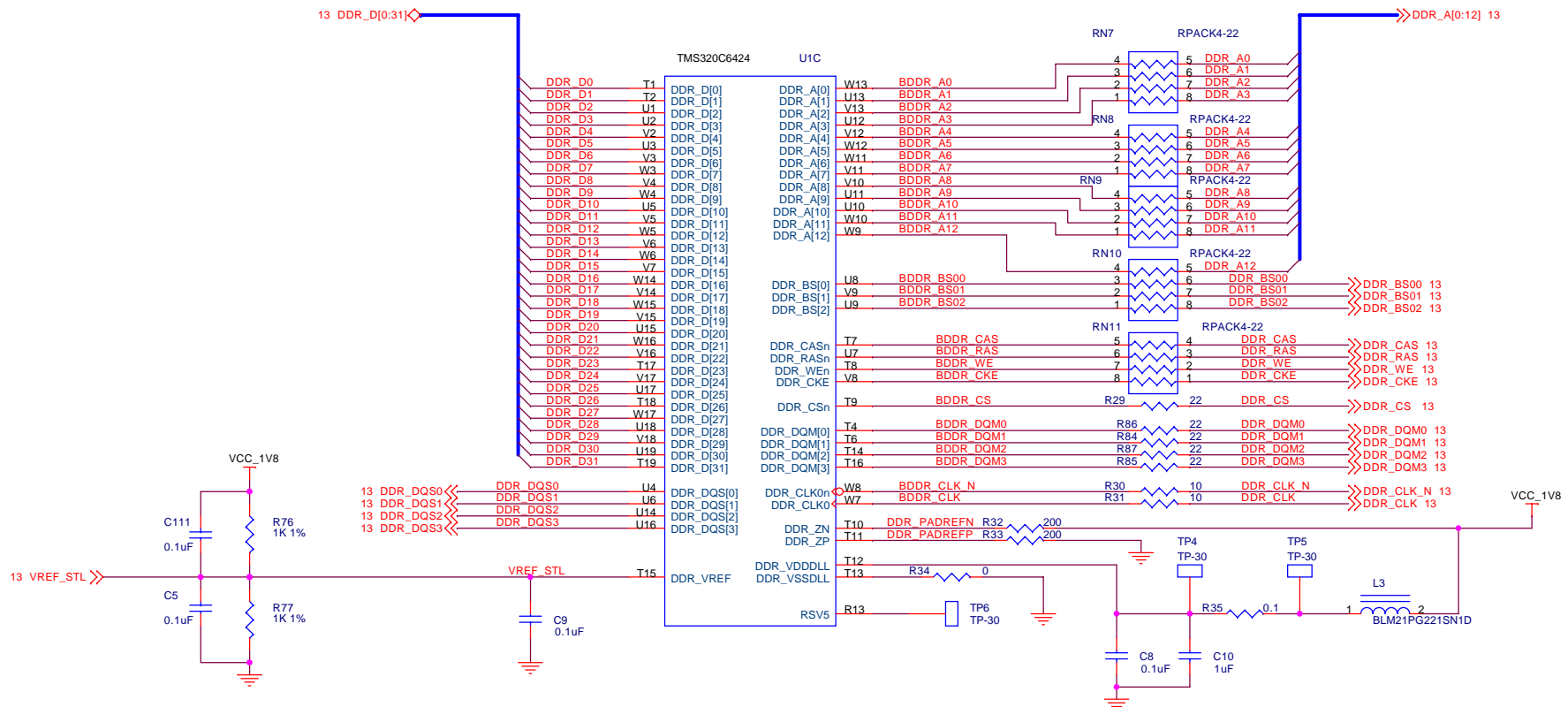
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Page Contents: DSP CLKS/RST/EMU			
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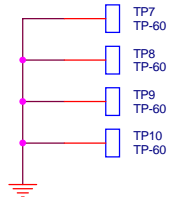
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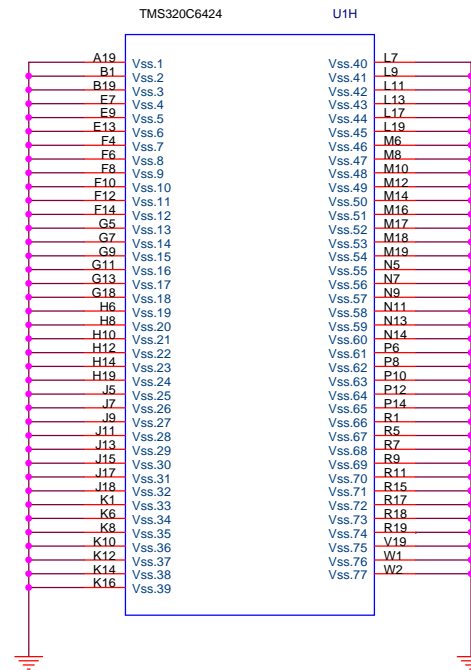
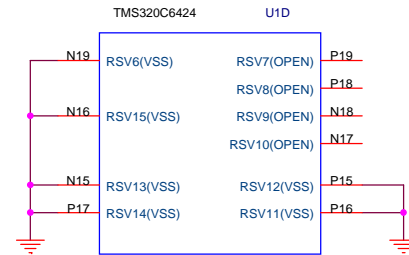


Follow the DDR PCB Layout App Note

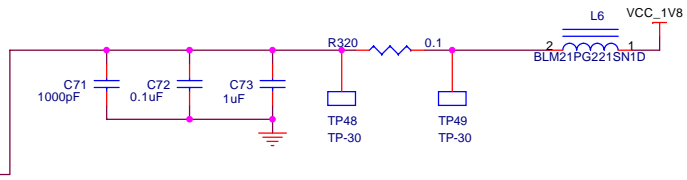
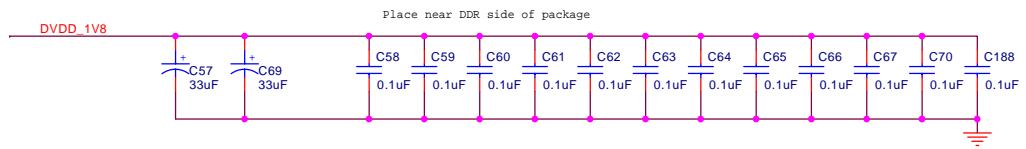
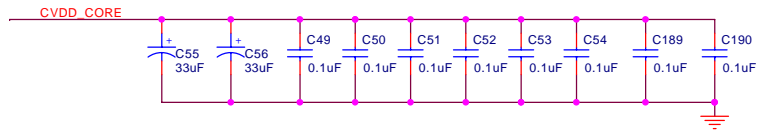
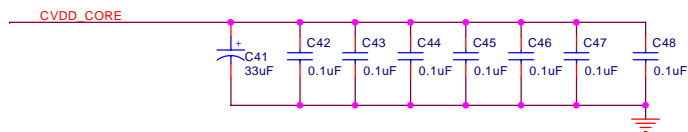
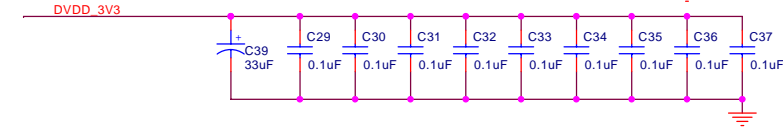
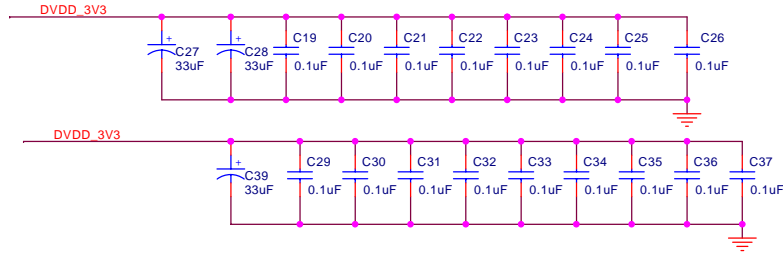
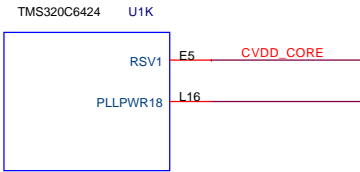
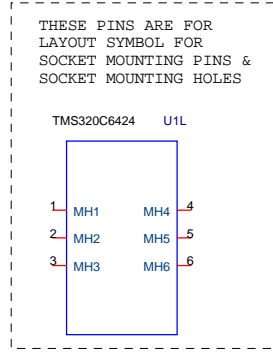
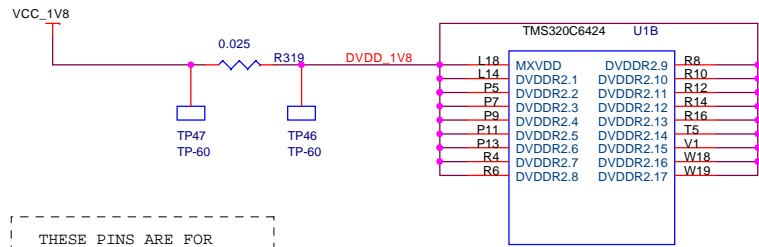
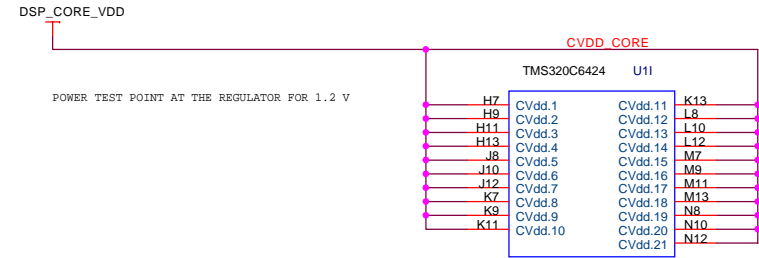
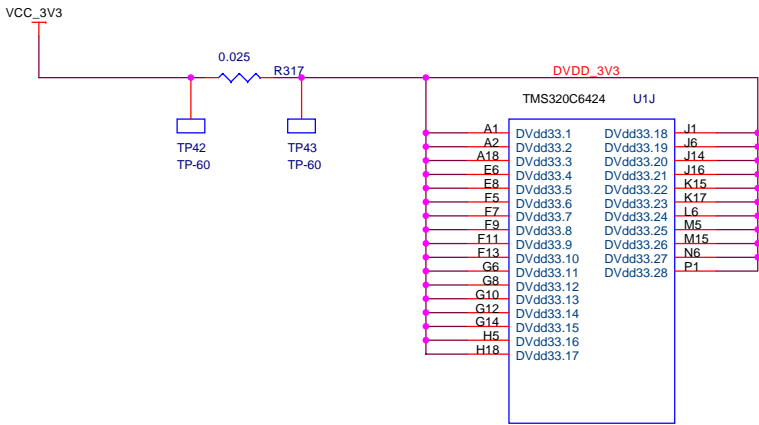


SURFACE MOUNT TEST POINT PADS
USED FOR VERIFYING DDR TIMINGS

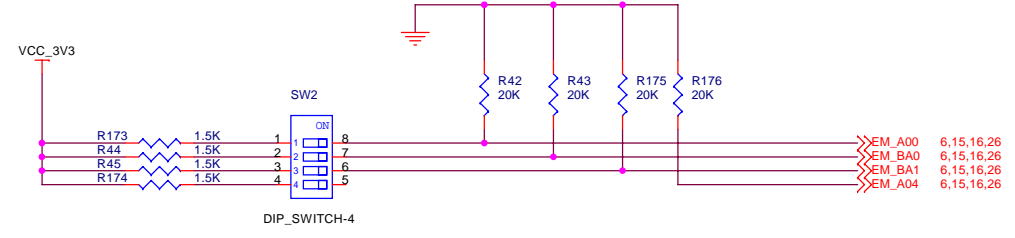
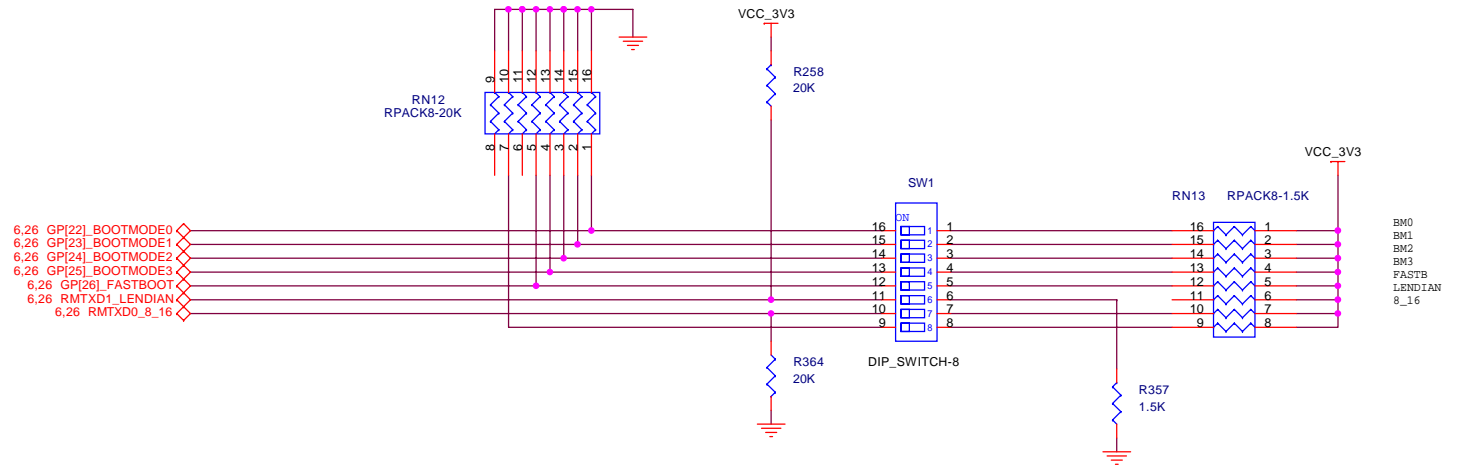
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Page Contents: DSP DDR Interface			
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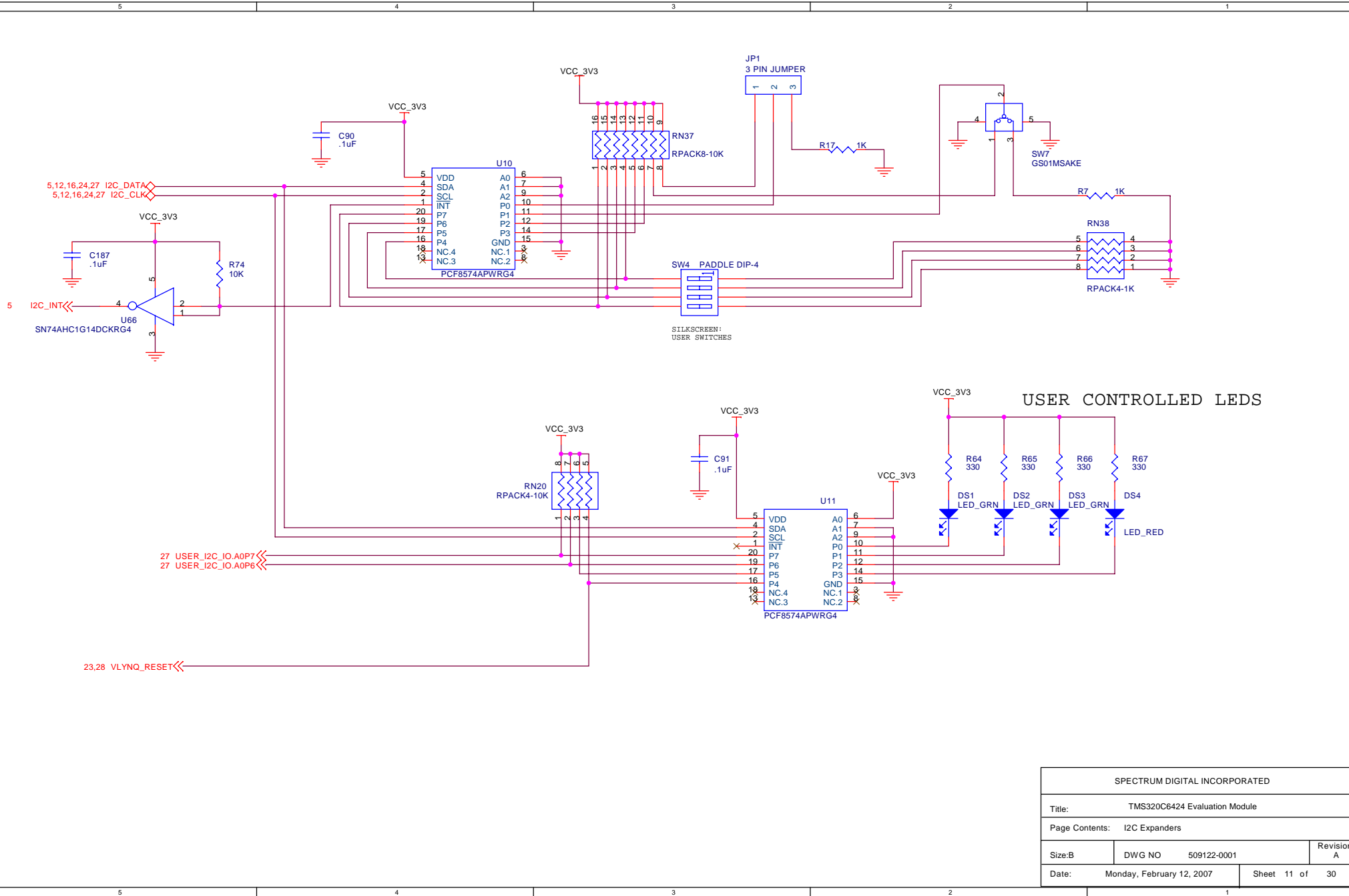
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Page Contents: DSP DACS/GND-pins			
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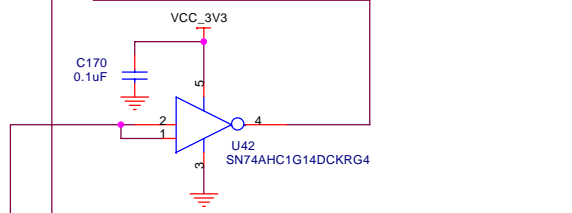
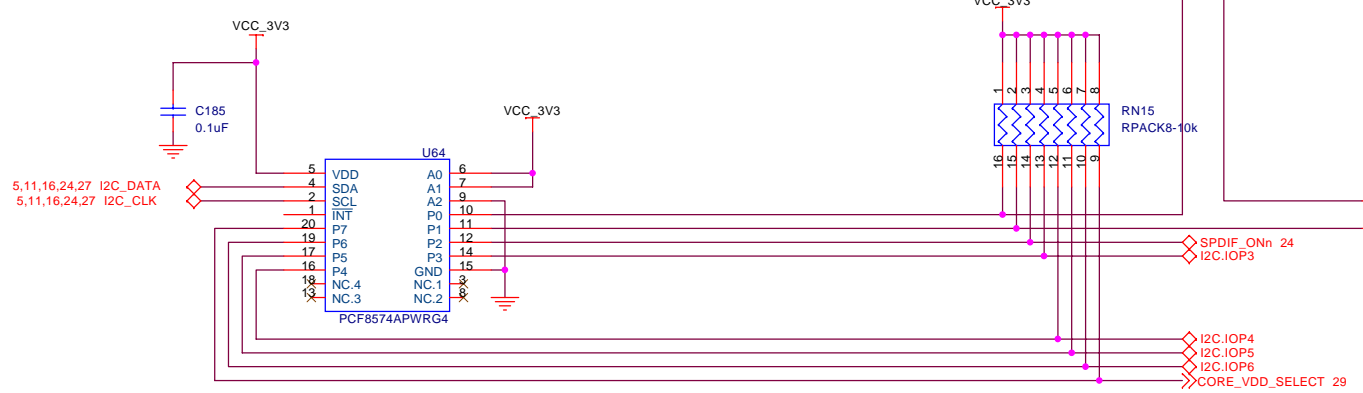
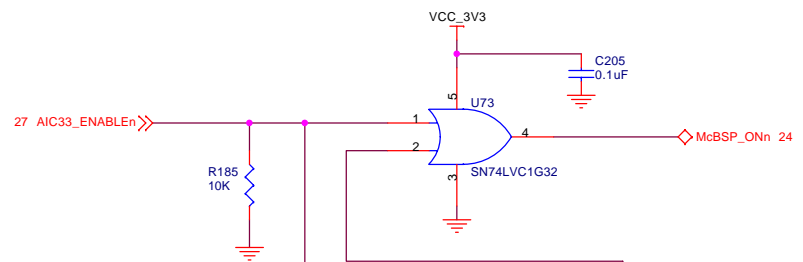
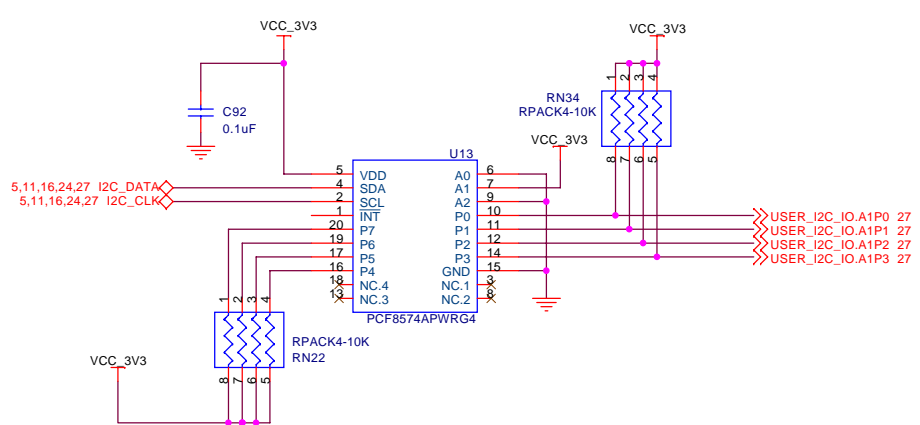
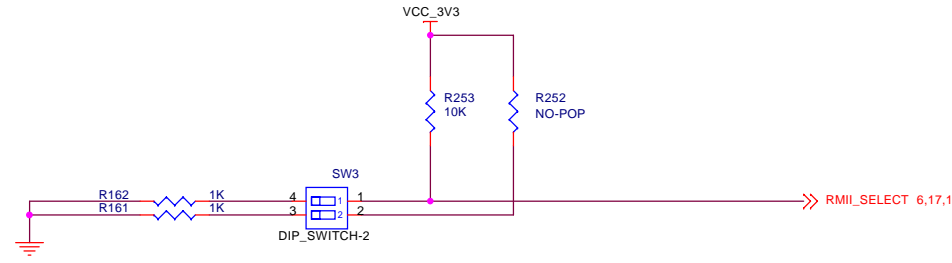
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Page Contents: DSP Power Pins			
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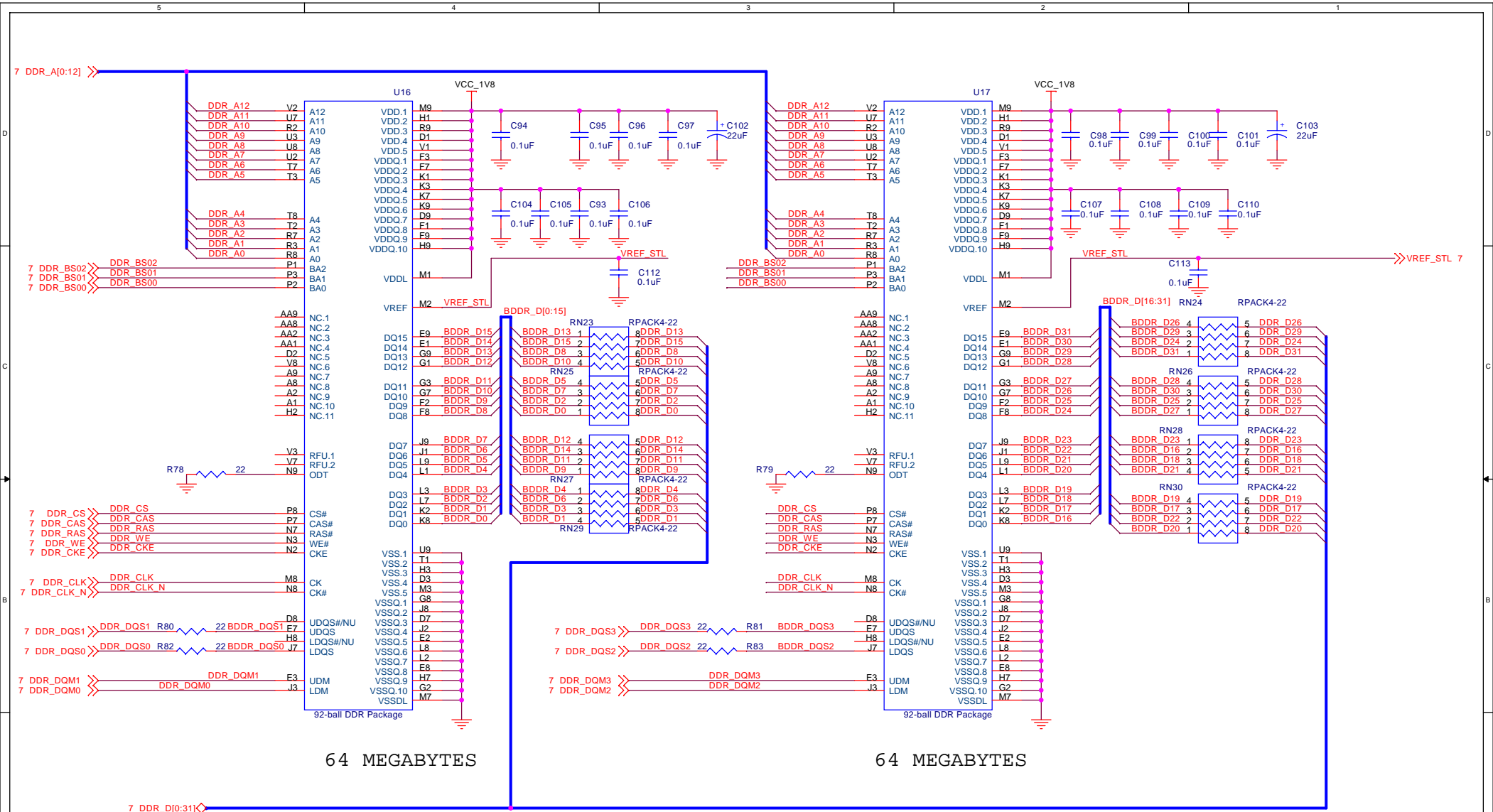
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Page Contents: Boot DIP Switches			
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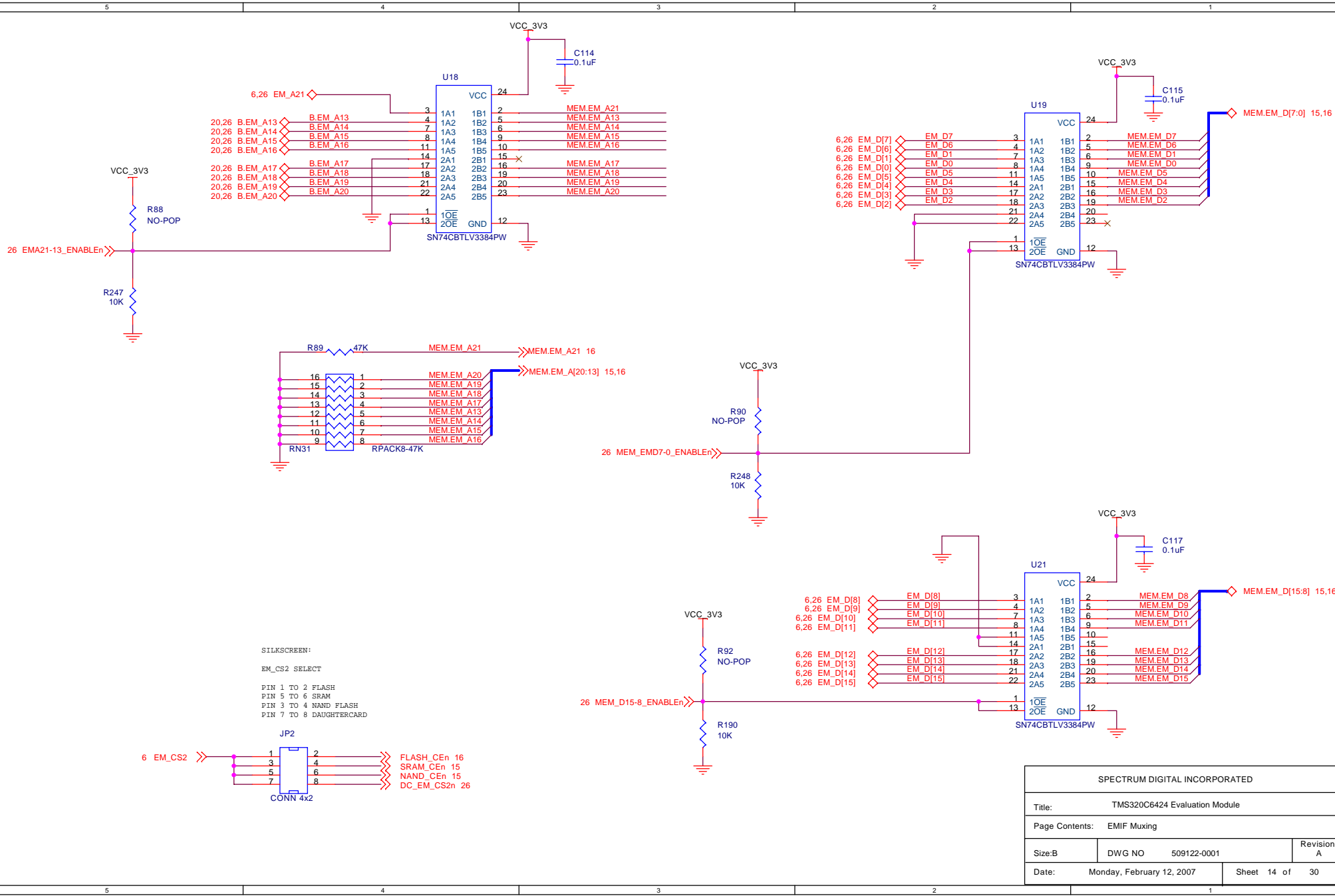


64 MEGABYTES

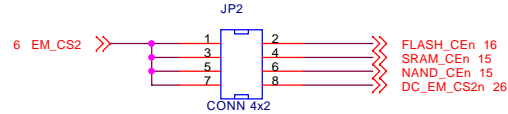
64 MEGABYTES

Layout for the 92-ball DDR Package but populate the 84-ball EDE5116AFSE.
 Ball assignments are incorrect for 84-ball package.
 Use -5C-E (533MHz) or -4A-E (400MHz) speed grade?

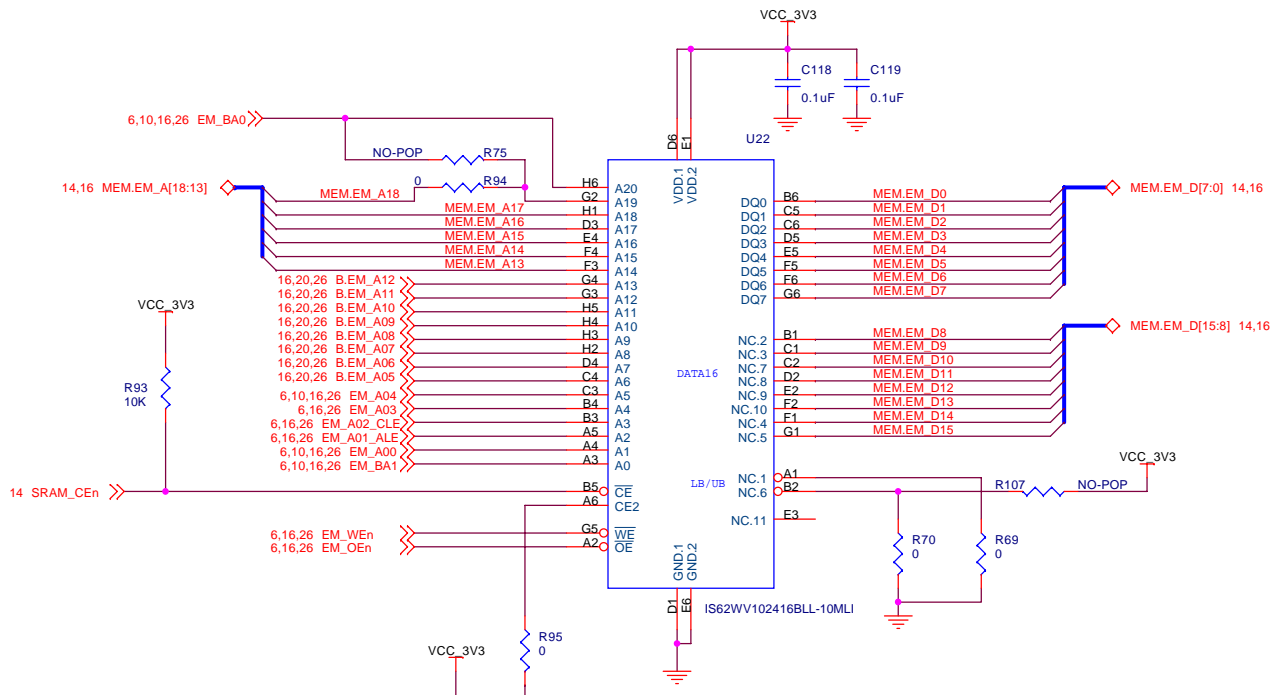
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SILKSCREEN:
 EM_CS2 SELECT
 PIN 1 TO 2 FLASH
 PIN 5 TO 6 SRAM
 PIN 3 TO 4 NAND FLASH
 PIN 7 TO 8 DAUGHTERCARD



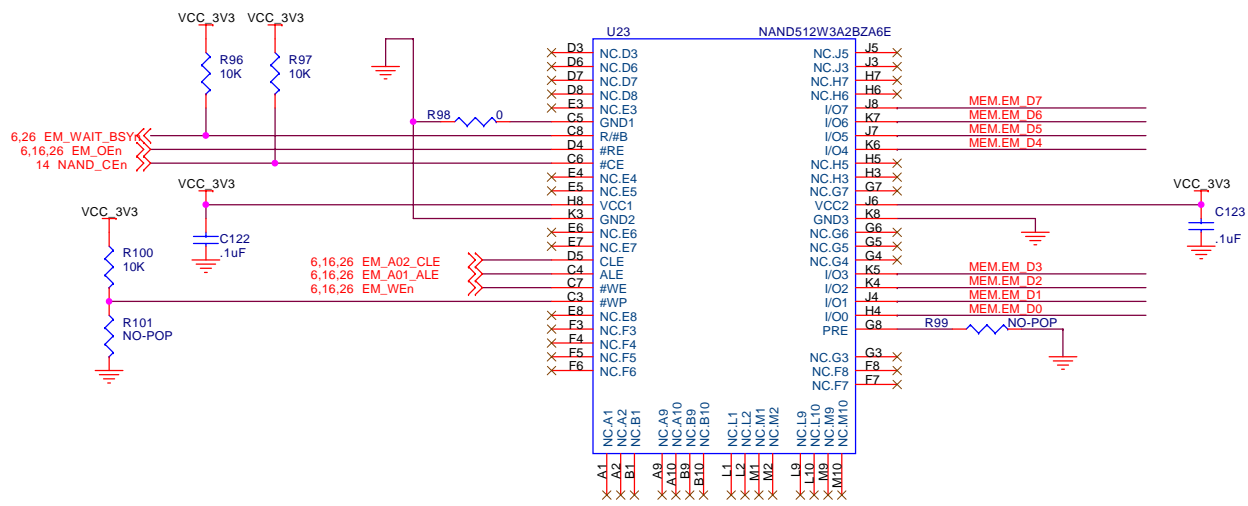
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Page Contents: EMIF Muxing			
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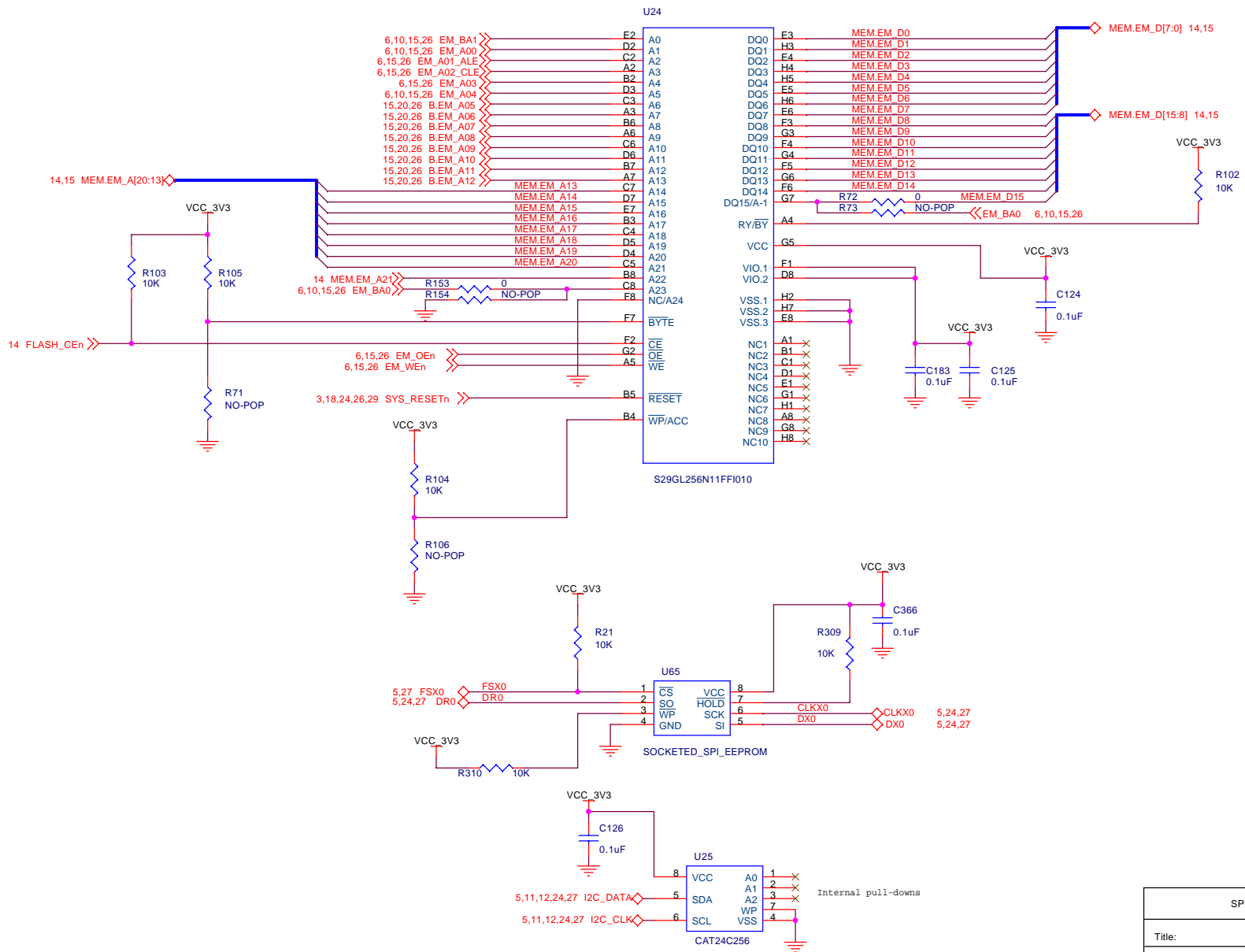
Set this up to run 8 or 16 bit

16 BIT INTERFACE	8 BIT INTERFACE
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IS61WV102416BLL-10MLI	IS61WV20488BLL-25MLI

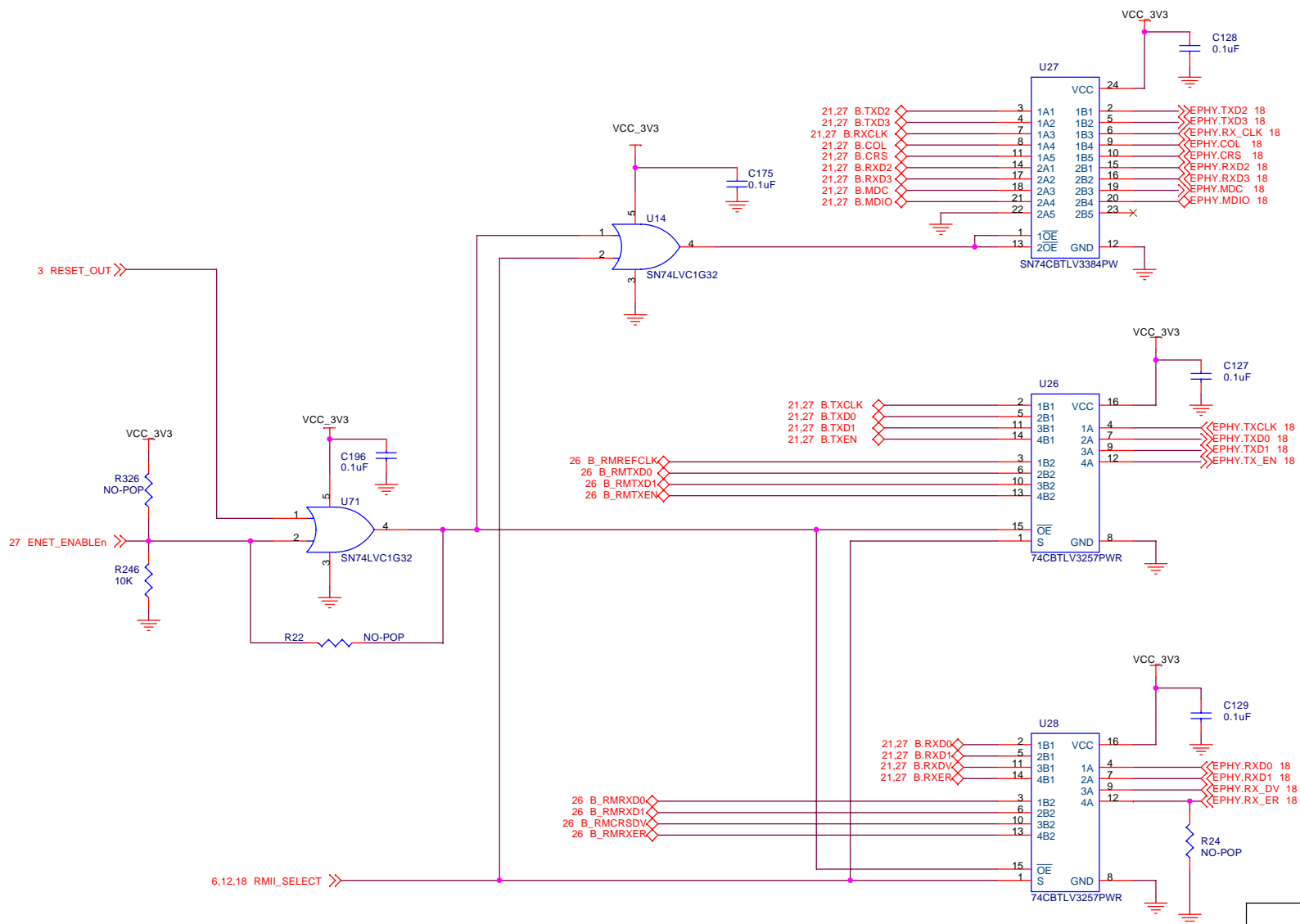
CE DON'T CARE DEVICE



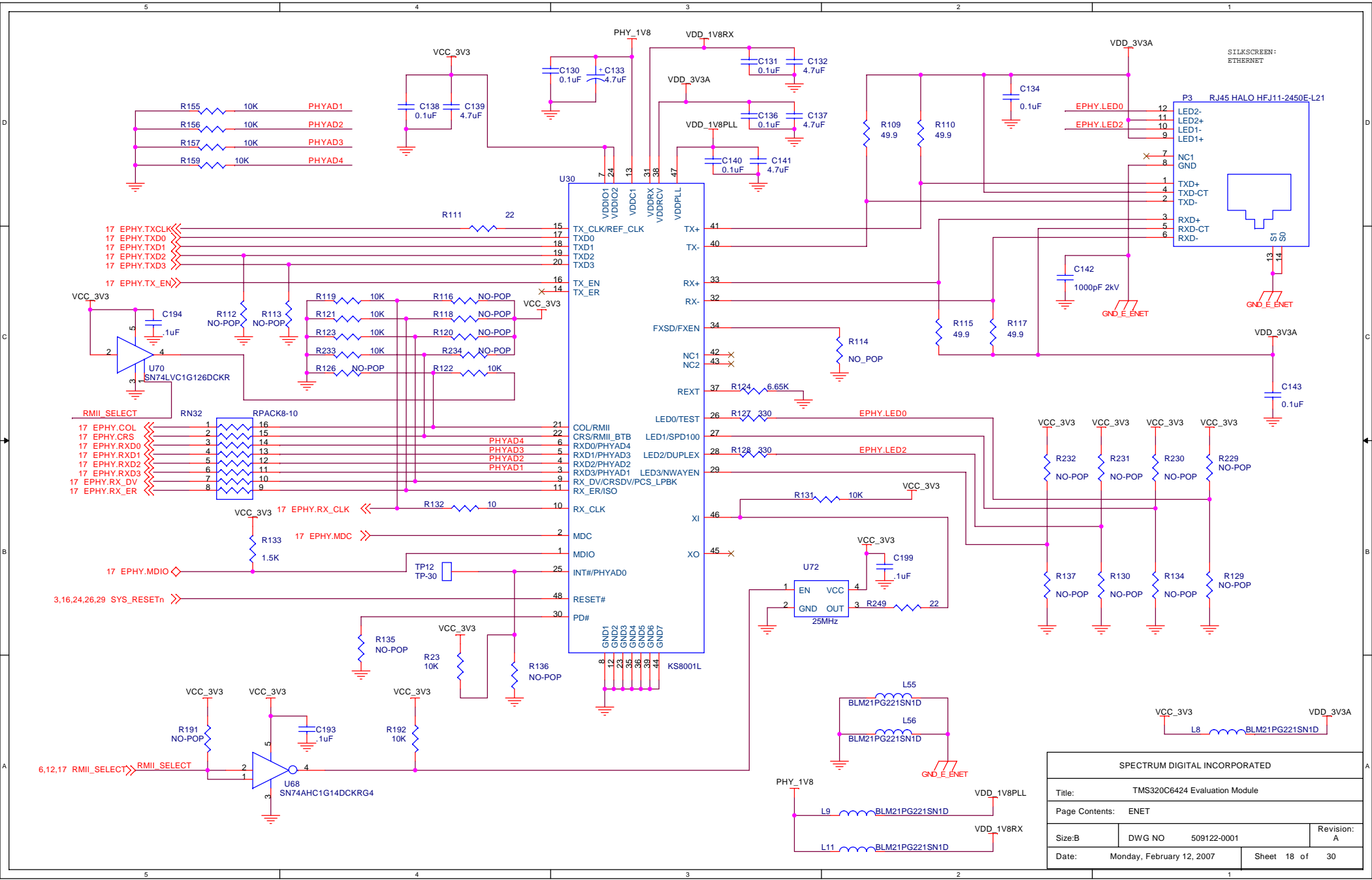
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Page Contents: NAND-Flash/SRAM			
Size: B	DWG NO: 509122-0001	Revision: B	
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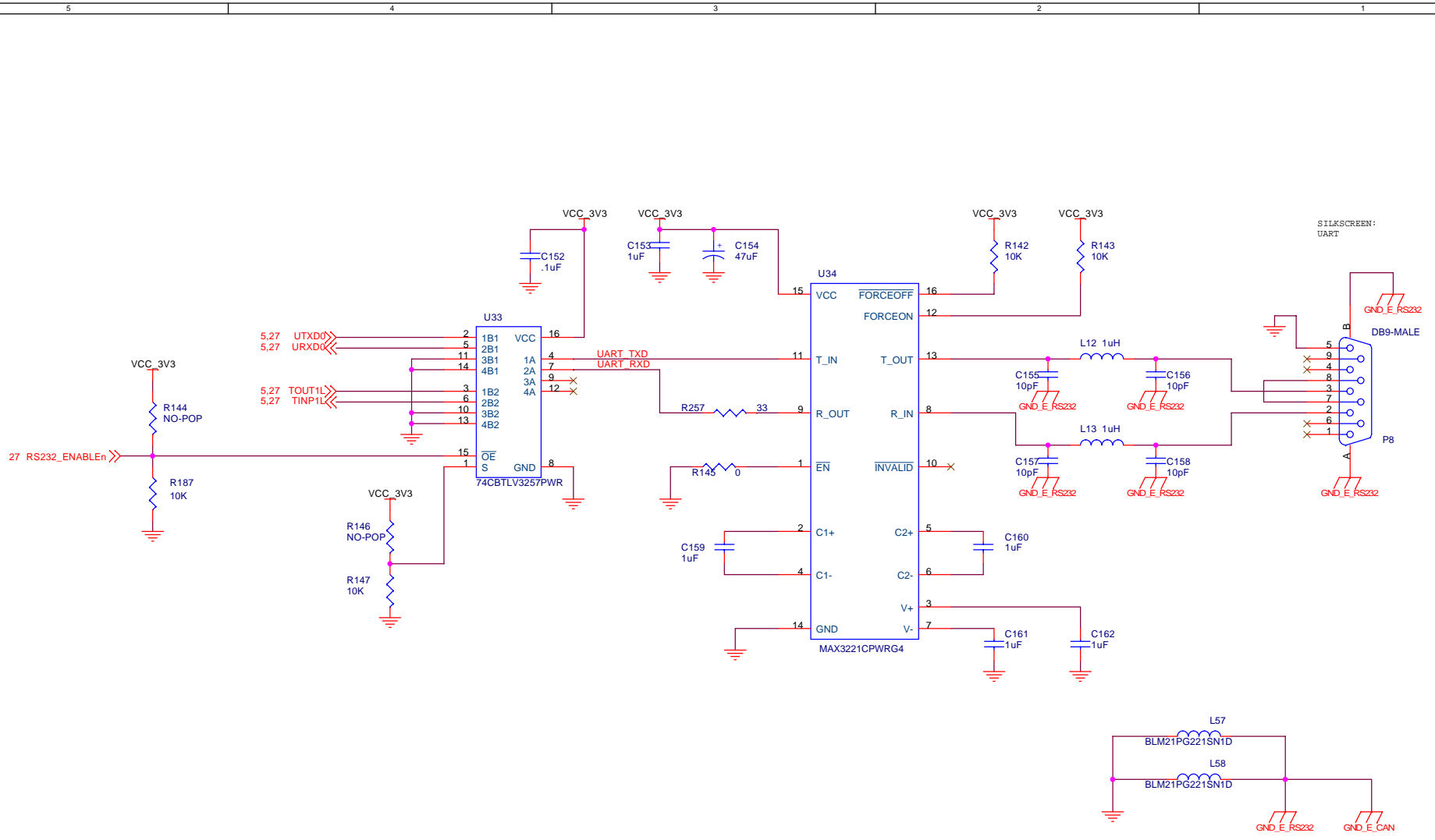
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Page Contents: NOR-Flash/EEPROM			
Size: B	DWG NO	509122-0001	Revision: A
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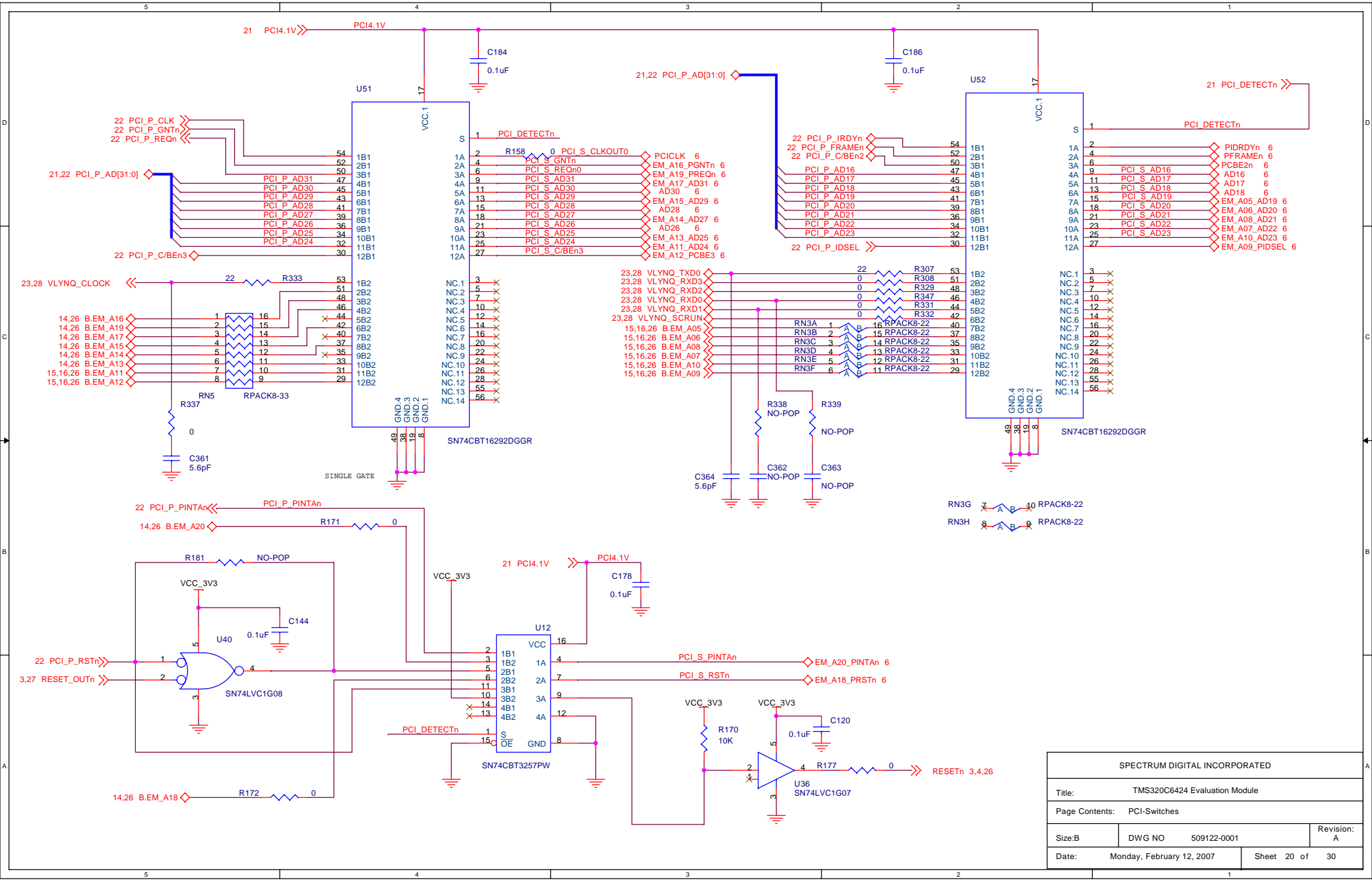
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Page Contents: ENET Muxing			
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Page Contents: ENET			
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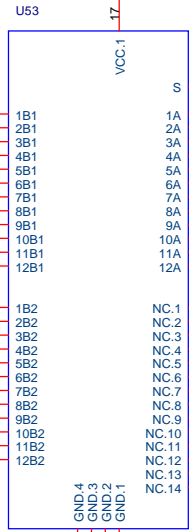
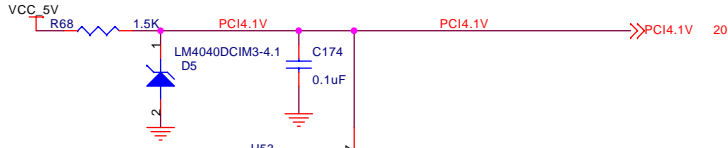


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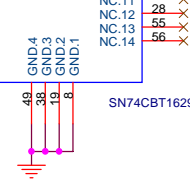
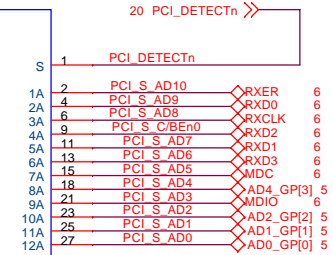
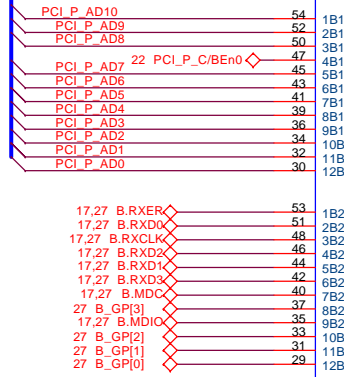
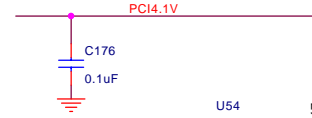
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Title: TMS320C6424 Evaluation Module			
Page Contents: PCI-Switches			
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20,22 PCI_P_AD[31:0]

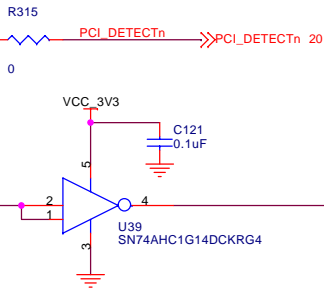


The PCI 33 Mhz Signals must be shorter than 1.5"

The CLK signal trace length must be 2.5" +/- 0.1".



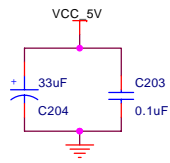
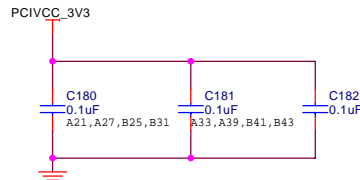
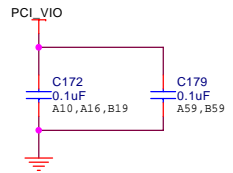
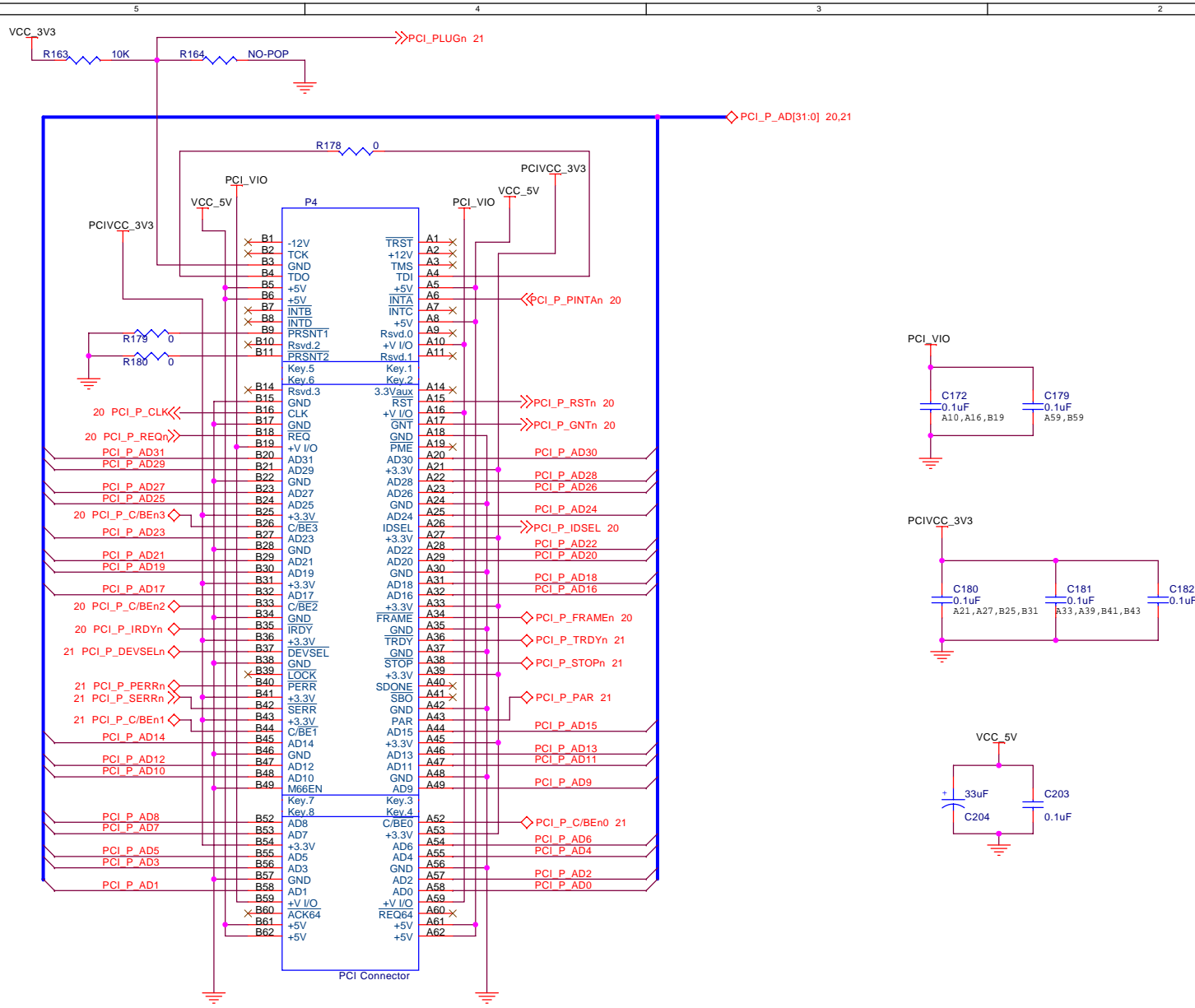
SN74CBT16292DGGR



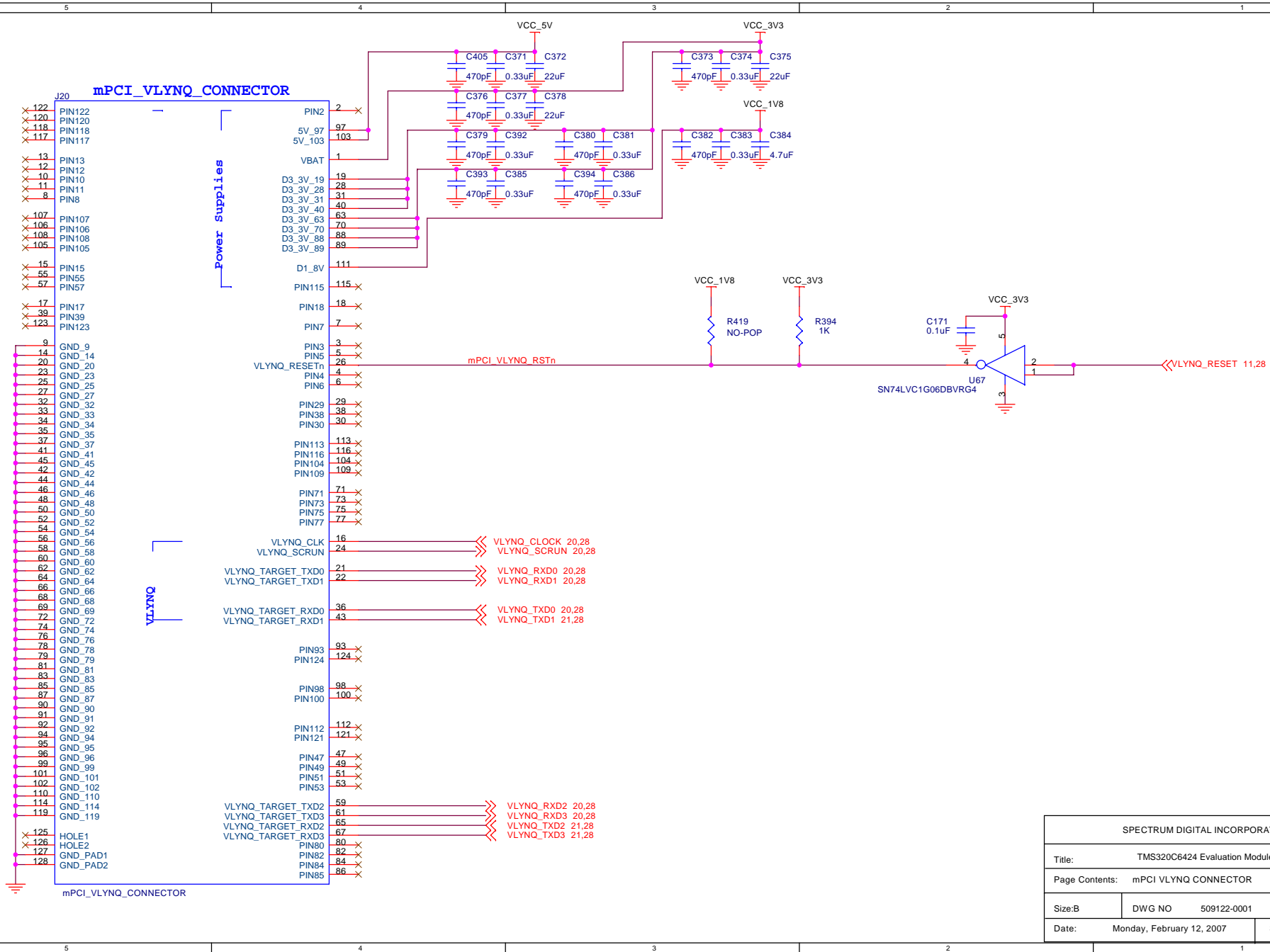
22 PCI_PLUGn

U39 SN74AHC1G14DCKRG4

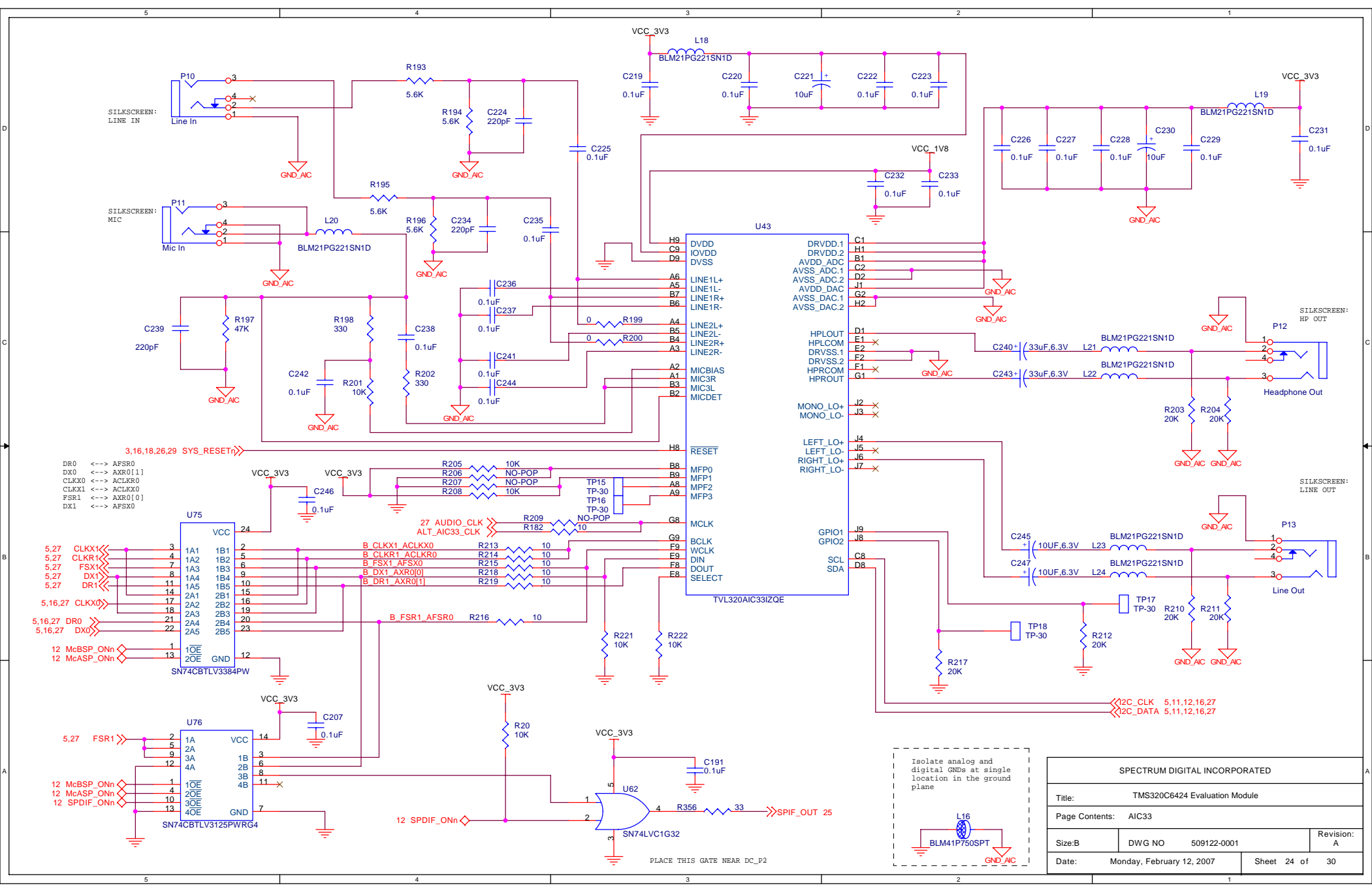
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Title: TMS320C6424 Evaluation Module			
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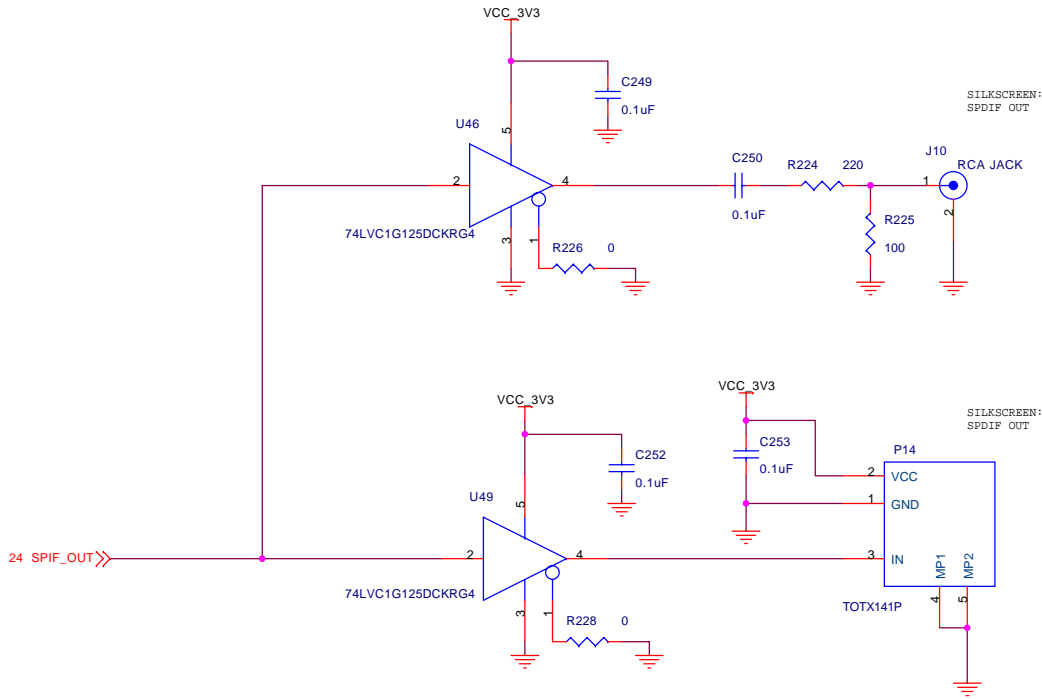


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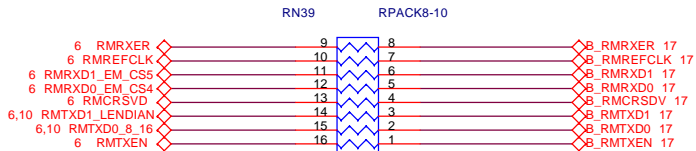
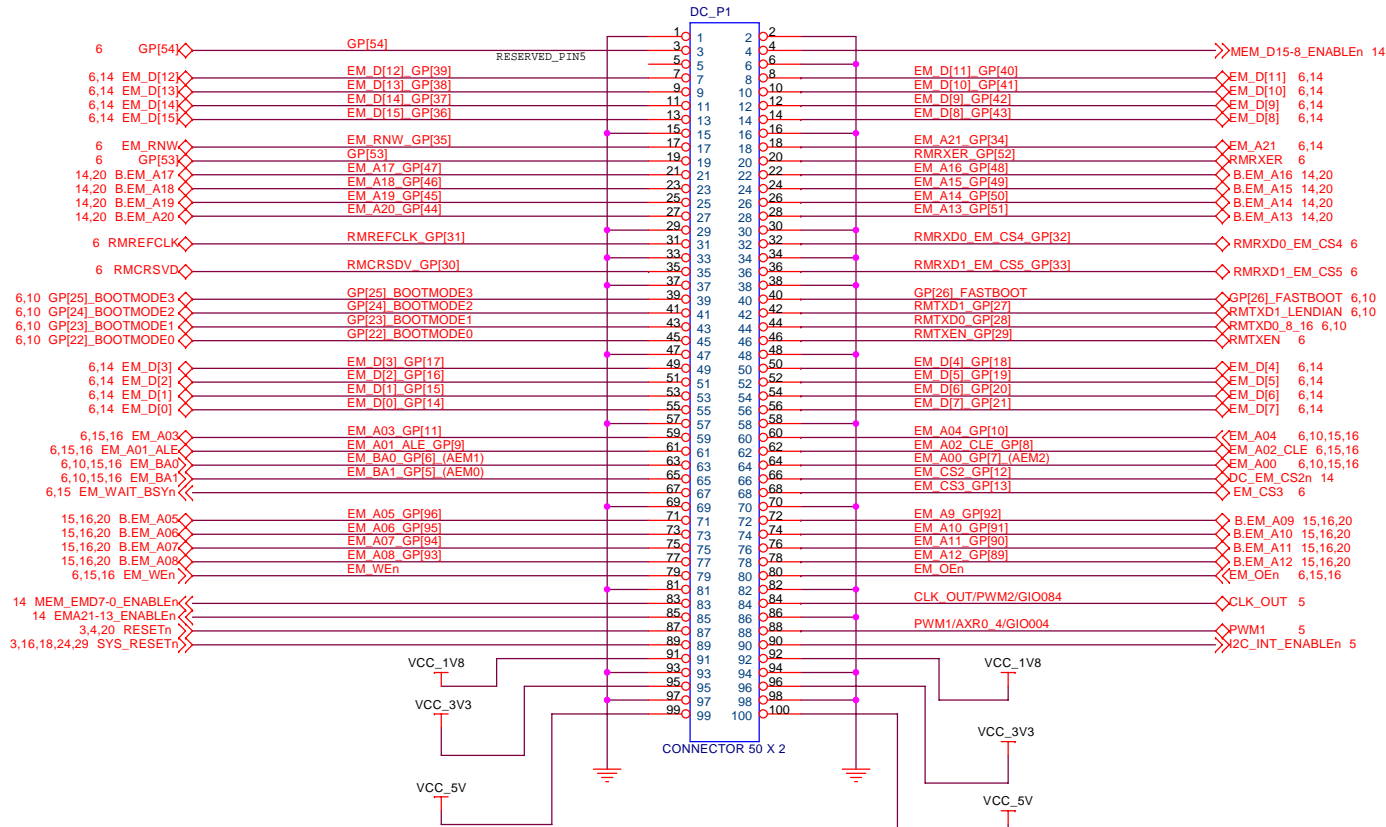
Isolate analog and digital GNDs at single location in the ground plane

SPECTRUM DIGITAL INCORPORATED			
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Page Contents: AIC33			
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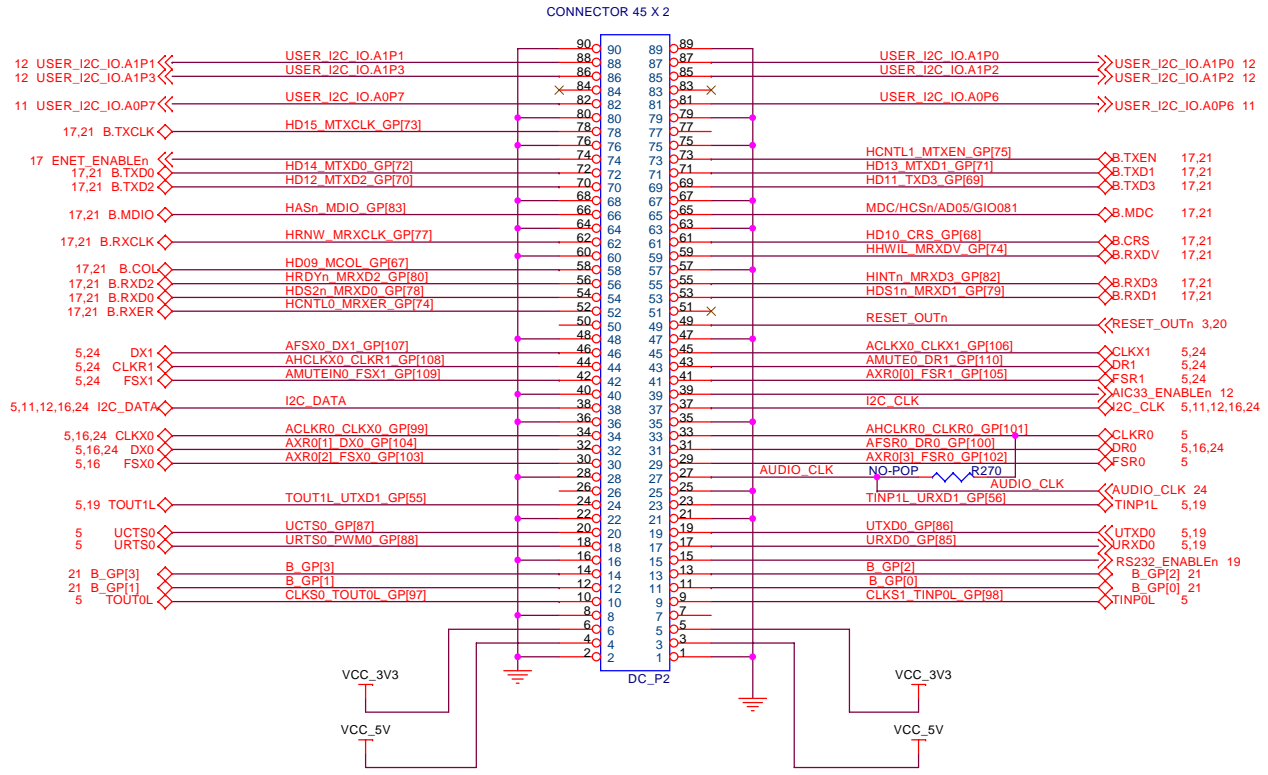


SPECTRUM DIGITAL INCORPORATED			
Title: TMS320C6424 Evaluation Module			
Page Contents: SPDIF/TVP5146-Switch			
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SILKSCREEN:
DC_P1

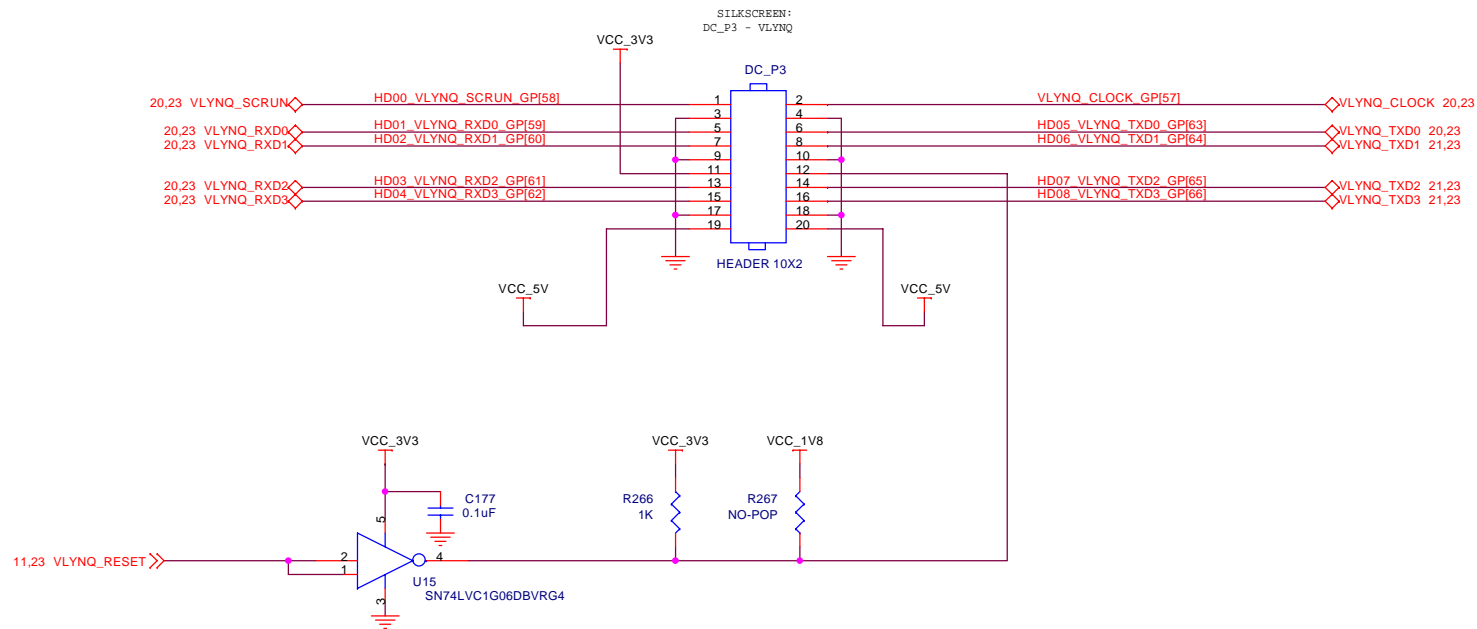


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Page Contents: VIDEO DC Conn.			
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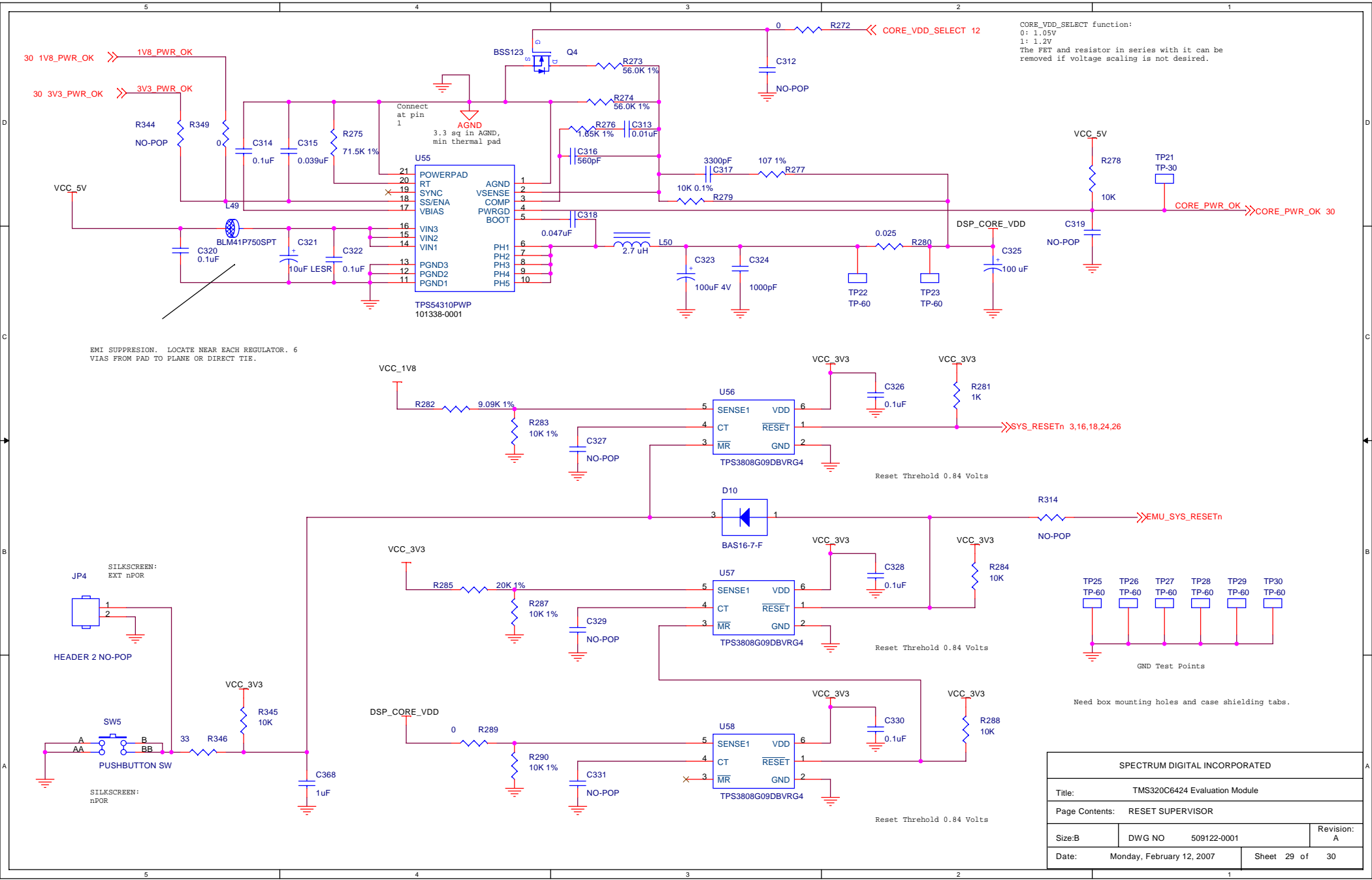


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Page Contents: EMAC/MCBSP DC Conn.			
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Note: Place ontop of traces going between the bus-exchange switches and the mPCI connector to improve signal integrity.



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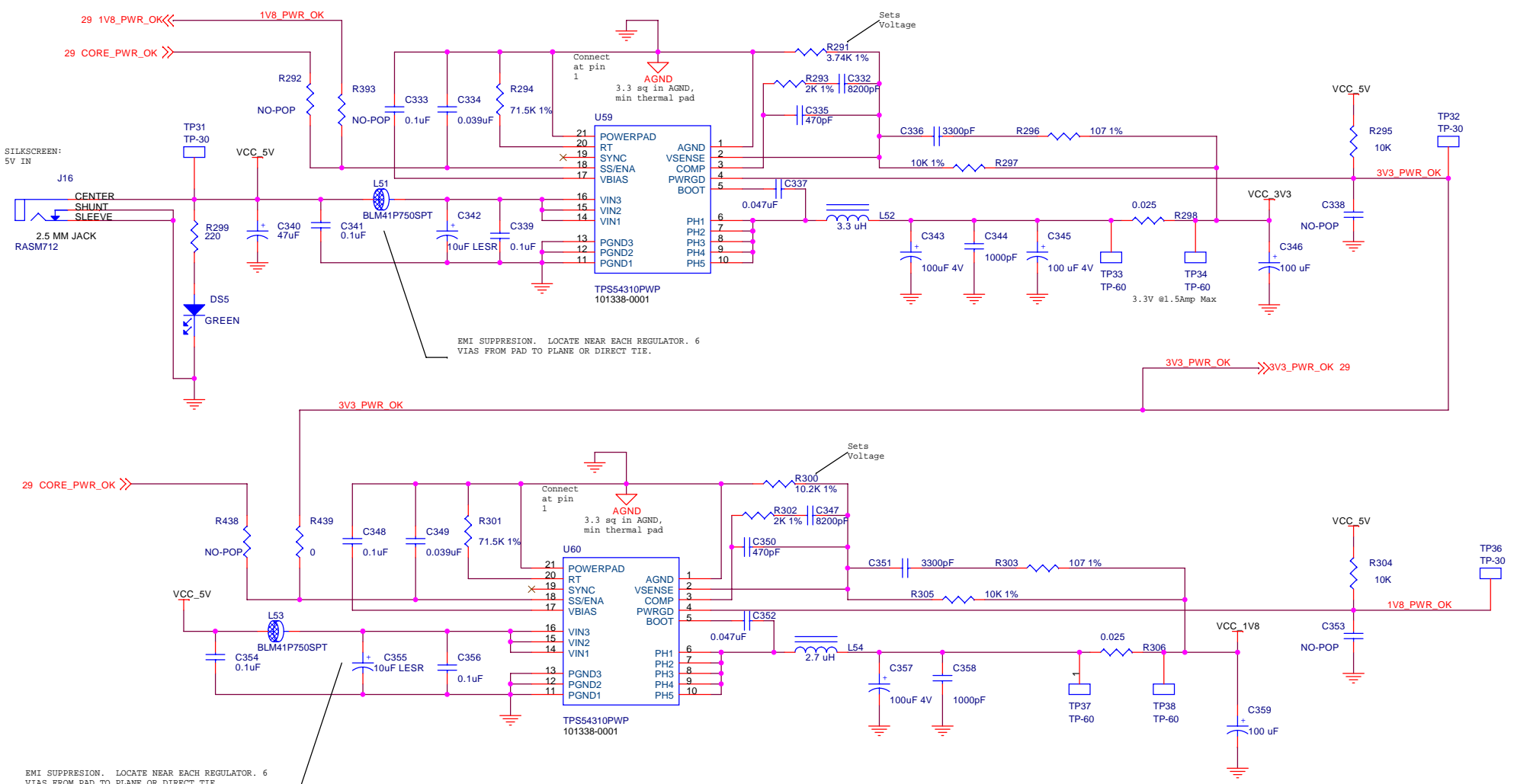


CORE_VDD_SELECT function:
 0: 1.05V
 1: 1.2V
 The FET and resistor in series with it can be removed if voltage scaling is not desired.

EMI SUPPRESSION. LOCATE NEAR EACH REGULATOR. 6 VIAS FROM PAD TO PLANE OR DIRECT TIE.

Need box mounting holes and case shielding tabs.

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SILKSCREEN:
5V IN

J16
CENTER
SHUNT
SLEEVE
2.5 MM JACK
RASM712

EMI SUPPRESSION. LOCATE NEAR EACH REGULATOR. 6 VIAS FROM PAD TO PLANE OR DIRECT TIE.

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