

What is new going from A2 to A3:

- 1) IR Remote Support Added, see ECP offsets 0x16, 0x17, and 0x18
- 2) User Input Button Support, see ECP offsets 0x16, 0x17, and 0x18
- 3) Corrected some I2C typos.

User input buttons are supported as special remote codes. Also user buttons are debounced and available raw to the DM355 if desired.

## ECP I2C Access:

The ECP is mapped to I2C address 0x25. The ECP uses 7 bit addressing. The ECP also utilizes the built-in not ready mechanism of the I2C bus – holding the clock low to extend access times. It is crucial that the I2C master access the ECP properly.

An ECP write cycle consists of writing the ECP I2C address (0x25), the desired ECP offset, and the data to be written to that offset. Auto-increment/bursting is not supported.

The ECP I2C WRITE cycle is as follows:

S	0	1	0	0	1	0	1	0	A	y	y	y	y	y	y	y	A
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

w	w	w	w	w	w	w	w	A	P
---	---	---	---	---	---	---	---	---	---

Where yyyyyyyy is the desired offset, and wwwwwwww is the write data.

The ECP READ cycle is similar. It consists of writing the ECP I2C address (0x25), the desired ECP offset, and then issuing a read via a repeated start sequence:

S	0	1	0	0	1	0	1	0	A	y	y	y	y	y	y	y	A
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

R	0	1	0	0	1	0	1	1	A	r	r	r	r	r	r	r	N	P
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Where yyyyyyyy is the desired offset, and rrrrrrrr is the read data.

(S = start condition, R = repeated start condition, A = acknowledge, N = nack, P = stop condition. Acknowledge comes from destination.)

Each ECP read and write is a single I2C transaction. It is very important that the I2C master honor the I2C ready mechanism. When the ECP is not-ready it will hold the clock line low. At the end of the not-ready condition, the ECP will let the clock line go, allowing the master to continue clocking.

To test that the ECP has completed a WRITE, one could issue the WRITE followed by a READ of any ECP offset. When the READ completes, the user is guaranteed the ECP operation caused by the WRITE has completed.

Alternatively, if two sequential WRITES occur, the user is guaranteed the ECP operation caused by the first WRITE is complete when the second WRITE occurs.

Note: The ECP uses the built-in ready mechanism of I2C. The I2C HW on the ECP is also buffered. The I2C HW on the ECP will accept one ECP write transaction with no intervention by the MSP430. This write transaction will not be acted upon until the MSP430 responds to the interrupt from the I2C hardware. Thus, if it is necessary for the ECP to finish a write operation (i.e. setting up a mux), then the DM648 code should follow the write by another write or read to ensure the previous operation has completed.

*It is very important that the DM355 I2C driver honor the I2C ready mechanism which consists of the ECP slave holding down the SCL line when not ready.*

ECP Register Definitions:

**ECP Command Register (Offset 0x00)**

7

0

COMMAND CODE	
R/W-0	

Bit	Field	Value	Description
7-0	COMMAND CODE	0xnn	Command code for MSP430 internal function

Valid COMMAND CODEs are:

0x00	Null command
0x01	Cold Reset The EVM is powered off, back on, and reset. ECP registers are reinitialized.
0x02	Warm Reset – The DSP is reset. ECP registers are not reinitialized.
0x03	Warm Reset With Init – The DSP is reset and ECP registers are reinitialized.
0x04	Power Off – The EVM is powered off and will not turn back on until SW5 is pressed or the 5V power is removed and reapplied.
0x05	Reinitialize IR Remote
0x06	
0x07	
0x08	

**ECP Status Register (Offset 0x01)**

7

0

STATUS CODE
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R/W

Bit	Field	Value	Description
7-0	STATUS CODE	0xnn	Status code for MSP430 internal function

0x01	I2C Bad Offset
0x02	I2C Bad Command
0x04	DM355 EVM Power Supply Error
0x08	DM355 EVM IR Receive Buffer Overrun
0x10	
0x20	
0x40	
0x80	

**Reset Output Register (Offset 0x02)**

7

6

5

4

3

2

1

0

AIC33	CPLD	SYS	ETHERNET	IMAGER	TVP5154	NORFLASH	DC5
R/W-0	R/W-P0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-P0	R/W-0

Bit	Field	Value	Description
7	AIC33	0	AIC33 in reset
		1	AIC33 not in reset
6	CPLD	0	CPLD in reset
		1	CPLD not in reset
5	SYS	0	SYS reset low
		1	SSY reset high
4	ETHERNET	0	Ethernet controller in reset
		1	Ethernet controller out of reset
3	IMAGER	0	Imager in reset
		1	Imager out of reset
2	TVP5154	0	TVP5154 in reset
		1	TVP5154 out of reset
1	NORFLASH	0	NORFLASH in reset
		1	NORFLASH out of reset
0	DC5	0	DC5 reset low
		1	DC5 reset high

### LED Register (Offset 0x03)

7	6	5	4	3	2	1	0
LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit	Field	Value	Description
7	LED7	0	LED7 is lit
		1	LED7 is extinguished
6	LED6	0	LED6 is lit
		1	LED6 is extinguished
5	LED5	0	LED5 is lit
		1	LED5 is extinguished
4	LED4	0	LED4 is lit
		1	LED4 is extinguished
3	LED3	0	LED3 is lit
		1	LED3 is extinguished
2	LED2	0	LED2 is lit
		1	LED2 is extinguished
1	LED1	0	LED1 is lit
		1	LED1 is extinguished
0	LED0	0	LED0 is lit
		1	LED0 is extinguished

### Input Switch Register #1 (Offset 0x04)

7	6	5	4	3	2	1	0
USER0	CPLDO	430INT	NTSC/PAL	SW6.4	SW6.3	SW6.2	SW6.1
R	R/W	R	R	R	R	R	R

Bit	Field	Value	Description
7	USER0	0	J7 is pulled down (2-3)
		1	J7 is pulled up (1-2)
6	CPLDO	0	CPLD_USER_OPT is low
		1	CPLD_USER_OPT is high
5	430INT	0	MSP430INT is low events in cue.
		1	MSP430INT is high no events in cue.
4	NTSC/PAL	0	J1 is pulled down (2-3)
		1	J1 is pulled up (1-2)
3	SW6.4	0	SW6.4 is off
		1	SW6.4 is on
2	SW6.3	0	SW6.3 is off
		1	SW6.3 is on
1	SW6.2	0	SW6.2 is off
		1	SW6.2 is on
0	SW6.1	0	SW6.1 is off
		1	SW6.1 is on

### Input Switch Register #2 (Offset 0x05)

7	6	5	4	3	2	0
SW14	SW13	SW12	SW11	SW10	RESERVED	
R	R	R	R	R	R	

Bit	Field	Value	Description
7	SW14 (Debounced)	0	SW14 is pushed
		1	SW14 is released
6	SW13 (Debounced)	0	SW13 is pushed
		1	SW13 is released
5	SW12 (Debounced)	0	SW12 is pushed
		1	SW12 is released
4	SW11 (Debounced)	0	SW11 is pushed
		1	SW11 is released
3	SW10 (Debounced)	0	SW10 is pushed
		1	SW10 is released
2-0	Reserved	X	Reserved

### SD/MMC Status Register (Offset 0x06)

7	5	4	3	2	1	0
RSVD	SDMMC1INST	SDMMC1WP	SCMMC0INST	SDMMC0WP	RSVD	
R	R	R	R	R	R	

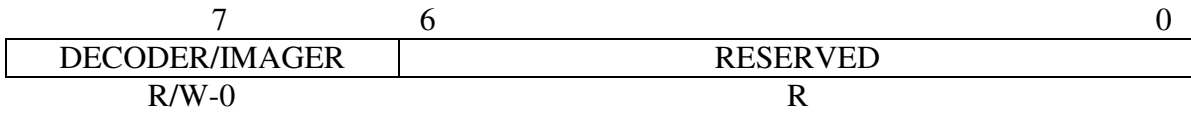
Bit	Field	Value	Description
7-5	RSVD	X	Reserved
4	SDMMC1INST	0	SDMMC1 Card Installed
		1	SDMMC1 Card Not Installed
3	SDMMC1WP	0	SDMMC1 Card Not Write Protected
		1	SDMMC1 Card Write Protected
2	SDMMC0INST	0	SDMMC0 Card Installed
		1	SDMMC0 Card Not Installed
1	SDMMC0WP	0	SDMMC0 Card Not Write Protected
		1	SDMMC0 Card Write Protected
0	Reserved	X	Reserved

**Firmware Revision Register (Offset 0x07)**



Bit	Field	Value	Description
7-0	FIRMREV		PCB Firmware Revision Number

**Video Input Mux Control (Offset 0x08)**



Bit	Field	Value	Description
7	DECODER/IMAGER	0	DM355 Input Video Port Connected to TVP5146
		1	DM355 Input Video Port Connected to Imager Daughter Card
6-0	RESERVED	X	Reserved

**Power Supply Control/Status (Offset 0x09)\***

7	6	5	4	3	2	1	0
1V8EN	1V3EN	1V8ST	1V3ST	3V3ST	ECPVST	RSVD	3V3EN
R	R	R	R	R	R	R	R

Bit	Field	Value	Description
7	1V8EN	0	1.8V Power Supply Off
		1	1.8V Power Supply On
6	1V3EN	0	1.3V Power Supply Off
		1	1.3V Power Supply On
5	1V8ST	0	1.8V Power Out Of Spec
		1	1.8V Power Good
4	1V3ST	0	1.3V Power Out Of Spec
		1	1.3V Power Good
3	3V3ST	0	3.3V Power Out of Spec
		1	3.3V Power Good
2	ECPVST	0	3.3V ECP Power Out Of Spec
		1	3.3V ECP Power Good
1	RSVD	X	Reserved
0	3V3EN	0	3.3V Power Supply Off
		1	3.3V Power Supply On

\*Reading from this register will initiate a voltage reading on all the power supplies. Power good status as well as the supply voltage readings available from offset 0x1A through 0x21 will be updated. Reading from the voltage readings only will give the values at the time of the last voltage reading taken by the last read from offset 0x09

**ECP Voltage Low and High (Offsets 0x0A and 0x0B)**

7	0
ECP Voltage Low	
R	

Bit	Field	Value	Description
7-0	ECP Voltage Low		Lower 8 bits of measured ECP voltage

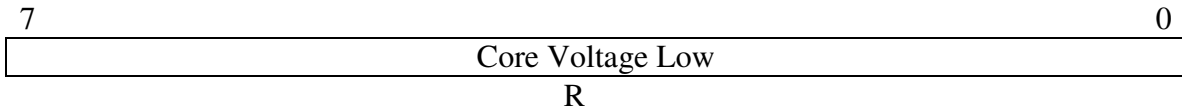
7	4	3	0
Reserved		ECP Voltage High	
R-0		R	

Bit	Field	Value	Description
7-0	Reserved		Reserved
3-0	ECP Voltage High		Upper 4 bits of measured ECP voltage

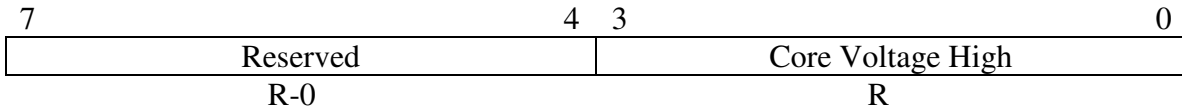
ECP voltage (v) = ECP Voltage Count/819



### VCC 1V3 Voltage Low and High (Offsets 0x0C and 0x0D)



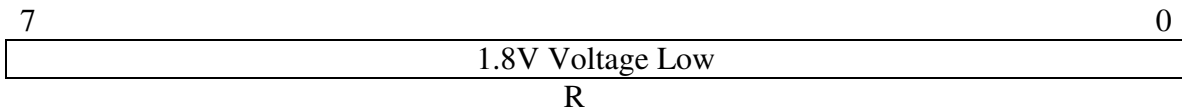
Bit	Field	Value	Description
7-0	Core Voltage Low		Lower 8 bits of measured core voltage



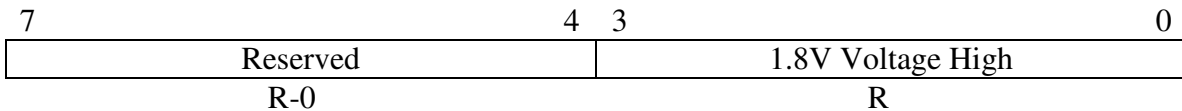
Bit	Field	Value	Description
7-0	Reserved		Reserved
3-0	Core Voltage High		Upper 4 bits of measured core voltage

Core voltage (v) = Core Voltage Count/1638

### 1.8V Voltage Low and High (Offsets 0x0E and 0x0F)



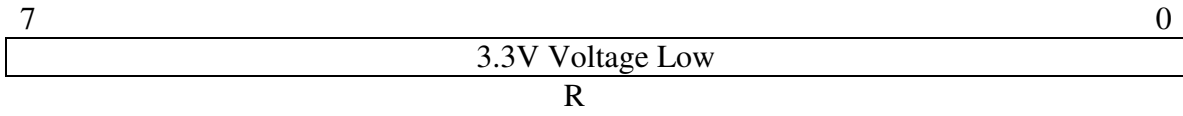
Bit	Field	Value	Description
7-0	1.8V Voltage Low		Lower 8 bits of measured 1.8V voltage



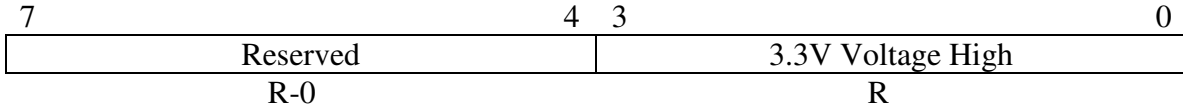
Bit	Field	Value	Description
7-0	Reserved		Reserved
3-0	1.8V Voltage High		Upper 4 bits of measured 1.8V voltage

1.8V voltage (v) = 1.8V Voltage Count/1638

### 3.3V Voltage Low and High (Offsets 0x10 and 0x11)



Bit	Field	Value	Description
7-0	3.3V Voltage Low		Lower 8 bits of measured 3.3V voltage



Bit	Field	Value	Description
7-0	Reserved		Reserved
3-0	3.3V Voltage High		Upper 4 bits of measured 3.3V voltage

3.3V voltage (v) = 3.3V Voltage Count/972.872

### Real Time Clock Registers (Offsets 0x12, 0x13, 0x14, and 0x15)

7	0
RTC Count Byte 0	
R/W	

Bit	Field	Value	Description
7-0	RTC Count Byte 0		Lower 8 bits of the real time count (LSB)

7	0
RTC Count Byte 1	
R/W	

Bit	Field	Value	Description
7-0	RTC Count Byte 1		Next 8 bits of the real time count

7	0
RTC Count Byte 2	
R/W	

Bit	Field	Value	Description
7-0	RTC Count Byte 2		Next 8 bits of the real time count

7	0
RTC Count Byte 3	
R/W	

Bit	Field	Value	Description
7-0	RTC Count Byte 4		Upper 8 bits of the real time count (MSB)

### IR Remote Data Count (Offset 0x16)

7	0
User Input Data Count	
R	

Bit	Field	Value	Description
7-0	User Input Data Count		Number of 16 bit IR/Pushbutton events in cue. Decrementd when low byte of user input word is read from offset 0x18. User is advised to read the high byte at offset 0x17 first, then read 0x18 to get the low byte. When IR Data Count is zero there are no user events in cue.

**IR Data High Byte (Offset 0x17)**

7

0

User Data High Byte
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R

Bit	Field	Value	Description
7-0	User Data High Byte		High byte of User Data. Reading this register will not decrement offset 0x16.

**User Data Low Byte (Offset 0x18)**

7

0

User Data Low Byte
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R

Bit	Field	Value	Description
7-0	User Data Low Byte		Low Byte of User Data. Reading this register will decrement offset 0x16.

The User Data consists of remote or PCB pushbutton codes. A user code will be generated upon IR reception or a user pushbutton being pressed. Both types of inputs repeat at about the same rate. The pushbuttons are debounced. The 32 word IR buffer fills up in about 4.5 seconds. Once full additional inputs are ignored. Reading an empty buffer yields the result 0xDEAD.

IR Remote "0"	0x3000	IR Remote "RIGHTARROW"	0x3010
IR Remote "1"	0x3001	IR Remote "CC"	0x301E
IR Remote "2"	0x3002	IR Remote "DOWN ARROW"	0x3021
IR Remote "3"	0x3003	IR Remote "PREV CH"	0x3022
IR Remote "4"	0x3004	IR Remote "SLEEP"	0x3026
IR Remote "5"	0x3005	IR Remote "REW"	0x30CA
IR Remote "6"	0x3006	IR Remote "PLAY"	0x3175
IR Remote "7"	0x3007	IR Remote "FF"	0x3174
IR Remote "8"	0x3008	IR Remote "REC"	0x3177
IR Remote "9"	0x3009	IR Remote "STOP"	0x3176
IR Remote "ENTER"	0x3022	IR Remote "PAUSE"	0x3169
IR Remote "TV/VCR"	0x30EC	PCB Pushbutton SW12 ("OK")	0x00D8
IR Remote "SELECT"	0x300F	PCB Pushbutton SW13 ("UP")	0x00B8
IR Remote "UP ARROW"	0x3020	PCB Pushbutton SW11 ("DN")	0x00E8
IR Remote "IN/OUT"	0x302E	PCB Pushbutton SW14 ("LT")	0x0078
IR Remote "LEFT ARROW"	0x3011	PCB Pushbutton SW10 ("RT")	0x00F0
IR Remote "OK"	0x300D		