NOTES, UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES IN OHMS.
2. CAPACTITANCE VALUES IN MICROFARADS.
3. REFERENCE DESIGNATORS USED:

4. ALL 0.1 uF AND 0.01uF CAPACITORS ARE DECOUPLING CAPS UNLESS OTHERWISE NOTED. THEY ARE SHOWN ON THE PAGE WITH THE INTEGRATED CIRCUITS THEY SHOULD BE PLACED NEAR.
5. OBSERVE THE FOLLOWING LAYOUT NOTES:
6. BOARD PROPERTIES

   A. ROUTE TO WITHIN 10% OF MANHATTAN DISTANCE
   B. 50 +/- 5 OHM MATCHED IMPEDANCE
   C. OUTER LAYERS 0.5 OZ CU /W 0.5 OZ AU PLATING
   D. INNER LAYERS 1.0 OZ CU
   E. FR4 BOARD MATERIAL
   F. MINIMUM TRACE WIDTH/SPACING 4 MILS
   G. MINIMUM VIA SIZE 10/19 MIL
   H. LAYER STACKUP:

      1. TOP - SIGNAL ROUTING
      2. GROUND PLANE
      3. INNER1 - SIGNAL ROUTING
      4. VCC3 PLANE (3.3V BOARD)
      5. INNER2 - SIGNAL ROUTING
      6. INNER3 - SIGNAL ROUTING
      7. VCC PLANE 2
      8. INNER4 - SIGNAL ROUTING
      9. GROUND PLANE
      10. BOTTOM - SIGNAL ROUTING

SCHEMATIC INDEX

REV	DESCRIPTION	DATE	APPROVED
A	Initial schematic ready for layout.	01/07/03	RRP
B	Sheet 2: Changed LENDIAN_MODE signal so R221 is a pull-up and S2 provides a pull-down. Sheet 3: Swapped DSP_SCL0 and DSP_SDA0 signals going to U16. Sheet 7: Added series terminations RN28, R246, R247, & R248. Sheet 11: Routed DC_A[8:6], UART_CSA#, & UART_CSB# to U15. Sheet 13: Changed bus routed to U53 to VP0D[9:2] and U52 to VP1D[9:2]. Sheet 15: Added pull-up (R241) to DC_ARDY. Sheet 17: Pin 177 is Ground not VCC Sheet 20: Changed U36 & U37 to SN74LVC1G125DCKR.	04/01/03	RRP
C	Sheet 2: Changed EMAC_ENABLE to autodect S2 is now 2 position switch. Sheet 3: Routed FPGALOCK to pullup R101 to lock FPGA programming Sheet 7: Implemented EMAC_ENABLE Autodetect on U41-1A, added R249 Sheet 11: Added TCE2# ,TCE3#, SOE3# to U15 Decoder. Sheet 16: Swapped pins 141 and 149 on FPGA for HDTV speed paths, changed fpga to -7 part Sheet 17: Added AND Gate U55 to Lock FPGA programming, changed FPGA to -7 Sheet 20: Swapped Red and Blue on VGA Connector. Removed R102,R129,R183 Sheet 22: Added R250 for HPI option	05/15/03	RRP
D	Sheet 10: Changed Buffers U2,U3,U4,U5 to non-holder type SN74LVT16245B Sheet 18: Changed crystal capacitors C168 and C169 from 18pF to 33 pF Sheet 19: Changed crystal capacitors C288 and C289 from 18pF to 33 pF Sheet 20: Changed Value on output termination R82,R130,R184 from 75 ohms to 82 ohms.	08/01/03	RRP
D	Sheet 03: Changed Oscillator U26 to 60MHz. For -0003 version of 506840	08/01/04	RRP

REVISION STATUS OF SHEETS

REV	A	C	A	A	B							
SH	21	22	23	24	25							
REV	C	A	B	A	B	C	C	D	D	D		
SH	11	12	13	14	15	16	17	18	19	20		
REV	D	C	D	A	A	A	C	B	A	D	NEXT ASSY	USED ON
SH	1	2	3	4	5	6	7	8	9	10	APPLICATION	

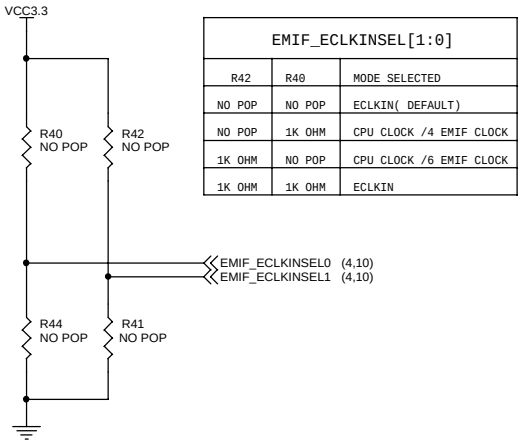
DWN	R.R.P.	DATE 03/30/2003
CHK	T.W.K.	DATE 03/30/2003
ENGR	R.R.P.	DATE 03/30/2003
ENGR-MGR	R.R.P.	DATE 03/30/2003
QA	C.M.D.	DATE 03/30/2003
MFG	R.R.P.	DATE 03/30/2003
RLSE	R.R.P.	DATE 03/30/2003

SPECTRUM DIGITAL INCORPORATED

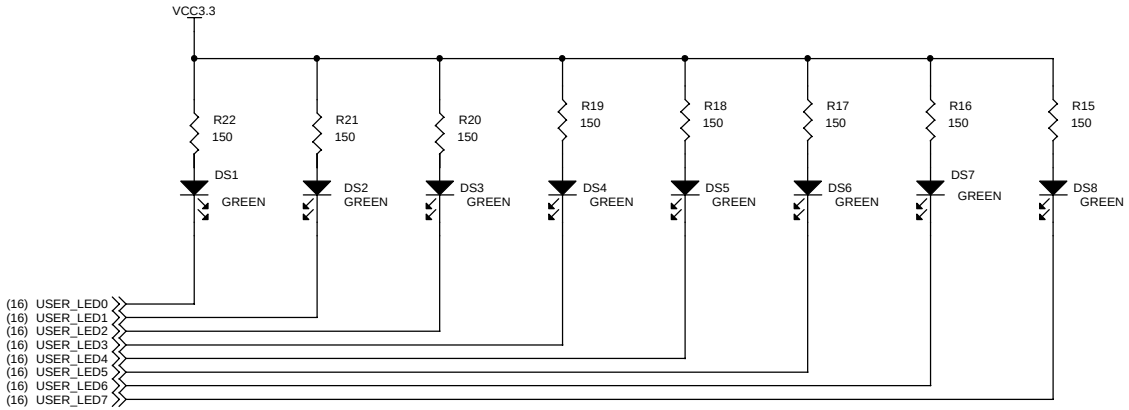
Title: DM642 Evaluation Module

Size B | Document Number: 506842 | Rev D

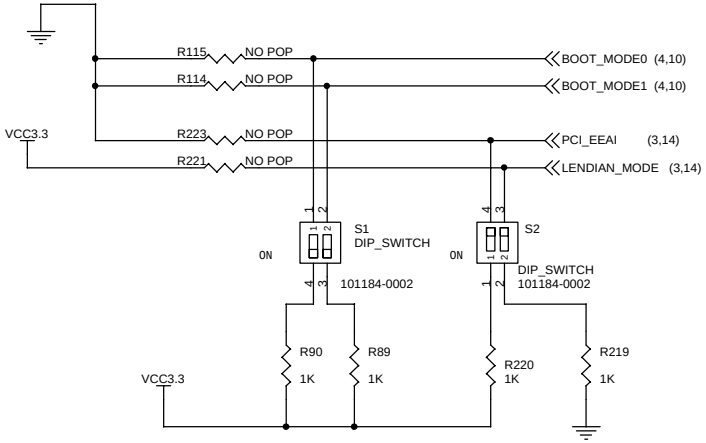
Date: Monday, September 20, 2004 | Sheet 1 of 25



EMIF_ECLKINSEL[1:0]		
R42	R40	MODE SELECTED
NO POP	NO POP	ECLKIN(DEFAULT)
NO POP	1K OHM	CPU CLOCK /4 EMIF CLOCK
1K OHM	NO POP	CPU CLOCK /6 EMIF CLOCK
1K OHM	1K OHM	ECLKIN



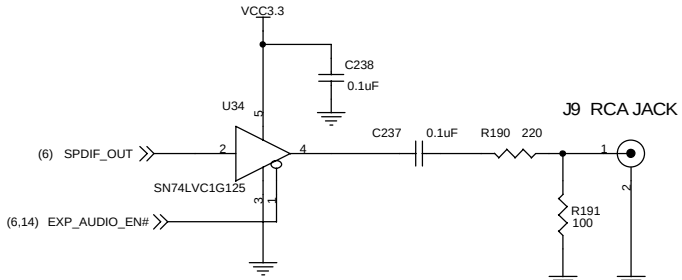
USER LEDS



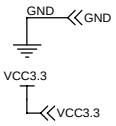
BOOT_MODE[1:0]		
S1-2	S1-1	MODE SELECTED
OFF	OFF	NO BOOT (DEFAULT)
OFF	ON	HPI/PCI BOOT MODE
ON	OFF	RESERVED
ON	ON	EMIF 8 BIT ROM BOOT

PCI MODE CONFIGURATION	
S2-1(PCI ROM)	MODE SELECTED
OFF	PCI EEPROM DISABLED(DEFAULT)
ON	PCI ROM ENABLED

ENDIAN MODE CONFIGURATION	
S2-2(ENDIAN)	MODE SELECTED
OFF	LITTLE ENDIAN MODE (DEFAULT)
ON	BIG ENDIAN MODE



SPDIF BLOCK



LEDS/SWITCHES/CONFIGURATION INPUTS

SPECTRUM DIGITAL. INCORPORATED

Title: DM642 EVALUATION MODULE		
Size: B	Document Number: 506842	Rev: C
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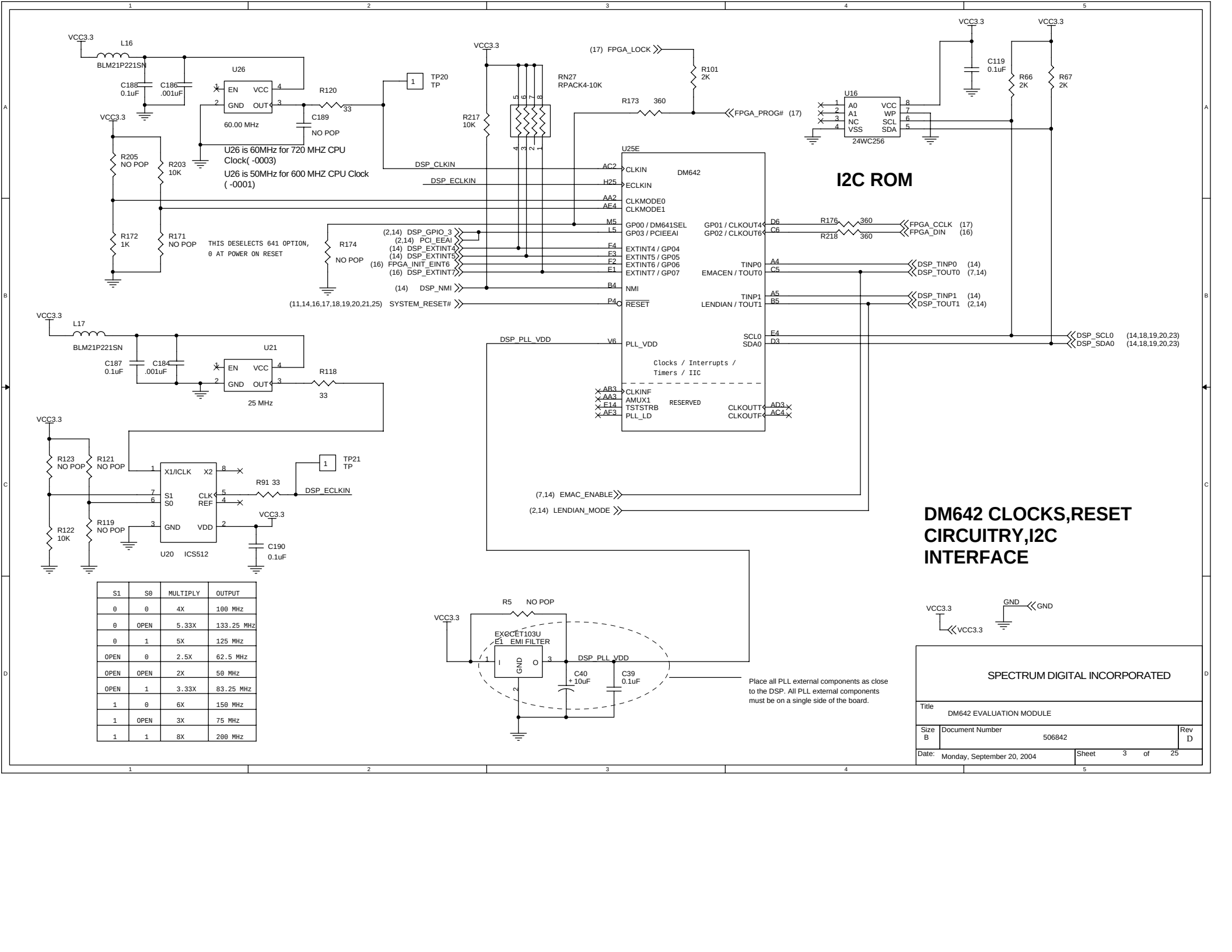
VCC3.3
L16
BLM21P221SN
C188 0.1uF
C186 .001uF
U26
EN VCC GND OUT
60.00 MHz
R120 33
C189 NO POP
TP20 TP
U26 is 60MHz for 720 MHZ CPU Clock(-0003)
U26 is 50MHz for 600 MHZ CPU Clock (-0001)
R205 NO POP
R203 10K
R172 1K
R171 NO POP
THIS DESELECTS 641 OPTION, 0 AT POWER ON RESET
R174 NO POP
RN27 RPACK4-10K
R217 10K
(17) FPGA_LOCK
R101 2K
R173 360
FPGA_PROG# (17)
U16
A0 A1 NC VSS VCC WP SCL SDA
24WC256
C119 0.1uF
R66 2K
R67 2K
I2C ROM
U25E
DM642
DSP_CLKIN
DSP_ECLKIN
AC2 CLKIN
H25 ECLKIN
AA2 CLKMODE0
AE4 CLKMODE1
M5 GP00 / DM641SEL
L5 GP03 / PCIEEAI
(2,14) DSP_GPIO_3
(2,14) PCI_EEAI
(14) DSP_EXTINT4
(14) DSP_EXTINT5
(16) FPGA_INIT_EINT6
(16) DSP_EXTINT7
F4 EXTINT4 / GP04
F3 EXTINT5 / GP05
F2 EXTINT6 / GP06
E1 EXTINT7 / GP07
(14) DSP_NMI
B4 NMI
(11,14,16,17,18,19,20,21,25) SYSTEM_RESET#
P4 RESET
GP01 / CLKOUT4 D6
GP02 / CLKOUT6 C6
R176 360
R218 360
FPGA_CCLK (17)
FPGA_DIN (16)
TINP0 A4
EMACEN / TOUT0 C5
DSP_TINP0 (14)
DSP_TOUT0 (7,14)
TINP1 A5
LENDIAN / TOUT1 B5
DSP_TINP1 (14)
DSP_TOUT1 (2,14)
SCL0 E4
SDA0 D3
DSP_SCL0 (14,18,19,20,23)
DSP_SDA0 (14,18,19,20,23)
DSP_PLL_VDD
V6 PLL_VDD
Clocks / Interrupts / Timers / IIC
AB3 CLKINF
AA3 AMUX1
F14 TSTSTRB
AF3 PLL_LD
RESERVED
CLKOUTT AD3
CLKOUTF AC4
(7,14) EMAC_ENABLE
(2,14) LENDIAN_MODE
L17
BLM21P221SN
C187 0.1uF
C184 .001uF
U21
R118 33
25 MHz
R123 NO POP
R121 NO POP
R122 10K
R119 NO POP
X1/ICLK X2 S1 S0 CLK REF GND VDD
U20 ICS512
R91 33
TP21 TP
DSP_ECLKIN
C190 0.1uF
S1 S0 MULTIPLY OUTPUT
0 0 4X 100 MHz
0 OPEN 5.33X 133.25 MHz
0 1 5X 125 MHz
OPEN 0 2.5X 62.5 MHz
OPEN OPEN 2X 50 MHz
OPEN 1 3.33X 83.25 MHz
1 0 6X 150 MHz
1 OPEN 3X 75 MHz
1 1 8X 200 MHz
R5 NO POP
EXCCET103U
E1 EMI FILTER
I GND O
C40 + 10uF
C39 0.1uF
Place all PLL external components as close to the DSP. All PLL external components must be on a single side of the board.
GND
DM642 CLOCKS,RESET CIRCUITRY,I2C INTERFACE
SPECTRUM DIGITAL INCORPORATED
Title DM642 EVALUATION MODULE
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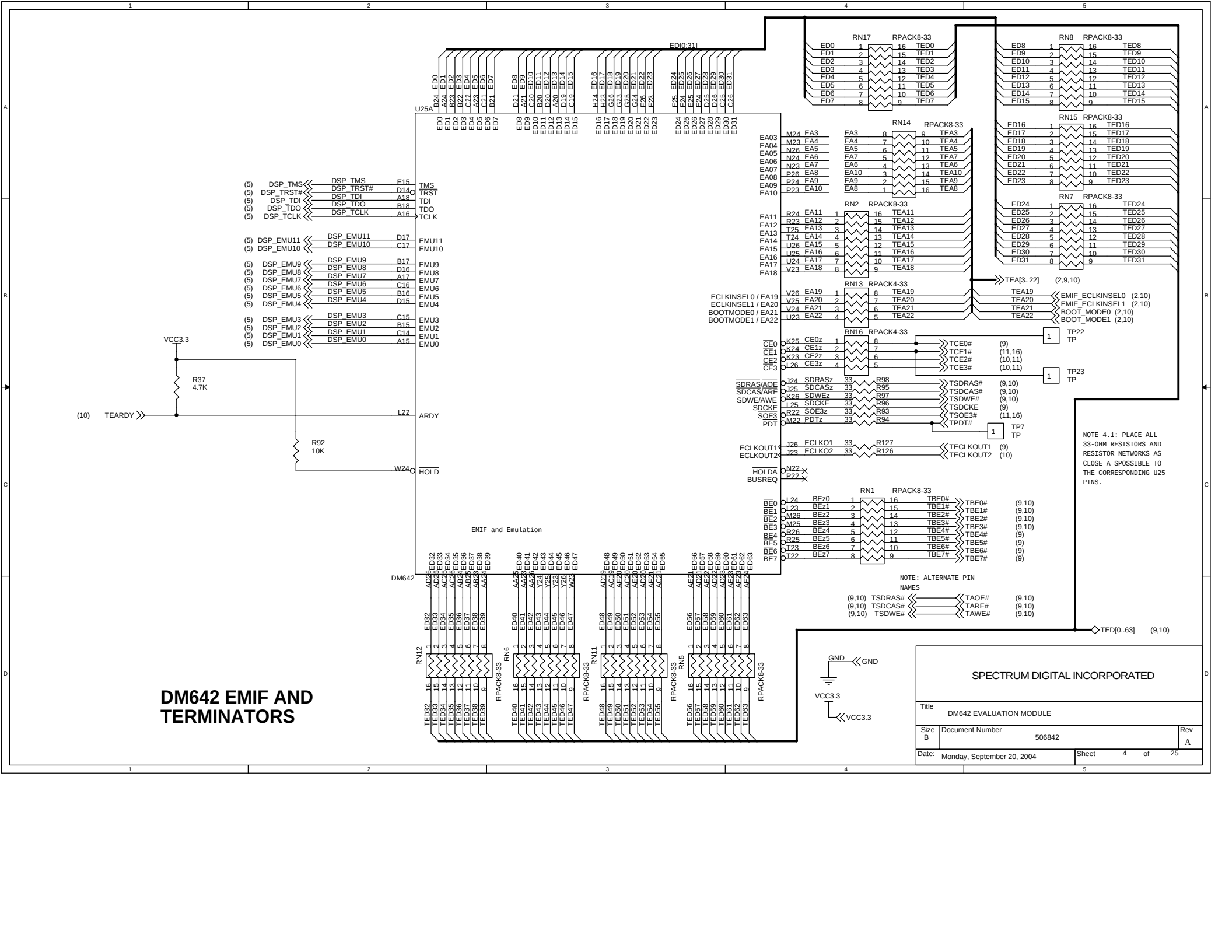
DM642 EMIF AND TERMINATORS
U25A
ED[0:31]
EMIF and Emulation
DM642
DSP_TMS
DSP_TRST#
DSP_TDI
DSP_TDO
DSP_TCLK
DSP_EMU11
DSP_EMU10
DSP_EMU9
DSP_EMU8
DSP_EMU7
DSP_EMU6
DSP_EMU5
DSP_EMU4
DSP_EMU3
DSP_EMU2
DSP_EMU1
DSP_EMU0
TMS
TRST
TDI
TDO
TCLK
EMU11
EMU10
EMU9
EMU8
EMU7
EMU6
EMU5
EMU4
EMU3
EMU2
EMU1
EMU0
HOLD
ARDY
TEARDY
VCC3.3
R37
4.7K
R92
10K
RN17
RN8
RN14
RN15
RN2
RN7
RN13
RN16
RN1
RN12
RN6
RN11
RN5
RPACK8-33
RPACK4-33
TEA[3..22]
TEA19
TEA20
TEA21
TEA22
EMIF_ECLKINSEL0 (2,10)
EMIF_ECLKINSEL1 (2,10)
BOOT_MODE0 (2,10)
BOOT_MODE1 (2,10)
TP22
TP23
TP7
TP
TCE0#
TCE1#
TCE2#
TCE3#
TSDRAS#
TSDCAS#
TSDWE#
TSDCKE
TSOE3#
TPDT#
TECLKOUT1
TECLKOUT2
TBE0#
TBE1#
TBE2#
TBE3#
TBE4#
TBE5#
TBE6#
TBE7#
NOTE 4.1: PLACE ALL 33-OHM RESISTORS AND RESISTOR NETWORKS AS CLOSE A SPOSSIBLE TO THE CORRESPONDING U25 PINS.
NOTE: ALTERNATE PIN NAMES
TAOE#
TARE#
TAWE#
TED[0..63]
GND
VCC3.3
SPECTRUM DIGITAL INCORPORATED
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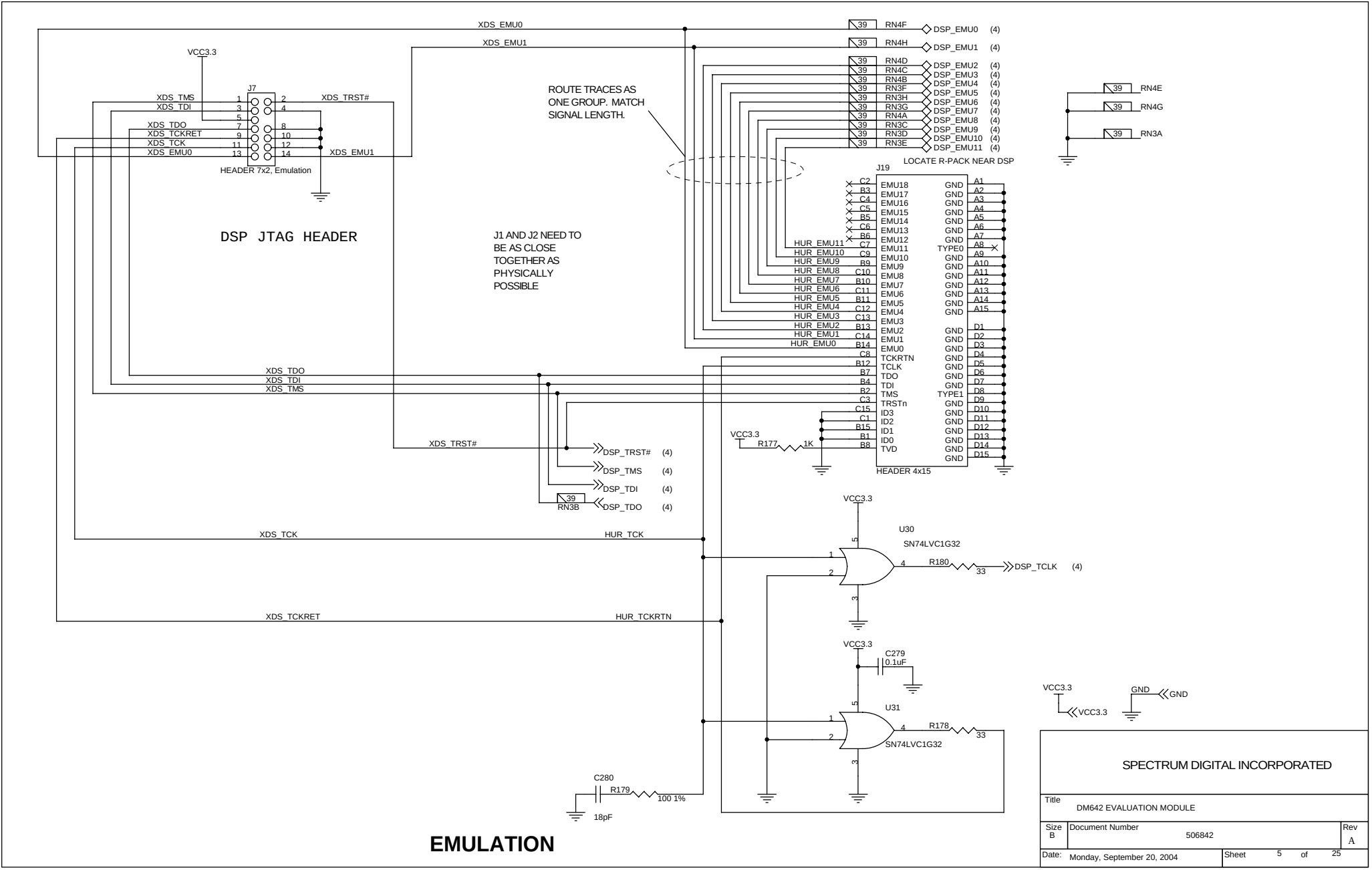
XDS_EMU0
XDS_EMU1
VCC3.3
J7
XDS_TMS
XDS_TDI
XDS_TDO
XDS_TCKRET
XDS_TCK
XDS_EMU0
XDS_TRST#
XDS_EMU1
HEADER 7x2, Emulation
DSP JTAG HEADER
ROUTE TRACES AS ONE GROUP. MATCH SIGNAL LENGTH.
J1 AND J2 NEED TO BE AS CLOSE TOGETHER AS PHYSICALLY POSSIBLE
RN4F
RN4H
RN4D
RN4C
RN4B
RN3F
RN3H
RN3G
RN4A
RN3C
RN3D
RN3E
DSP_EMU0 (4)
DSP_EMU1 (4)
DSP_EMU2 (4)
DSP_EMU3 (4)
DSP_EMU4 (4)
DSP_EMU5 (4)
DSP_EMU6 (4)
DSP_EMU7 (4)
DSP_EMU8 (4)
DSP_EMU9 (4)
DSP_EMU10 (4)
DSP_EMU11 (4)
LOCATE R-PACK NEAR DSP
RN4E
RN4G
RN3A
J19
HUR_EMU11
HUR_EMU10
HUR_EMU9
HUR_EMU8
HUR_EMU7
HUR_EMU6
HUR_EMU5
HUR_EMU4
HUR_EMU3
HUR_EMU2
HUR_EMU1
HUR_EMU0
EMU18
EMU17
EMU16
EMU15
EMU14
EMU13
EMU12
EMU11
EMU10
EMU9
EMU8
EMU7
EMU6
EMU5
EMU4
EMU3
EMU2
EMU1
EMU0
TCKRTN
TCLK
TDO
TDI
TMS
TRSTn
ID3
ID2
ID1
ID0
TVD
TYPE0
TYPE1
GND
HEADER 4x15
XDS_TDO
XDS_TDI
XDS_TMS
XDS_TRST#
DSP_TRST# (4)
DSP_TMS (4)
DSP_TDI (4)
DSP_TDO (4)
RN3B
VCC3.3
R177
1K
XDS_TCK
HUR_TCK
U30
SN74LVC1G32
R180
33
DSP_TCLK (4)
XDS_TCKRET
HUR_TCKRTN
C279
0.1uF
U31
R178
33
SN74LVC1G32
C280
R179
100 1%
18pF
GND
SPECTRUM DIGITAL INCORPORATED
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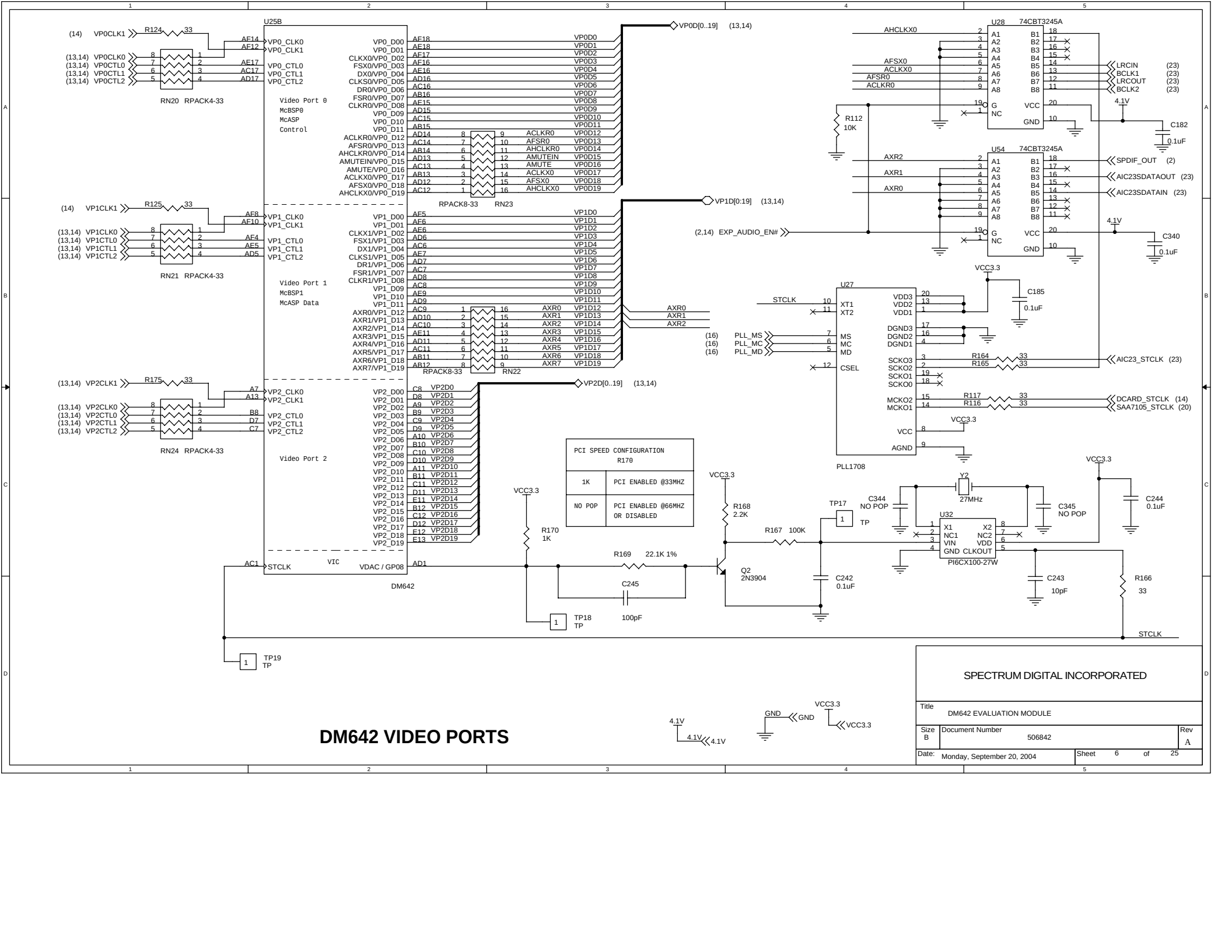
EMULATION



DM642 VIDEO PORTS

SPECTRUM DIGITAL INCORPORATED

Title	DM642 EVALUATION MODULE	
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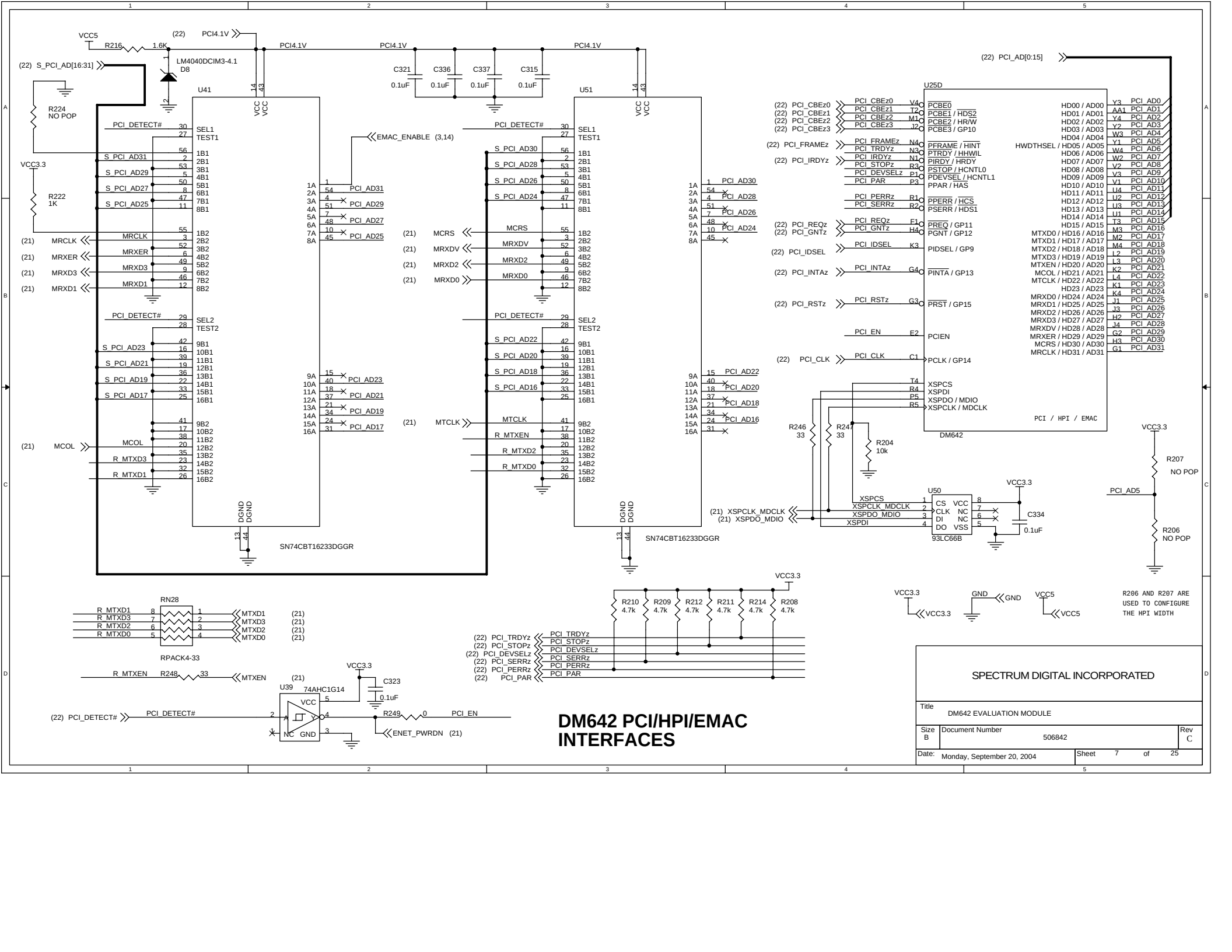
VCC5
R216 1.6K
(22) PCI4.1V
LM4040DCIM3-4.1
D8
(22) S_PCI_AD[16:31]
R224 NO POP
VCC3.3
R222 1K
U41
U51
C321 0.1uF
C336 0.1uF
C337 0.1uF
C315 0.1uF
PCI_DETECT#
SEL1
TEST1
SEL2
TEST2
EMAC_ENABLE (3,14)
S_PCI_AD31
S_PCI_AD29
S_PCI_AD27
S_PCI_AD25
S_PCI_AD30
S_PCI_AD28
S_PCI_AD26
S_PCI_AD24
S_PCI_AD23
S_PCI_AD21
S_PCI_AD19
S_PCI_AD17
S_PCI_AD22
S_PCI_AD20
S_PCI_AD18
S_PCI_AD16
(21) MRCLK
(21) MRXER
(21) MRXD3
(21) MRXD1
(21) MRXDV
(21) MRXD2
(21) MRXD0
(21) MCRS
(21) MCOL
(21) MTCLK
R_MTXD3
R_MTXD1
R_MTXEN
R_MTXD2
R_MTXD0
PCI_AD31
PCI_AD29
PCI_AD27
PCI_AD25
PCI_AD23
PCI_AD21
PCI_AD19
PCI_AD17
PCI_AD30
PCI_AD28
PCI_AD26
PCI_AD24
PCI_AD22
PCI_AD20
PCI_AD18
PCI_AD16
DGND
SN74CBT16233DGGR
(22) PCI_AD[0:15]
U25D
(22) PCI_CBEz0
(22) PCI_CBEz1
(22) PCI_CBEz2
(22) PCI_CBEz3
(22) PCI_FRAMEz
(22) PCI_IRDYz
(22) PCI_REQz
(22) PCI_GNTz
(22) PCI_IDSEL
(22) PCI_INTAz
(22) PCI_RSTz
(22) PCI_CLK
PCI_EN
PCBE0
PCBE1 / HDS2
PCBE2 / HR/W
PCBE3 / GP10
PFRAME / HINT
PTRDY / HHWIL
PIRDY / HRDY
PSTOP / HCNTL0
PDEVSEL / HCNTL1
PPAR / HAS
PPERR / HCS
PSERR / HDS1
PREQ / GP11
PGNT / GP12
PIDSEL / GP9
PINTA / GP13
PRST / GP15
PCIEN
PCLK / GP14
XSPCS
XSPDI
XSPDO / MDIO
XSPCLK / MDCLK
PCI / HPI / EMAC
DM642
HWDTHSEL / HD05 / AD05
R246 33
R247 33
R204 10k
U50
93LC66B
C334 0.1uF
(21) XSPCLK_MDCLK
(21) XSPDO_MDIO
R207 NO POP
R206 NO POP
PCI_AD5
RN28
RPACK4-33
R_MTXD1
R_MTXD3
R_MTXD2
R_MTXD0
MTXD1
MTXD3
MTXD2
MTXD0
R_MTXEN
R248 33
MTXEN
U39
74AHC1G14
C323 0.1uF
(22) PCI_DETECT#
R249 0
PCI_EN
ENET_PWRDN (21)
R210 4.7k
R209 4.7k
R212 4.7k
R211 4.7k
R214 4.7k
R208 4.7k
(22) PCI_TRDYz
(22) PCI_STOPz
(22) PCI_DEVSELz
(22) PCI_SERRz
(22) PCI_PERRz
(22) PCI_PAR
GND
R206 AND R207 ARE USED TO CONFIGURE THE HPI WIDTH
DM642 PCI/HPI/EMAC INTERFACES
SPECTRUM DIGITAL INCORPORATED
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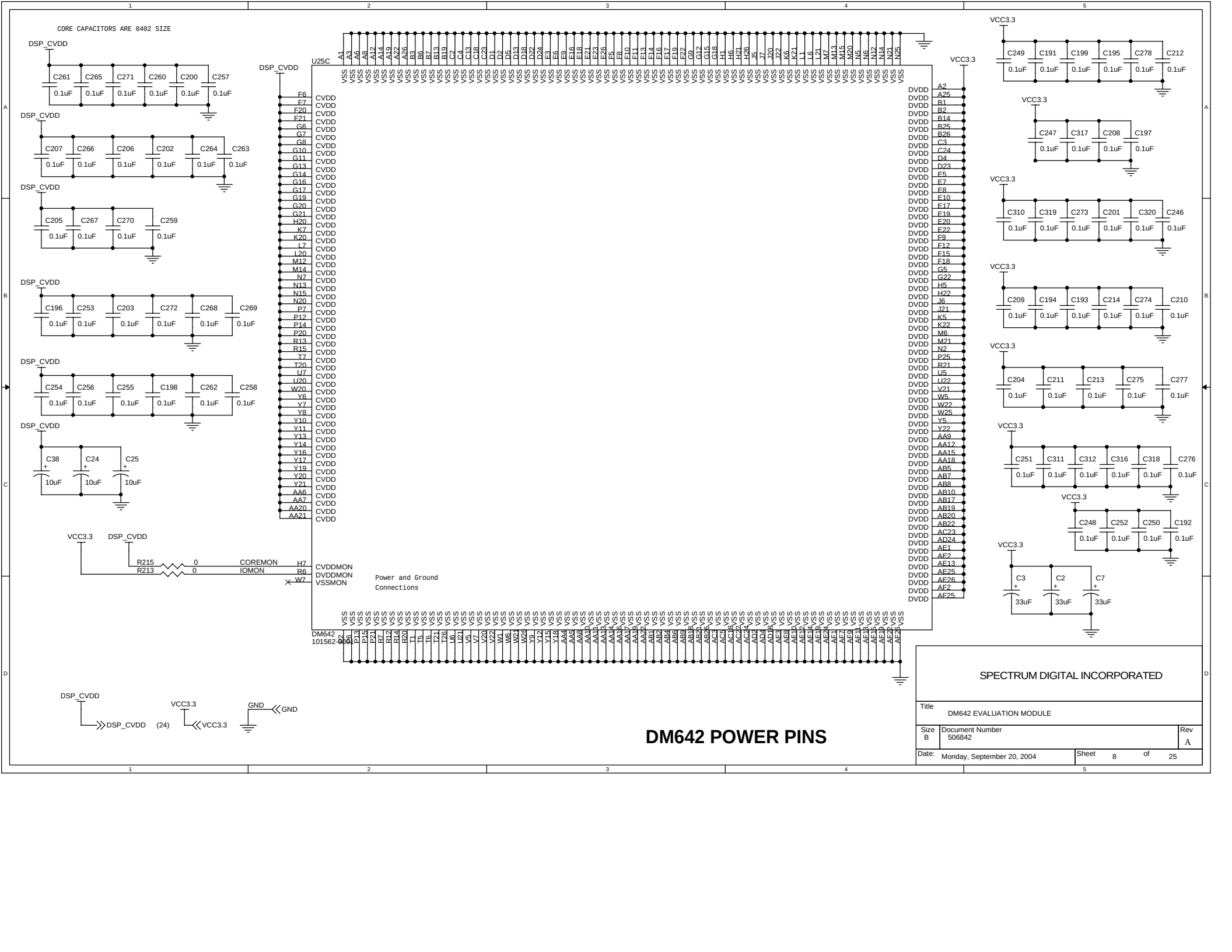
CORE CAPACITORS ARE 0402 SIZE
DSP_CVDD
C261 C265 C271 C260 C200 C257
0.1uF
C207 C266 C206 C202 C264 C263
C205 C267 C270 C259
C196 C253 C203 C272 C268 C269
C254 C256 C255 C198 C262 C258
C38 C24 C25
10uF
U25C
CVDD
VSS
DVDD
VCC3.3
C249 C191 C199 C195 C278 C212
C247 C317 C208 C197
C310 C319 C273 C201 C320 C246
C209 C194 C193 C214 C274 C210
C204 C211 C213 C275 C277
C251 C311 C312 C316 C318 C276
C248 C252 C250 C192
C3 C2 C7
33uF
R215 0 COREMON
R213 0 IOMON
CVDDMON
DVDDMON
VSSMON
Power and Ground Connections
DM642
101562-0001
GND
(24)
DM642 POWER PINS
SPECTRUM DIGITAL INCORPORATED
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DM642 EVALUATION MODULE
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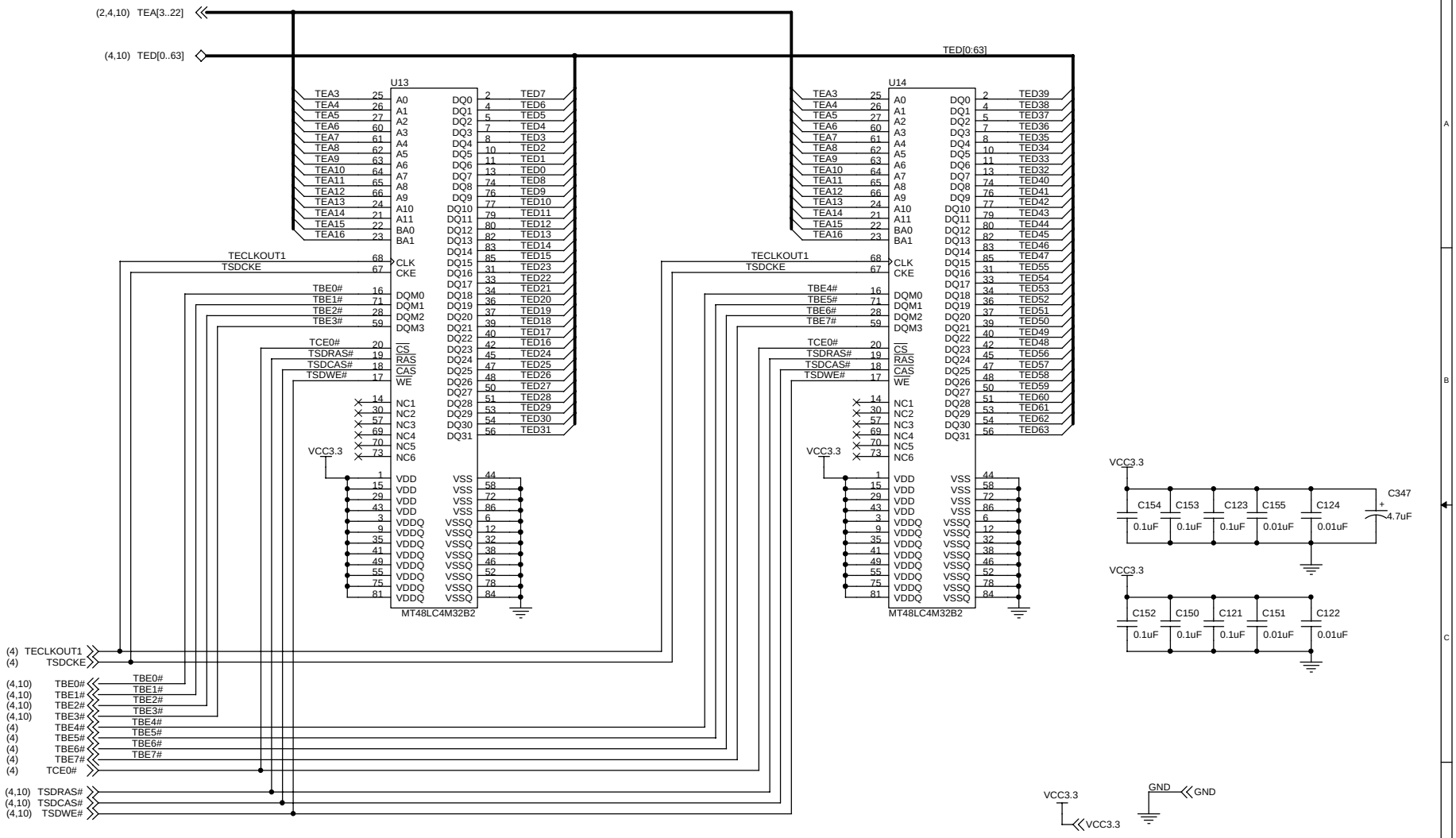

SDRAM MEMORY

SPECTRUM DIGITAL. INCORPORATED

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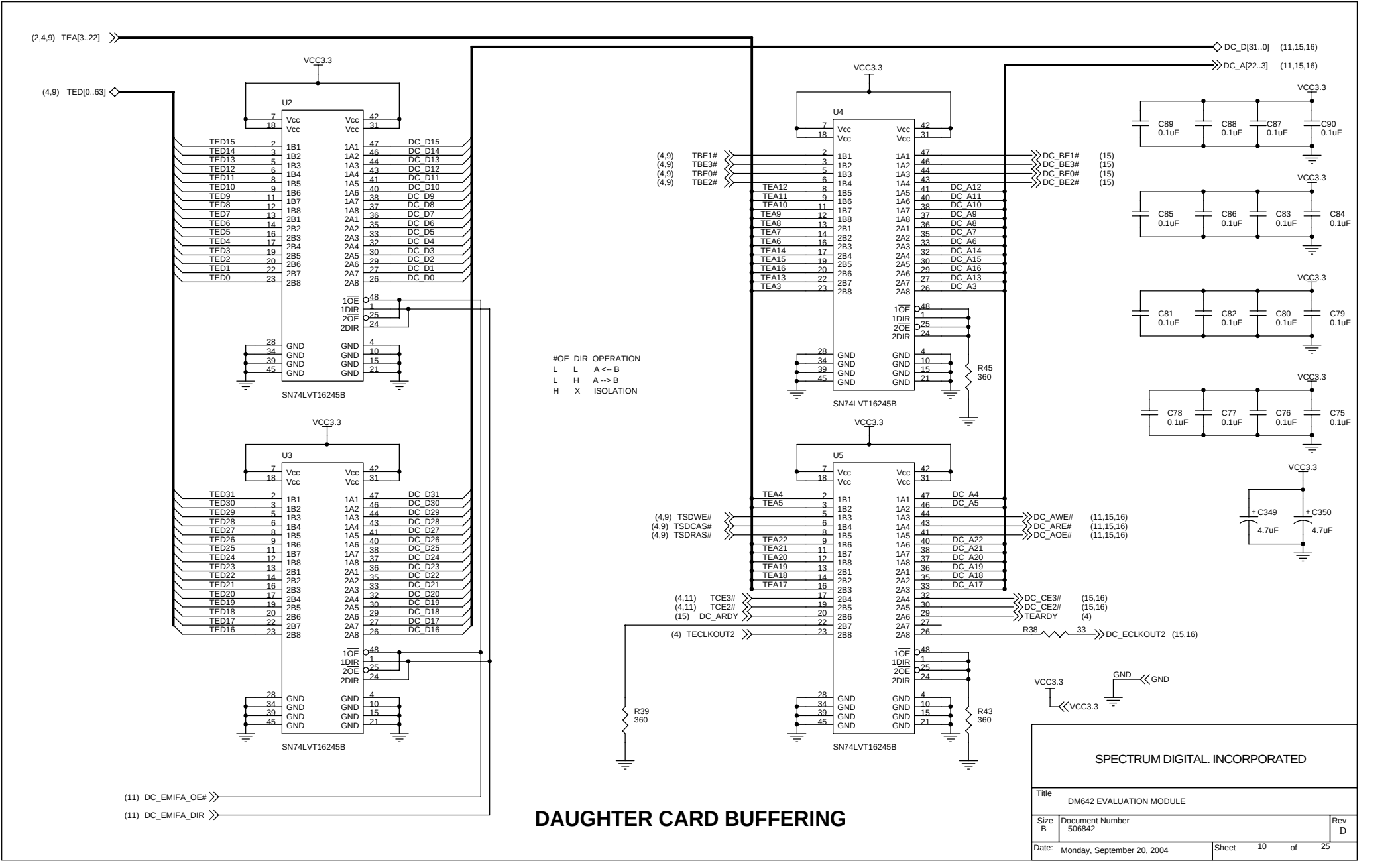

DAUGHTER CARD BUFFERING

SPECTRUM DIGITAL. INCORPORATED

Title: DM642 EVALUATION MODULE		
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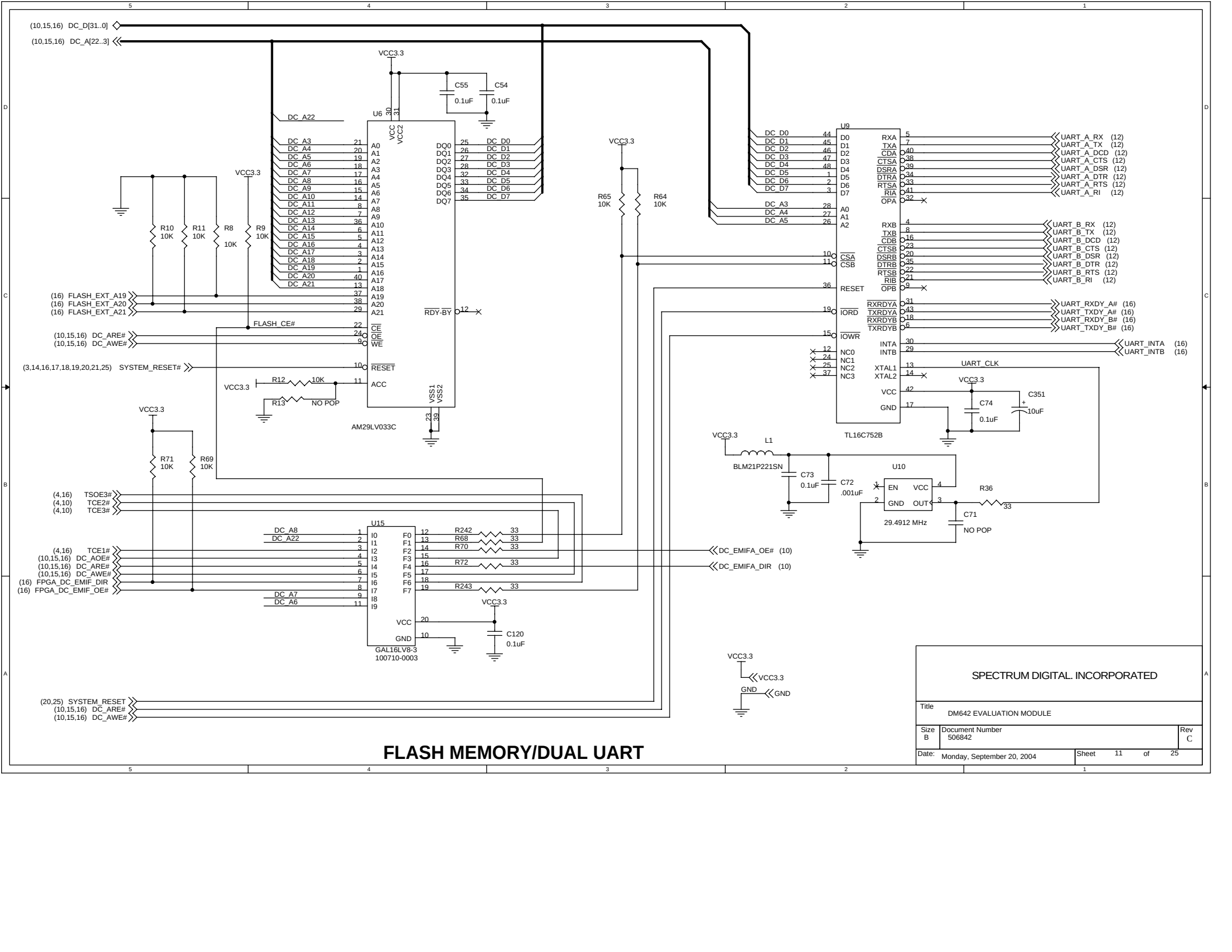
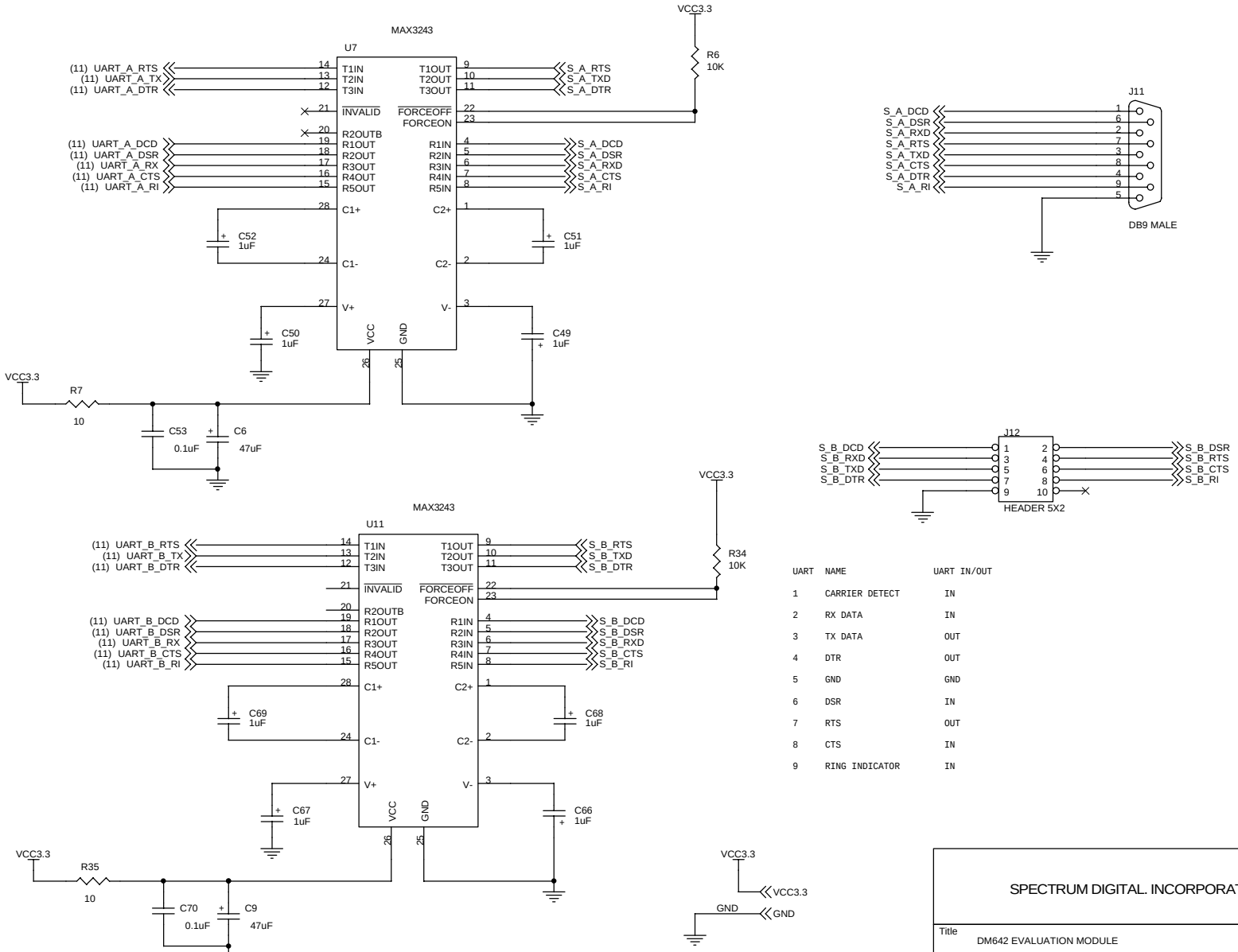


FLASH MEMORY/DUAL UART



UART	NAME	UART IN/OUT
1	CARRIER DETECT	IN
2	RX DATA	IN
3	TX DATA	OUT
4	DTR	OUT
5	GND	GND
6	DSR	IN
7	RTS	OUT
8	CTS	IN
9	RING INDICATOR	IN

UART DRIVERS

SPECTRUM DIGITAL. INCORPORATED

Title: DM642 EVALUATION MODULE		
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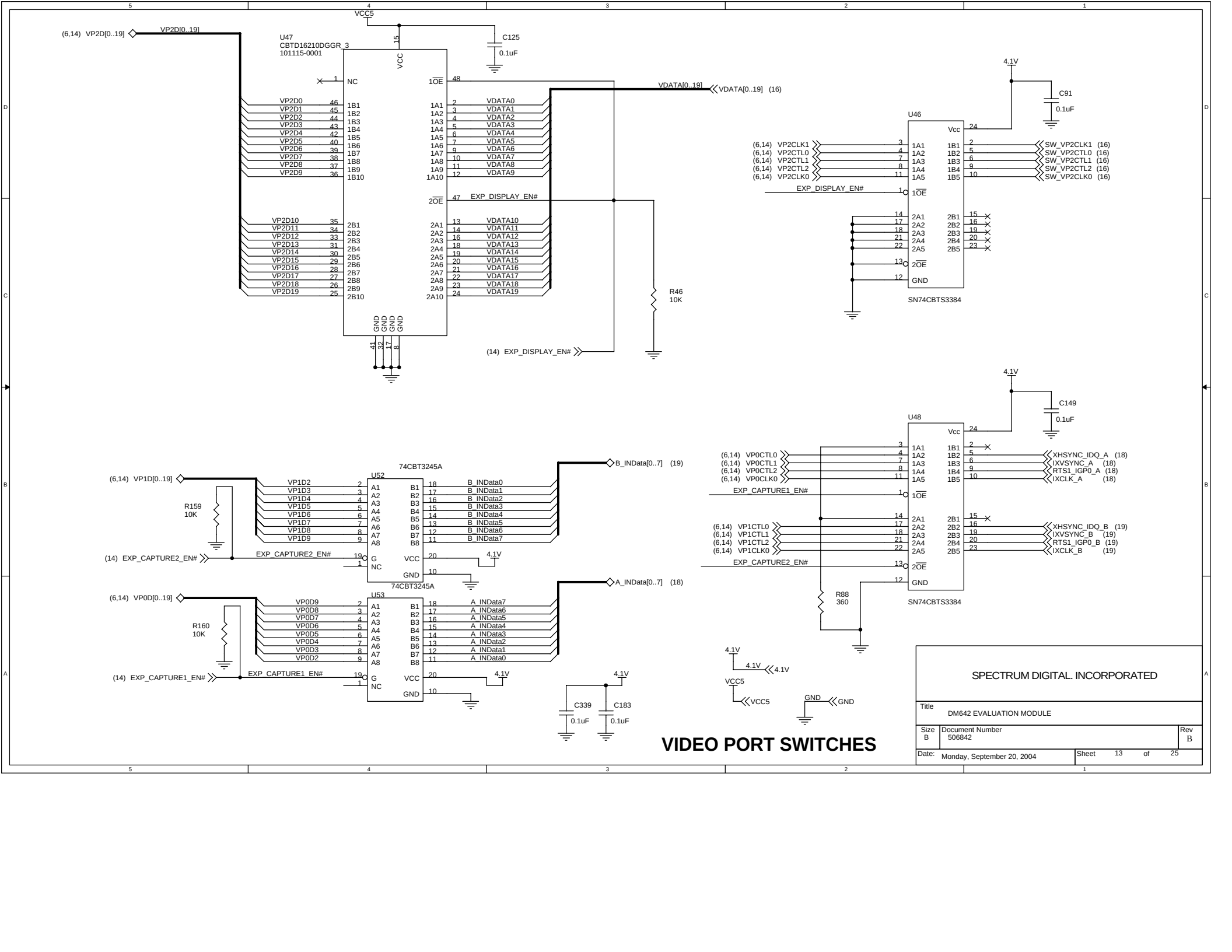
VCC5
(6,14) VP2D[0..19]
VP2D[0..19]
U47
CBTD16210DGGR_3
101115-0001
C125
0.1uF
VCC
NC
1OE
2OE
GND
VDATA[0..19]
VDATA[0..19] (16)
EXP_DISPLAY_EN#
(14) EXP_DISPLAY_EN#
R46
10K
4.1V
C91
0.1uF
U46
Vcc
SN74CBTS3384
(6,14) VP2CLK1
(6,14) VP2CTL0
(6,14) VP2CTL1
(6,14) VP2CTL2
(6,14) VP2CLK0
SW_VP2CLK1 (16)
SW_VP2CTL0 (16)
SW_VP2CTL1 (16)
SW_VP2CTL2 (16)
SW_VP2CLK0 (16)
74CBT3245A
U52
(6,14) VP1D[0..19]
B_INData[0..7] (19)
R159
10K
(14) EXP_CAPTURE2_EN#
EXP_CAPTURE2_EN#
U53
(6,14) VP0D[0..19]
A_INData[0..7] (18)
R160
10K
(14) EXP_CAPTURE1_EN#
EXP_CAPTURE1_EN#
C339
C183
0.1uF
C149
U48
(6,14) VP0CTL0
(6,14) VP0CTL1
(6,14) VP0CTL2
(6,14) VP0CLK0
XHSYNC_IDQ_A (18)
IXVSYNC_A (18)
RTS1_IGP0_A (18)
IXCLK_A (18)
EXP_CAPTURE1_EN#
(6,14) VP1CTL0
(6,14) VP1CTL1
(6,14) VP1CTL2
(6,14) VP1CLK0
XHSYNC_IDQ_B (19)
IXVSYNC_B (19)
RTS1_IGP0_B (19)
IXCLK_B (19)
EXP_CAPTURE2_EN#
R88
360
VCC5
GND
SPECTRUM DIGITAL. INCORPORATED
Title
DM642 EVALUATION MODULE
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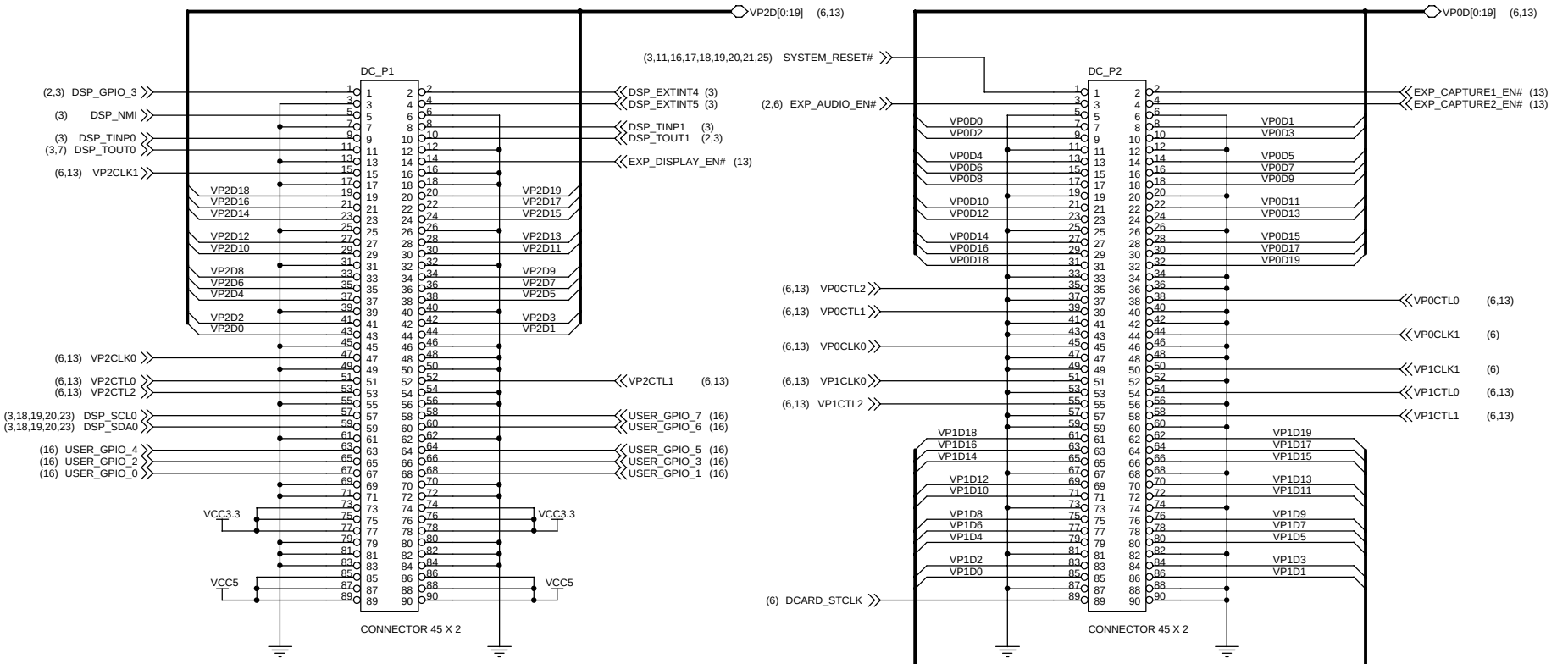
VIDEO PORT SWITCHES



VIDEO PORTS DAUGHTER CARD CONNECTIONS

SPECTRUM DIGITAL. INCORPORATED

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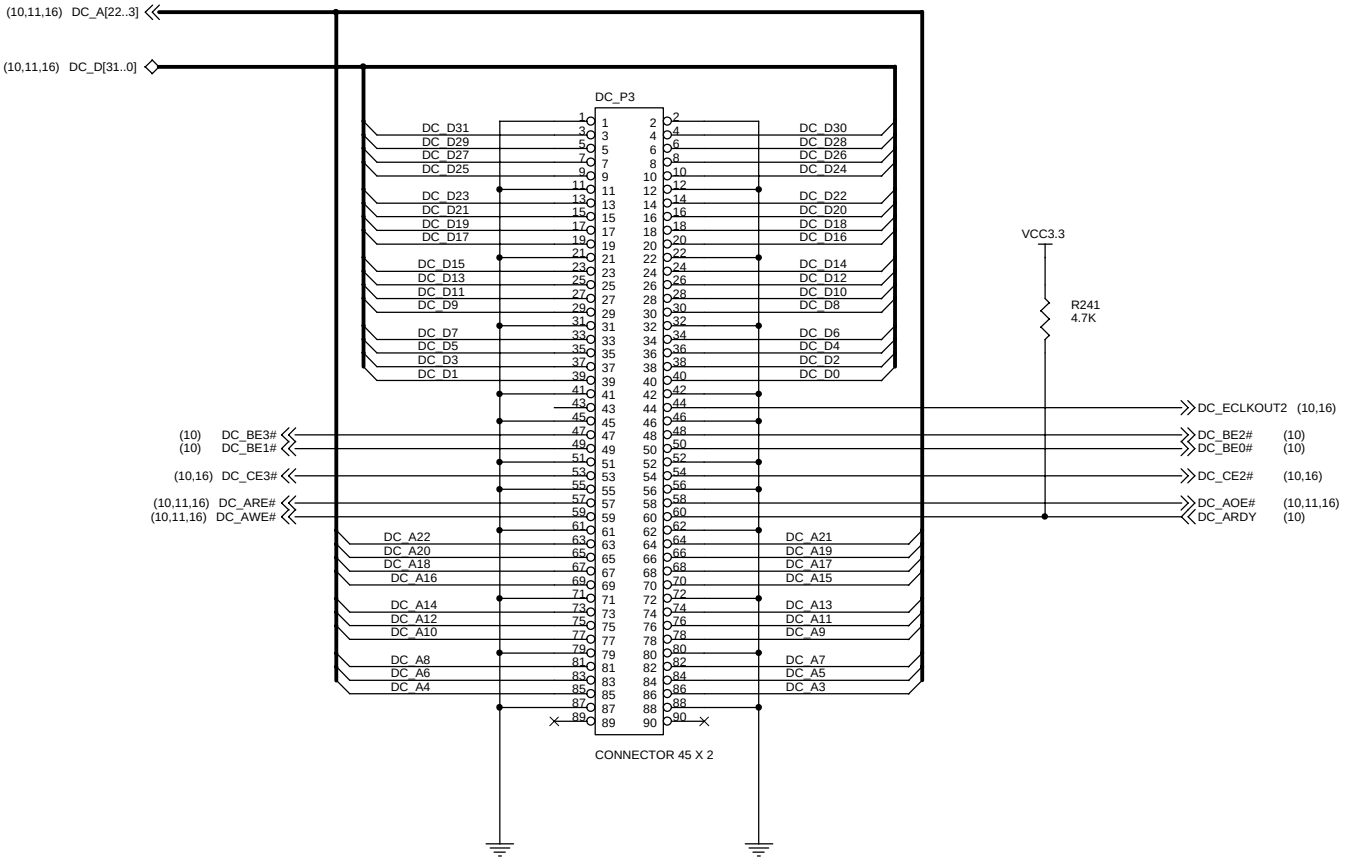

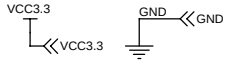

EXTERNAL MEMORY INTERFACE DAUGHTER CARD CONNECTIONS

SPECTRUM DIGITAL. INCORPORATED

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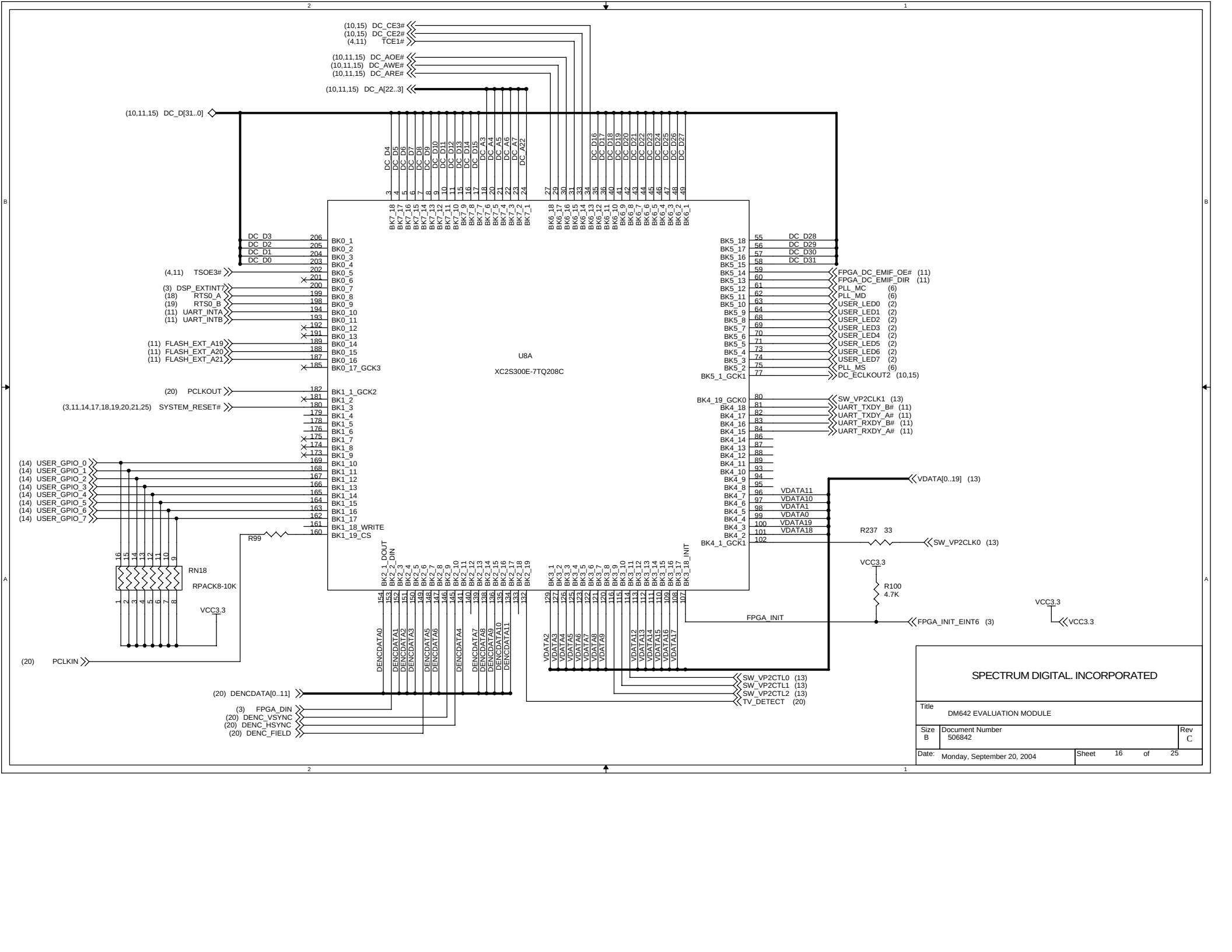

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Title: DM642 EVALUATION MODULE		
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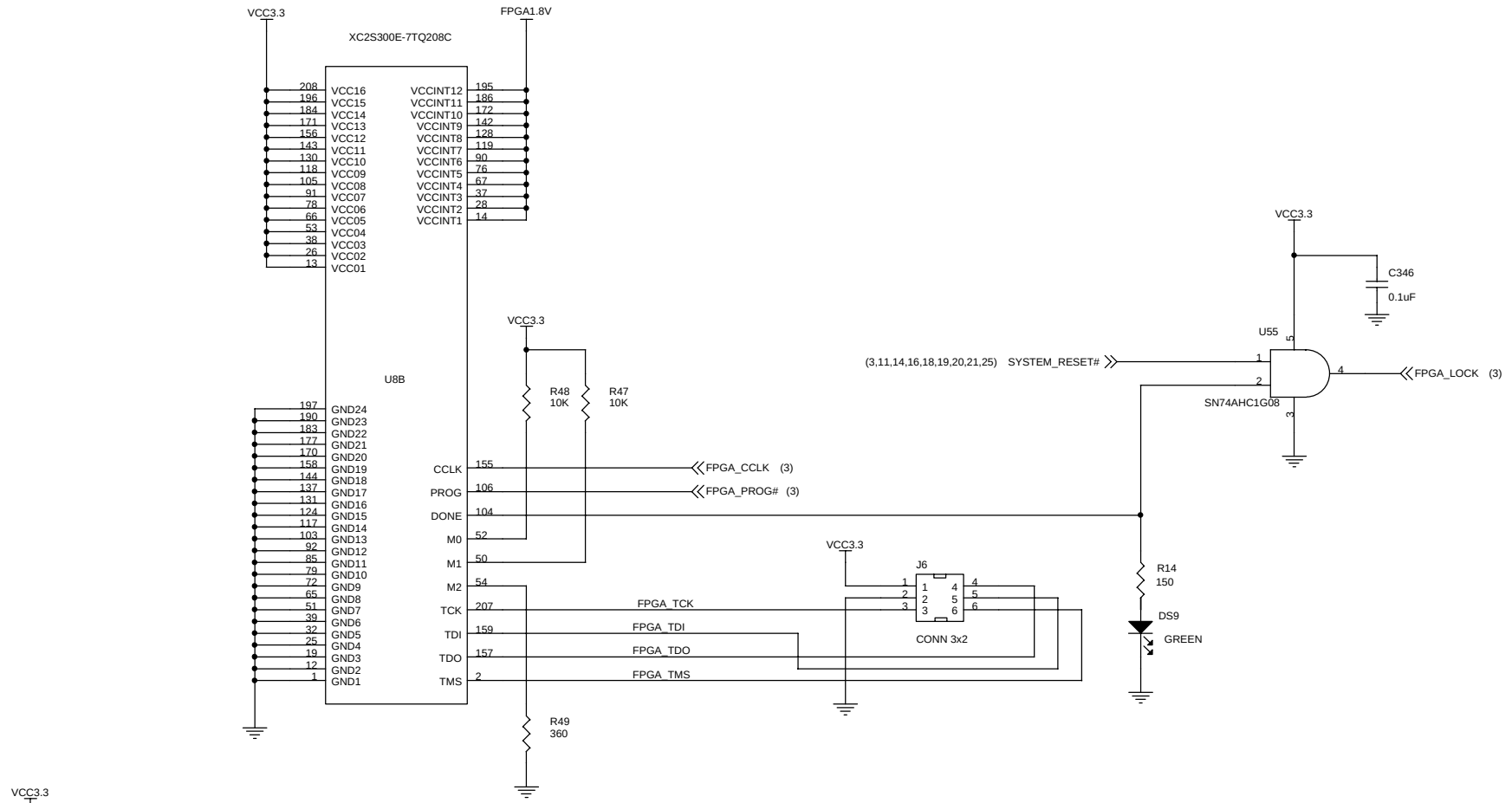

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Title: DM642 EVALUATION MODULE		
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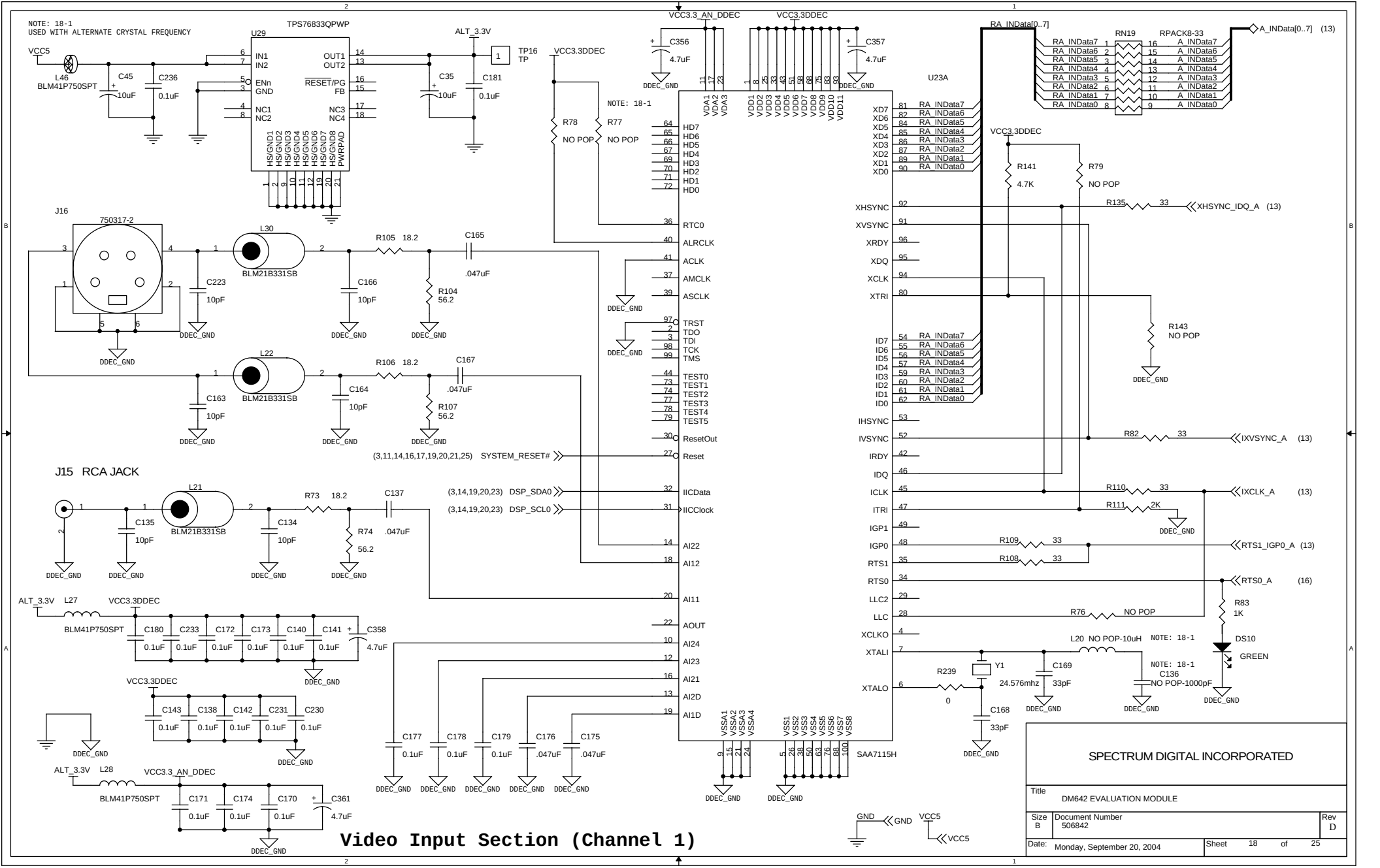
NOTE: 18-1
USED WITH ALTERNATE CRYSTAL FREQUENCY
TPS76833QPWP
U29
VCC5
L46
BLM41P750SPT
C45
10uF
C236
0.1uF
IN1
IN2
ENn
GND
NC1
NC2
OUT1
OUT2
RESET/PG
FB
NC3
NC4
HS/GND1
HS/GND2
HS/GND3
HS/GND4
HS/GND5
HS/GND6
HS/GND7
HS/GND8
PWRPAD
ALT_3.3V
C35
10uF
C181
0.1uF
TP16
TP
VCC3.3DDEC
C356
4.7uF
C357
4.7uF
DDEC_GND
VCC3.3_AN_DDEC
R78
NO POP
R77
NO POP
NOTE: 18-1
U23A
RA_INData[0..7]
RN19
RPACK8-33
A_INData[0..7] (13)
RA_INData7
RA_INData6
RA_INData5
RA_INData4
RA_INData3
RA_INData2
RA_INData1
RA_INData0
A_INData7
A_INData6
A_INData5
A_INData4
A_INData3
A_INData2
A_INData1
A_INData0
R141
4.7K
R79
NO POP
R135
33
XHSYNC_IDQ_A (13)
R143
NO POP
R82
33
IXVSYNC_A (13)
R110
33
IXCLK_A (13)
R111
2K
R109
33
R108
33
RTS1_IGP0_A (13)
RTS0_A (16)
R83
1K
DS10
GREEN
R76
NO POP
L20 NO POP-10uH
NOTE: 18-1
C136
NO POP-1000pF
R239
0
Y1
24.576mhz
C169
33pF
C168
33pF
HD7
HD6
HD5
HD4
HD3
HD2
HD1
HD0
RTC0
ALRCLK
ACLK
AMCLK
ASCLK
TRST
TDO
TDI
TCK
TMS
TEST0
TEST1
TEST2
TEST3
TEST4
TEST5
ResetOut
Reset
IICData
IICClock
AI22
AI12
AI11
AOUT
AI24
AI23
AI21
AI2D
AI1D
XD7
XD6
XD5
XD4
XD3
XD2
XD1
XD0
XHSYNC
XVSYNC
XRDY
XDQ
XCLK
XTRI
ID7
ID6
ID5
ID4
ID3
ID2
ID1
ID0
IHSYNC
IVSYNC
IRDY
IDQ
ICLK
ITRI
IGP1
IGP0
RTS1
RTS0
LLC2
LLC
XCLKO
XTALI
XTALO
SAA7115H
VDA1
VDA2
VDA3
VDD1
VDD2
VDD3
VDD4
VDD5
VDD7
VDD8
VDD9
VDD10
VDD11
VSSA1
VSSA2
VSSA3
VSSA4
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
J16
750317-2
L30
BLM21B331SB
R105 18.2
C165
.047uF
C223
10pF
C166
10pF
R104
56.2
L22
R106 18.2
C167
.047uF
C163
10pF
C164
10pF
R107
56.2
J15 RCA JACK
L21
BLM21B331SB
R73 18.2
C137
.047uF
C135
10pF
C134
10pF
R74
56.2
(3,11,14,16,17,19,20,21,25) SYSTEM_RESET#
(3,14,19,20,23) DSP_SDA0
(3,14,19,20,23) DSP_SCL0
ALT_3.3V
L27
BLM41P750SPT
C180
C233
C172
C173
C140
C141
C358
4.7uF
0.1uF
VCC3.3DDEC
C143
C138
C142
C231
C230
ALT_3.3V
L28
VCC3.3_AN_DDEC
BLM41P750SPT
C171
C174
C170
C361
4.7uF
C177
C178
C179
C176
C175
.047uF
GND
VCC5
Video Input Section (Channel 1)
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Title
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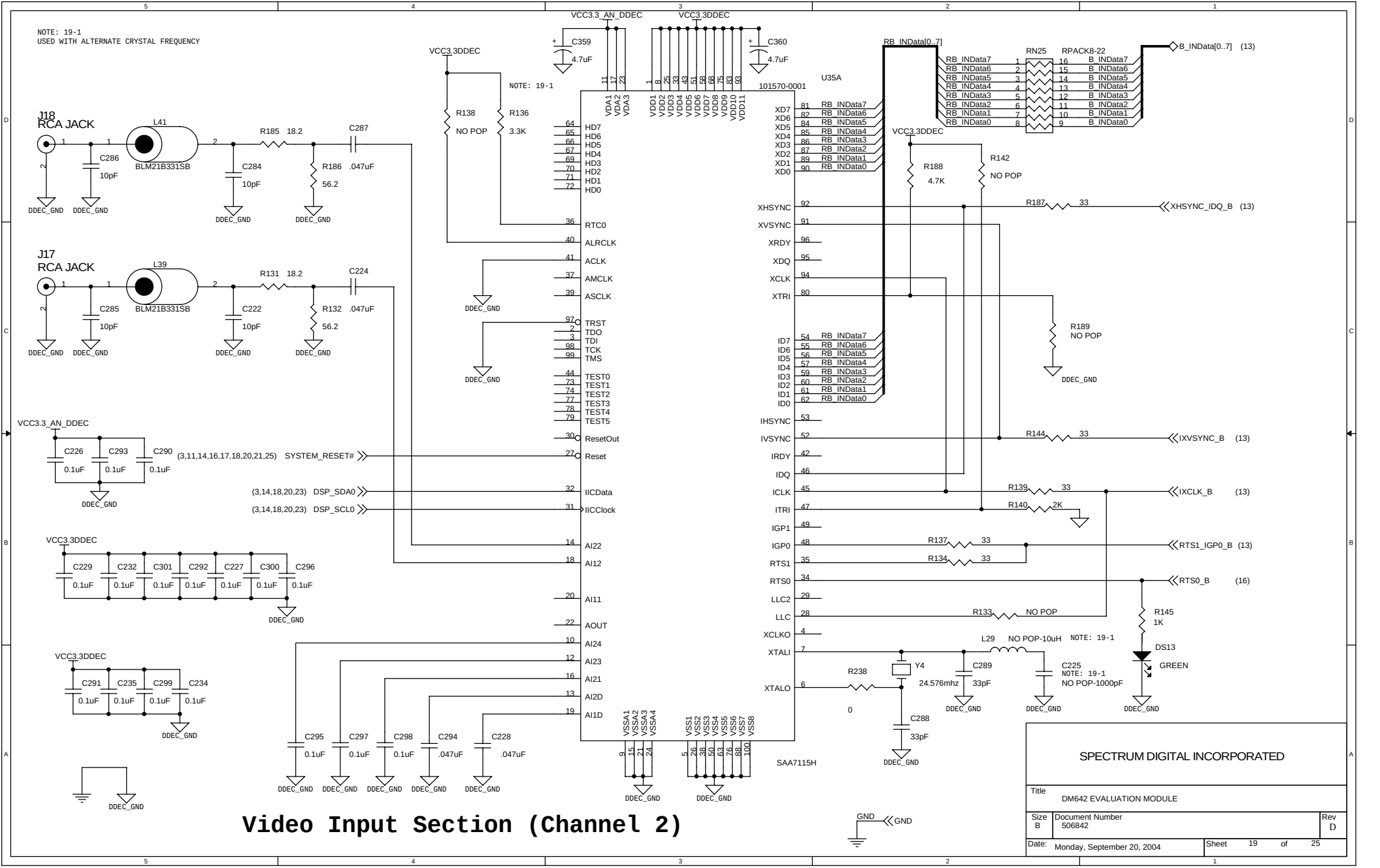
NOTE: 19-1
USED WITH ALTERNATE CRYSTAL FREQUENCY
J18
RCA JACK
J17
RCA JACK
L41
L39
BLM21B331SB
U35A
101570-0001
SAA7115H
SPECTRUM DIGITAL INCORPORATED
DM642 EVALUATION MODULE
Video Input Section (Channel 2)
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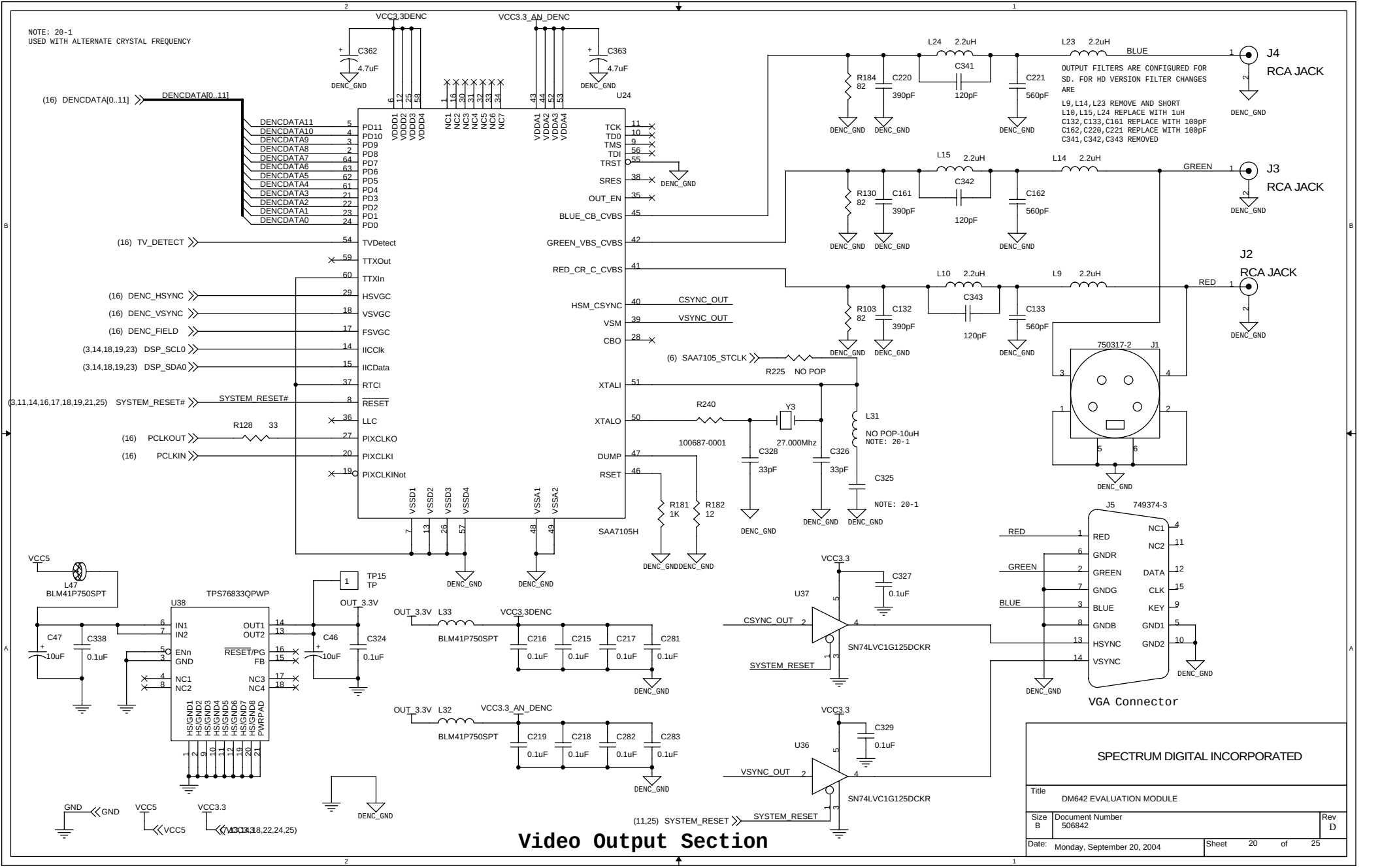
NOTE: 20-1
USED WITH ALTERNATE CRYSTAL FREQUENCY
VCC3.3DENC
VCC3.3_AN_DENC
C362
4.7uF
C363
4.7uF
DENC_GND
U24
(16) DENCDATA[0..11]
DENCDATA[0..11]
DENCDATA11
DENCDATA10
DENCDATA9
DENCDATA8
DENCDATA7
DENCDATA6
DENCDATA5
DENCDATA4
DENCDATA3
DENCDATA2
DENCDATA1
DENCDATA0
PD11
PD10
PD9
PD8
PD7
PD6
PD5
PD4
PD3
PD2
PD1
PD0
VDDD1
VDDD2
VDDD3
VDDD4
NC1
NC2
NC3
NC4
NC5
NC6
NC7
VDDA1
VDDA2
VDDA3
VDDA4
TCK
TDO
TMS
TDI
TRST
SRES
OUT_EN
BLUE_CB_CVBS
GREEN_VBS_CVBS
RED_CR_C_CVBS
HSM_CSYNC
VSM
CBO
XTALI
XTALO
DUMP
RSET
SAA7105H
(16) TV_DETECT
TVDetect
TTXOut
TTXIn
(16) DENC_HSYNC
HSVGC
(16) DENC_VSYNC
VSVGC
(16) DENC_FIELD
FSVGC
(3,14,18,19,23) DSP_SCL0
IICClk
(3,14,18,19,23) DSP_SDA0
IICData
RTCI
(3,11,14,16,17,18,19,21,25) SYSTEM_RESET#
SYSTEM_RESET#
RESET
LLC
R128 33
(16) PCLKOUT
PIXCLKO
(16) PCLKIN
PIXCLKI
PIXCLKINot
CSYNC_OUT
VSYNC_OUT
(6) SAA7105_STCLK
R225 NO POP
R240
Y3
100687-0001
27.000Mhz
C328
33pF
C326
33pF
L31
NO POP-10uH
NOTE: 20-1
C325
NOTE: 20-1
R181
1K
R182
12
VSSD1
VSSD2
VSSD3
VSSD4
VSSA1
VSSA2
L24 2.2uH
L23 2.2uH
BLUE
R184
82
C220
390pF
C341
120pF
C221
560pF
OUTPUT FILTERS ARE CONFIGURED FOR SD. FOR HD VERSION FILTER CHANGES ARE
L9,L14,L23 REMOVE AND SHORT
L10,L15,L24 REPLACE WITH 1uH
C132,C133,C161 REPLACE WITH 100pF
C162,C220,C221 REPLACE WITH 100pF
C341,C342,C343 REMOVED
J4
RCA JACK
L15 2.2uH
L14 2.2uH
GREEN
R130
82
C161
390pF
C342
120pF
C162
560pF
J3
RCA JACK
L10 2.2uH
L9 2.2uH
RED
R103
82
C132
390pF
C343
120pF
C133
560pF
J2
RCA JACK
750317-2
J1
VCC5
L47
BLM41P750SPT
U38
TPS76833QPWP
IN1
IN2
ENn
GND
NC1
NC2
OUT1
OUT2
RESET/PG
FB
NC3
NC4
HS/GND1
HS/GND2
HS/GND3
HS/GND4
HS/GND5
HS/GND6
HS/GND7
HS/GND8
PWRPAD
C47
10uF
C338
0.1uF
C46
10uF
C324
0.1uF
OUT_3.3V
TP15
TP
OUT_3.3V L33
VCC3.3DENC
BLM41P750SPT
C216
C215
C217
C281
0.1uF
OUT_3.3V L32
VCC3.3_AN_DENC
BLM41P750SPT
C219
C218
C282
C283
0.1uF
U37
U36
VCC3.3
C327
C329
0.1uF
CSYNC_OUT
VSYNC_OUT
SYSTEM_RESET
SN74LVC1G125DCKR
(11,25) SYSTEM_RESET
J5
749374-3
RED
GREEN
BLUE
GNDR
GNDG
GNDB
HSYNC
VSYNC
DATA
CLK
KEY
GND1
GND2
NC1
NC2
VGA Connector
GND
VCC5
VCC3.3
(3,11,14,16,17,18,19,21,22,24,25)
Video Output Section
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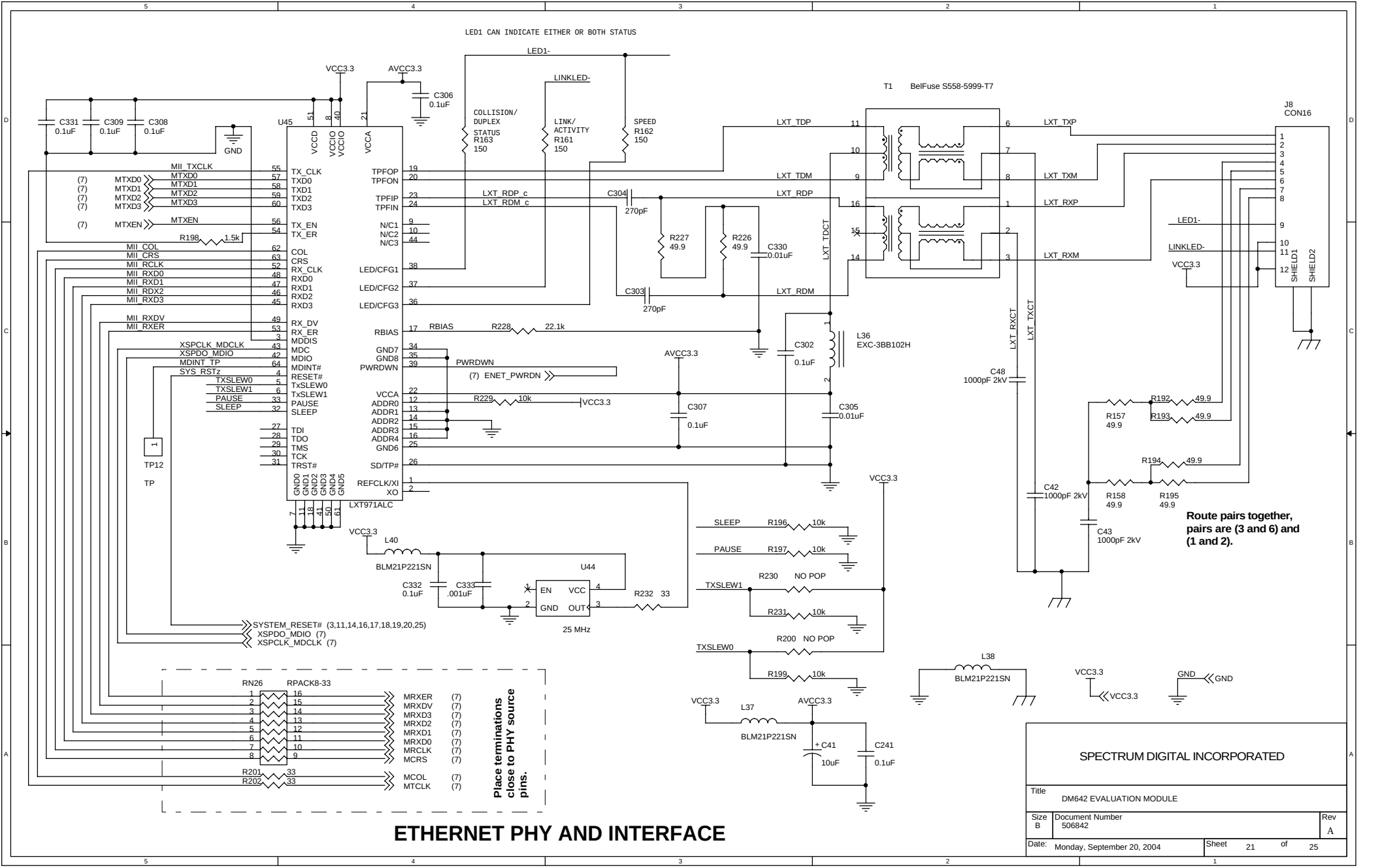

ETHERNET PHY AND INTERFACE

SPECTRUM DIGITAL INCORPORATED

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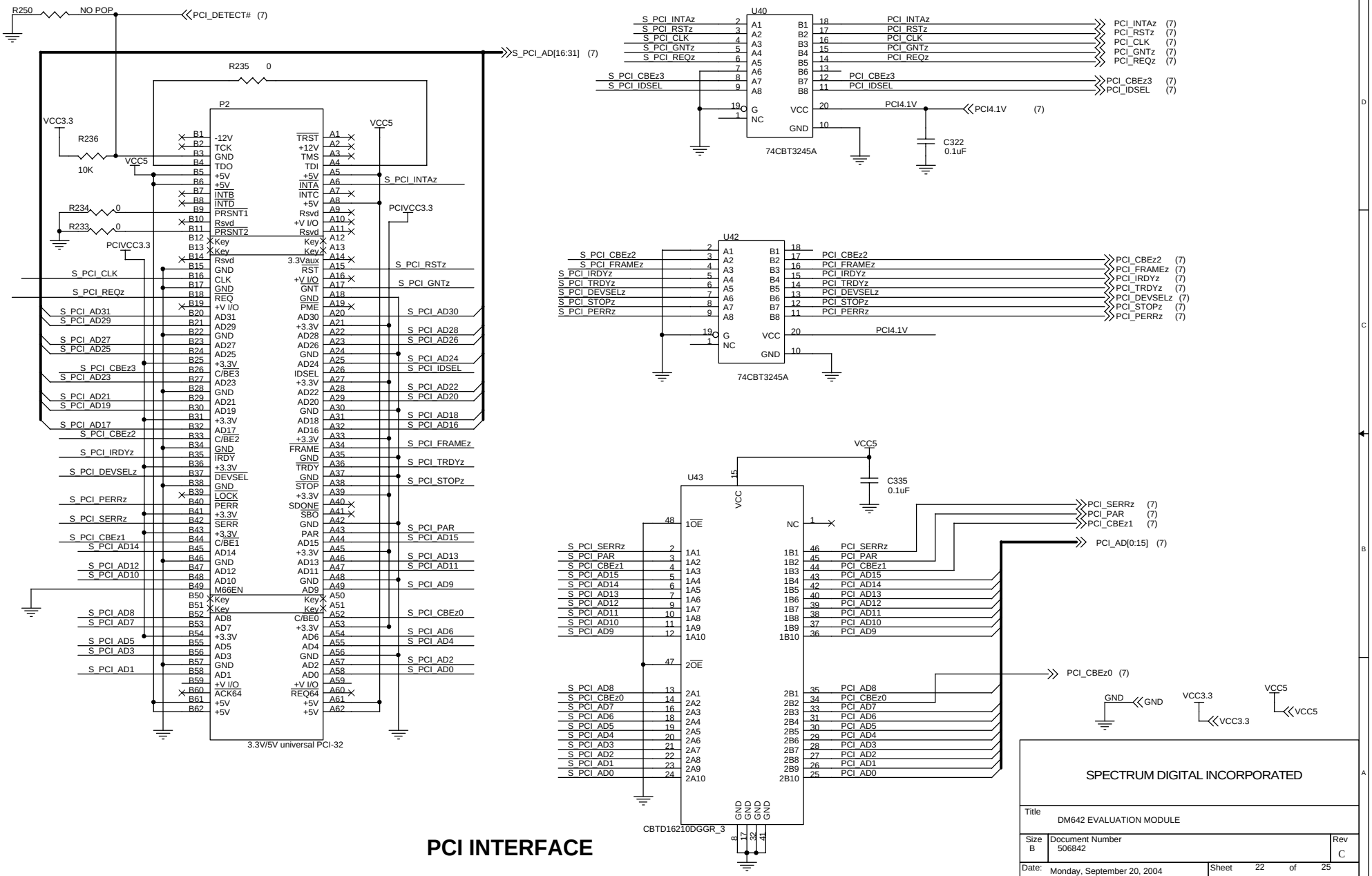
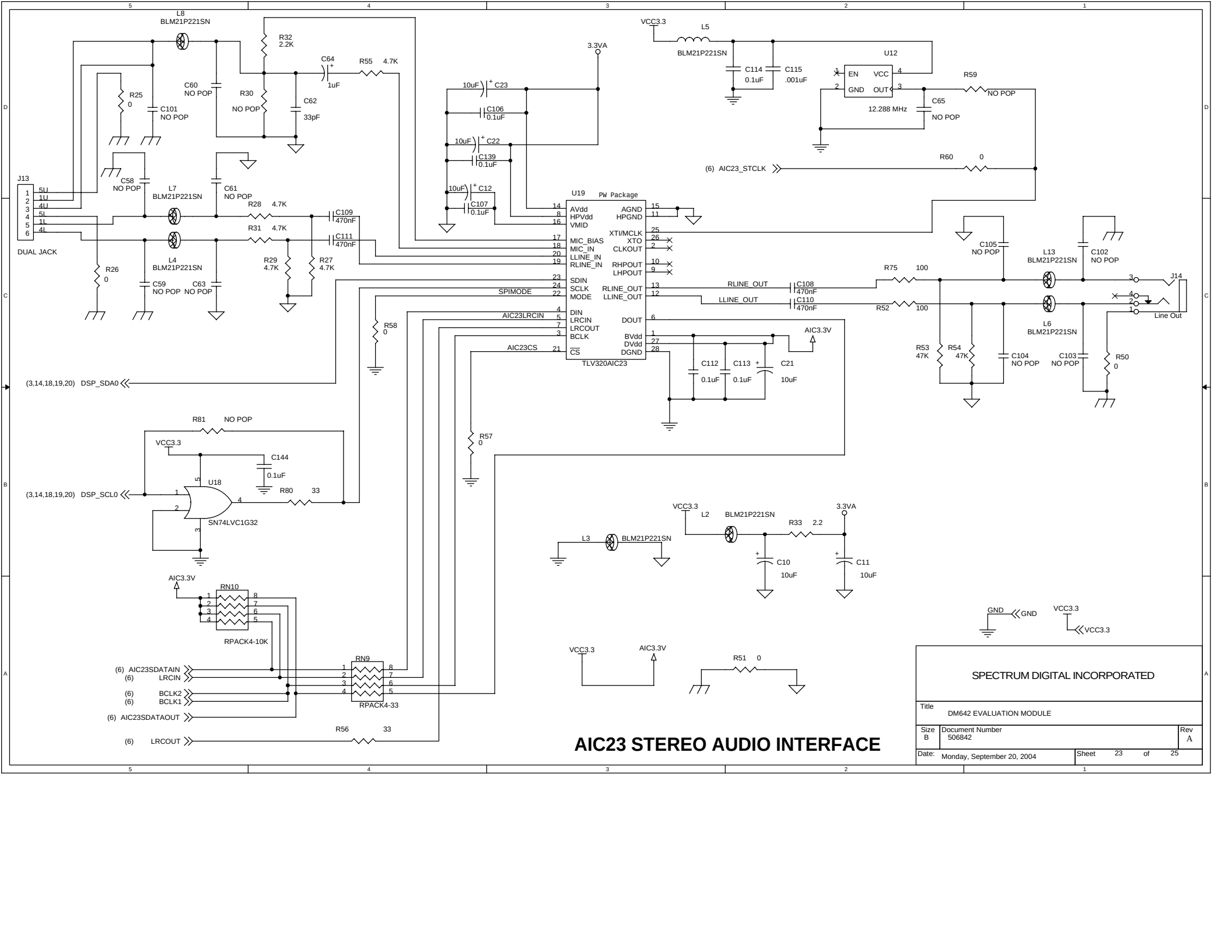


PCI INTERFACE



AIC23 STEREO AUDIO INTERFACE

SPECTRUM DIGITAL INCORPORATED

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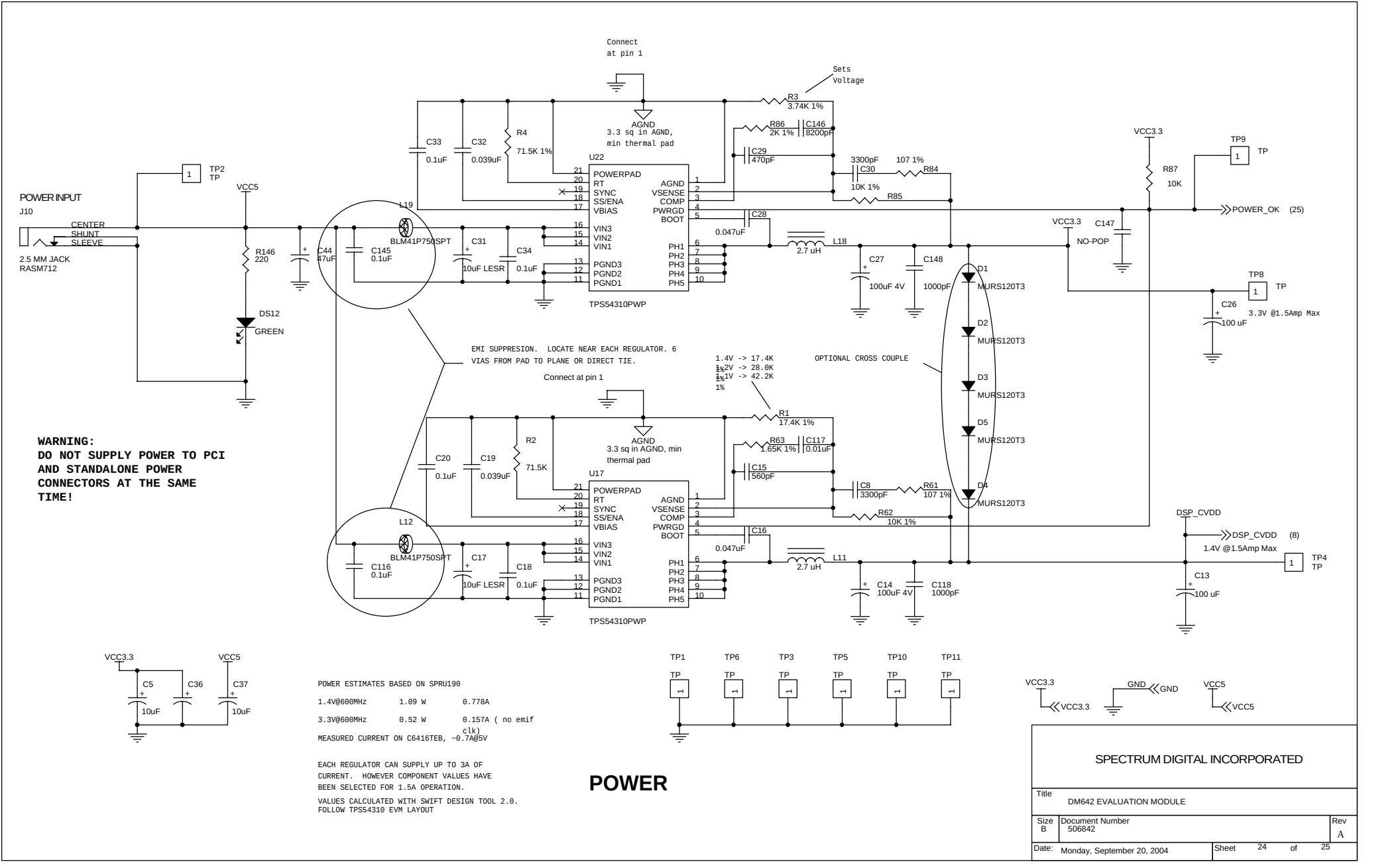
POWER INPUT
J10
CENTER
SHUNT
SLEEVE
2.5 MM JACK
RASM712
TP2
TP
VCC5
R146
220
DS12
GREEN
C44
47uF
C145
0.1uF
L19
BLM41P750SPT
C31
10uF LESR
C34
0.1uF
Connect
at pin 1
AGND
3.3 sq in AGND,
min thermal pad
Sets
Voltage
R3
3.74K 1%
R86
2K 1%
C146
8200pF
C33
0.1uF
C32
0.039uF
R4
71.5K 1%
C29
470pF
3300pF
C30
10K 1%
107 1%
R84
R85
U22
POWERPAD
RT
SYNC
SS/ENA
VBIAS
VIN3
VIN2
VIN1
PGND3
PGND2
PGND1
AGND
VSENSE
COMP
PWRGD
BOOT
PH1
PH2
PH3
PH4
PH5
TPS54310PWP
C28
0.047uF
L18
2.7 uH
C27
100uF 4V
C148
1000pF
VCC3.3
C147
NO-POP
R87
10K
TP9
TP
POWER_OK
(25)
TP8
TP
C26
100 uF
3.3V @1.5Amp Max
D1
MURS120T3
D2
MURS120T3
D3
MURS120T3
D5
MURS120T3
D4
MURS120T3
OPTIONAL CROSS COUPLE
EMI SUPPRESION. LOCATE NEAR EACH REGULATOR. 6
VIAS FROM PAD TO PLANE OR DIRECT TIE.
Connect at pin 1
1.4V -> 17.4K
3.2V -> 28.0K
3.1V -> 42.2K
1%
R1
17.4K 1%
R63
1.65K 1%
C117
0.01uF
C20
0.1uF
C19
0.039uF
R2
71.5K
C15
560pF
C8
3300pF
R61
107 1%
R62
10K 1%
U17
C16
0.047uF
L12
BLM41P750SPT
C17
10uF LESR
C18
0.1uF
C116
0.1uF
L11
2.7 uH
C14
100uF 4V
C118
1000pF
DSP_CVDD
DSP_CVDD
(8)
1.4V @1.5Amp Max
TP4
TP
C13
100 uF
WARNING:
DO NOT SUPPLY POWER TO PCI
AND STANDALONE POWER
CONNECTORS AT THE SAME
TIME!
VCC3.3
VCC5
C5
10uF
C36
C37
10uF
POWER ESTIMATES BASED ON SPRU190
1.4V@600MHz 1.09 W 0.778A
3.3V@600MHz 0.52 W 0.157A (no emif clk)
MEASURED CURRENT ON C6416TEB, ~0.7A@5V
EACH REGULATOR CAN SUPPLY UP TO 3A OF
CURRENT. HOWEVER COMPONENT VALUES HAVE
BEEN SELECTED FOR 1.5A OPERATION.
VALUES CALCULATED WITH SWIFT DESIGN TOOL 2.0.
FOLLOW TPS54310 EVM LAYOUT
TP1
TP6
TP3
TP5
TP10
TP11
GND
POWER
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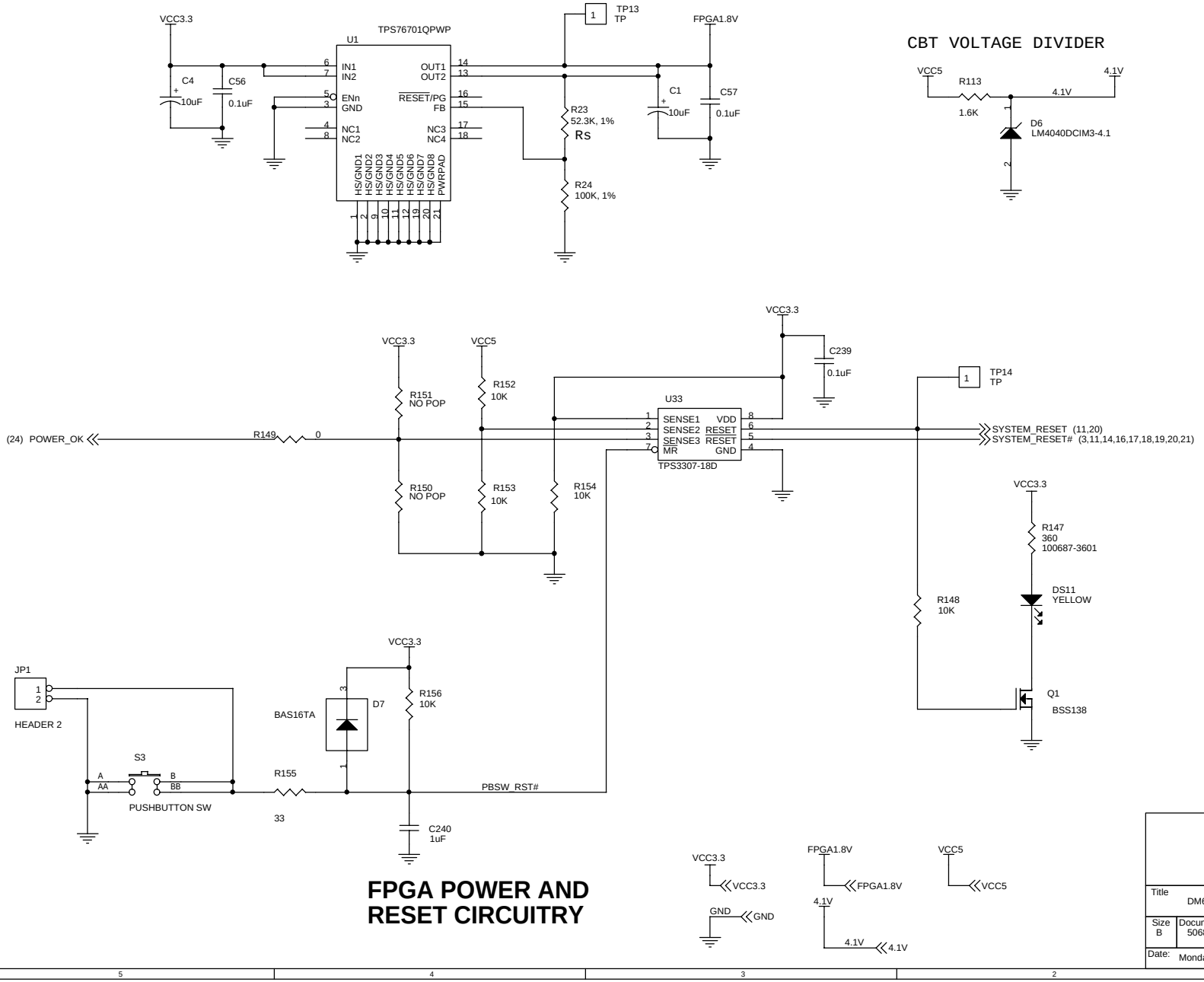

FPGA POWER AND RESET CIRCUITRY

SPECTRUM DIGITAL INCORPORATED

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