

NOTES, UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES IN OHMS.
2. CAPACITANCE VALUES IN MICROFARADS.
3. REFERENCE DESIGNATORS USED:

4. ALL 0.1 uF AND 0.01uF CAPACITORS ARE DECOUPLING CAPS UNLESS OTHERWISE NOTED. THEY ARE SHOWN ON THE PAGE WITH THE INTEGRATED CIRCUITS THEY SHOULD BE PLACED NEAR.

5. OBSERVE THE FOLLOWING LAYOUT NOTES:

6. BOARD PROPERTIES

- A. ROUTE TO WITHIN 10% OF MANHATTAN DISTANCE
- B. 50 +/- 5 OHM MATCHED IMPEDANCE
- C. OUTER LAYERS 0.5 OZ CU /W 0.5 OZ AU PLATING
- D. INNER LAYERS 1.0 OZ CU
- E. FR4 BOARD MATERIAL
- F. MINIMUM TRACE WIDTH/SPACING 4 MILS
- G. MINIMUM VIA SIZE 10/19 MIL
- H. LAYER STACKUP:

1. TOP - SIGNAL ROUTING
2. GROUND PLANE
3. INNER1 - SIGNAL ROUTING
4. VCC3 PLANE (3.3V BOARD)
5. INNER2 - SIGNAL ROUTING
6. INNER3 - SIGNAL ROUTING
7. VCC PLANE 2
8. INNER4 - SIGNAL ROUTING
9. GROUND PLANE
10. BOTTOM - SIGNAL ROUTING

SCHMATIC INDEX

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- 2 User Options/Config
- 3 DM642 Clocks, Reset, Interrupts, Timers, and IIC
- 4 DM642 EMIF
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- 21 Ethernet
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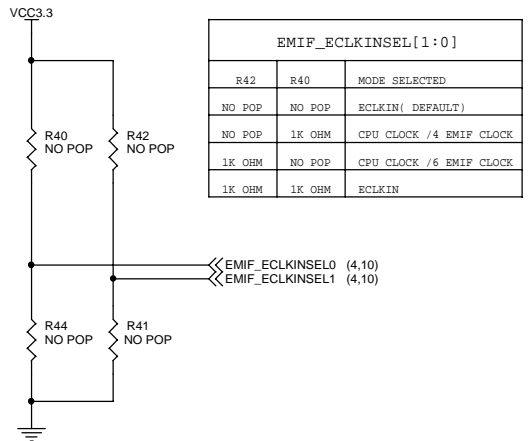
REV	DESCRIPTION	DATE	APPROVED
A	Initial schematic ready for layout.	01/07/03	RRP
B	Sheet 2: Changed LENDIAN_MODE signal so R221 is a pull-up and S2 provides a pull-down. Sheet 3: Swapped DSP_SCL0 and DSP_SDA0 signals going to U16. Sheet 7: Added series terminations RN28, R246, R247, & R248. Sheet 11: Routed DC_A[8:6], UART_CSA#, & UART_CSB# to U15. Sheet 13: Changed bus routed to U53 to VP0D[9:2] and U52 to VP1D[9:2]. Sheet 15: Added pull-up (R241) to DC_ARDY. Sheet 17: Pin 177 is Ground not VCC Sheet 20: Changed U36 & U37 to SN74LVC1G125DCKR.	04/01/03	RRP
C	Sheet 2: Changed EMAC_ENABLE to autodect S2 is now 2 position switch. Sheet 3: Routed FPGALOCK to pullup R101 to lock FPGA programming Sheet 7: Implemented EMAC_ENABLE Autodetect on U41-1A, added R249 Sheet 11: Added TCE2#, TCE3#, SOE3# to U15 Decoder. Sheet 16: Swapped pins 141 and 149 on FPGA for HDTV speed paths, changed fpga to -7 part Sheet 17: Added AND Gate U55 to Lock FPGA programming, changed FPGA to -7 Sheet 20: Swapped Red and Blue on VGA Connector. Removed R102,R129,R183 Sheet 22: Added R250 for HPI option	05/15/03	RRP
D	Sheet 10: Changed Buffers U2,U3,U4,U5 to non-holder type SN74LVT16245B Sheet 18: Changed crystal capacitors C168 and C169 from 18pF to 33 pF Sheet 19: Changed crystal capacitors C288 and C289 from 18pF to 33 pF Sheet 20: Changed Value on output termination R82,R130,R184 from 75 ohms to 82 ohms.	08/01/03	RRP
D	Sheet 03: Changed Oscillator U26 to 60MHz. For -0003 version of 506840	08/01/04	RRP

REVISION STATUS OF SHEETS

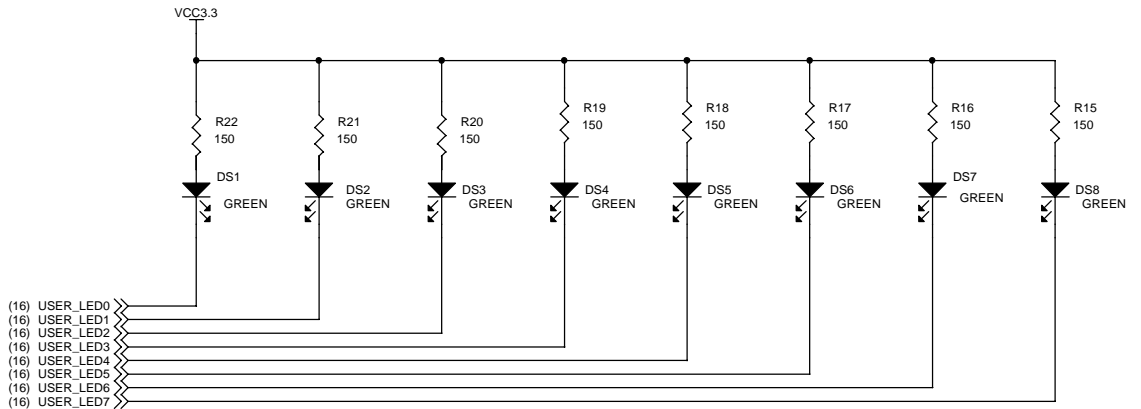
REV	A	C	A	A	B												
SH	21	22	23	24	25												
REV	C	A	B	A	B	C	C	D	D	D							
SH	11	12	13	14	15	16	17	18	19	20							
REV	D	C	D	A	A	A	C	B	A	D	NEXT ASSY	USED ON					
SH	1	2	3	4	5	6	7	8	9	10	APPLICATION						

DWN	DATE
R.R.P.	03/30/2003
CHK	DATE
T.W.K.	03/30/2003
ENGR	DATE
R.R.P.	03/30/2003
ENGR-MGR	DATE
R.R.P.	03/30/2003
QA	DATE
C.M.D.	03/30/2003
HFG	DATE
R.R.P.	03/30/2003
RLSE	DATE
R.R.P.	03/30/2003

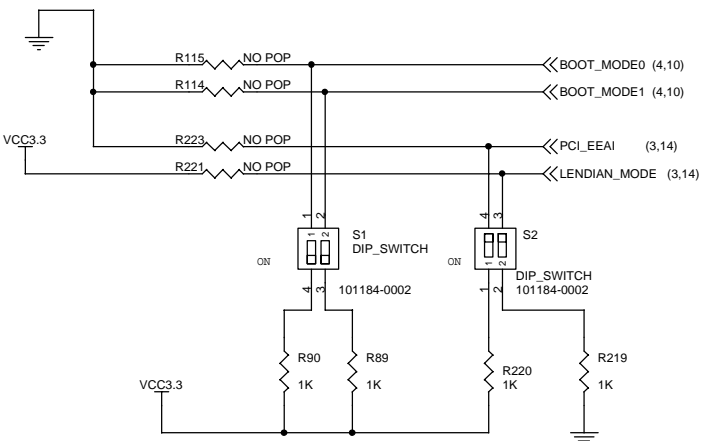
SPECTRUM DIGITAL INCORPORATED			
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EMIF_ECLKINSEL[1:0]		
R42	R40	MODE SELECTED
NO POP	NO POP	ECLKIN( DEFAULT)
NO POP	1K OHM	CPU CLOCK /4 EMIF CLOCK
1K OHM	NO POP	CPU CLOCK /6 EMIF CLOCK
1K OHM	1K OHM	ECLKIN



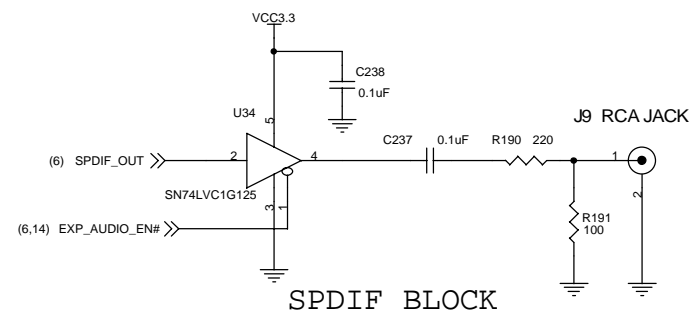
USER LEDS



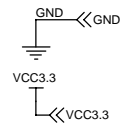
BOOT_MODE[1:0]		
S1-2	S1-1	MODE SELECTED
OFF	OFF	NO BOOT (DEFAULT)
OFF	ON	HPI/PCI BOOT MODE
ON	OFF	RESERVED
ON	ON	EMIF 8 BIT ROM BOOT

PCI MODE CONFIGURATION	
S2-1(PCI ROM)	MODE SELECTED
OFF	PCI EPROM DISABLED(DEFAULT)
ON	PCI ROM ENABLED

ENDIAN MODE CONFIGURATION	
S2-2(ENDIAN)	MODE SELECTED
OFF	LITTLE ENDIAN MODE (DEFAULT)
ON	BIG ENDIAN MODE

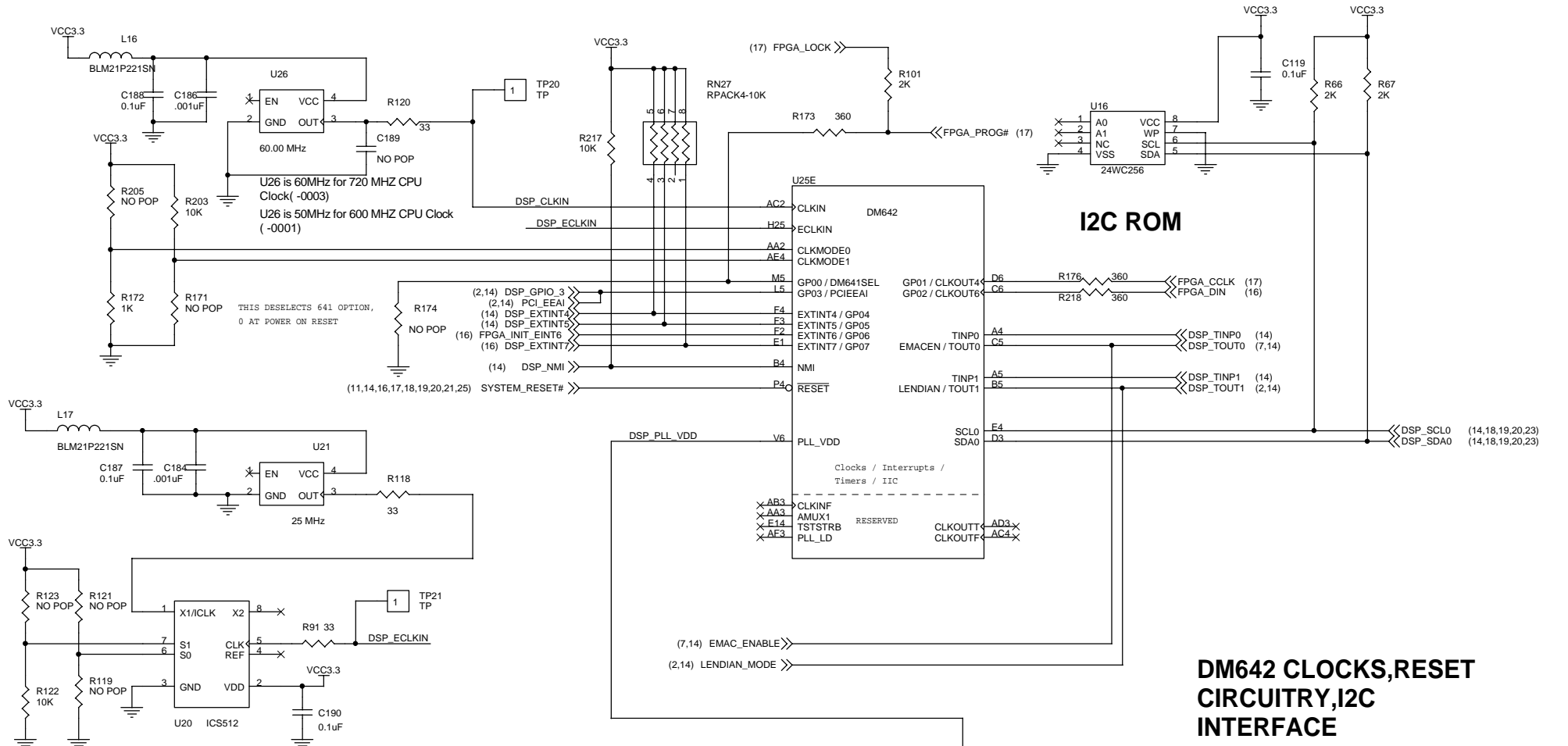


SPDIF BLOCK



**LEDS/SWITCHES/CONFIGURATION INPUTS**

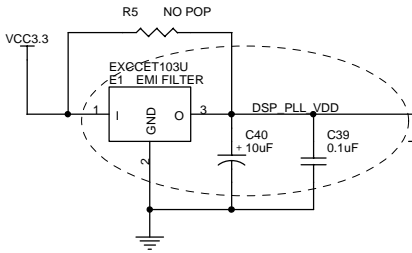
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### I2C ROM

### DM642 CLOCKS, RESET CIRCUITRY, I2C INTERFACE

S1	S0	MULTIPLY	OUTPUT
0	0	4X	100 MHz
0	OPEN	5.33X	133.25 MHz
0	1	5X	125 MHz
OPEN	0	2.5X	62.5 MHz
OPEN	OPEN	2X	50 MHz
OPEN	1	3.33X	83.25 MHz
1	0	6X	150 MHz
1	OPEN	3X	75 MHz
1	1	8X	200 MHz



Place all PLL external components as close to the DSP. All PLL external components must be on a single side of the board.

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Title: DM642 EVALUATION MODULE

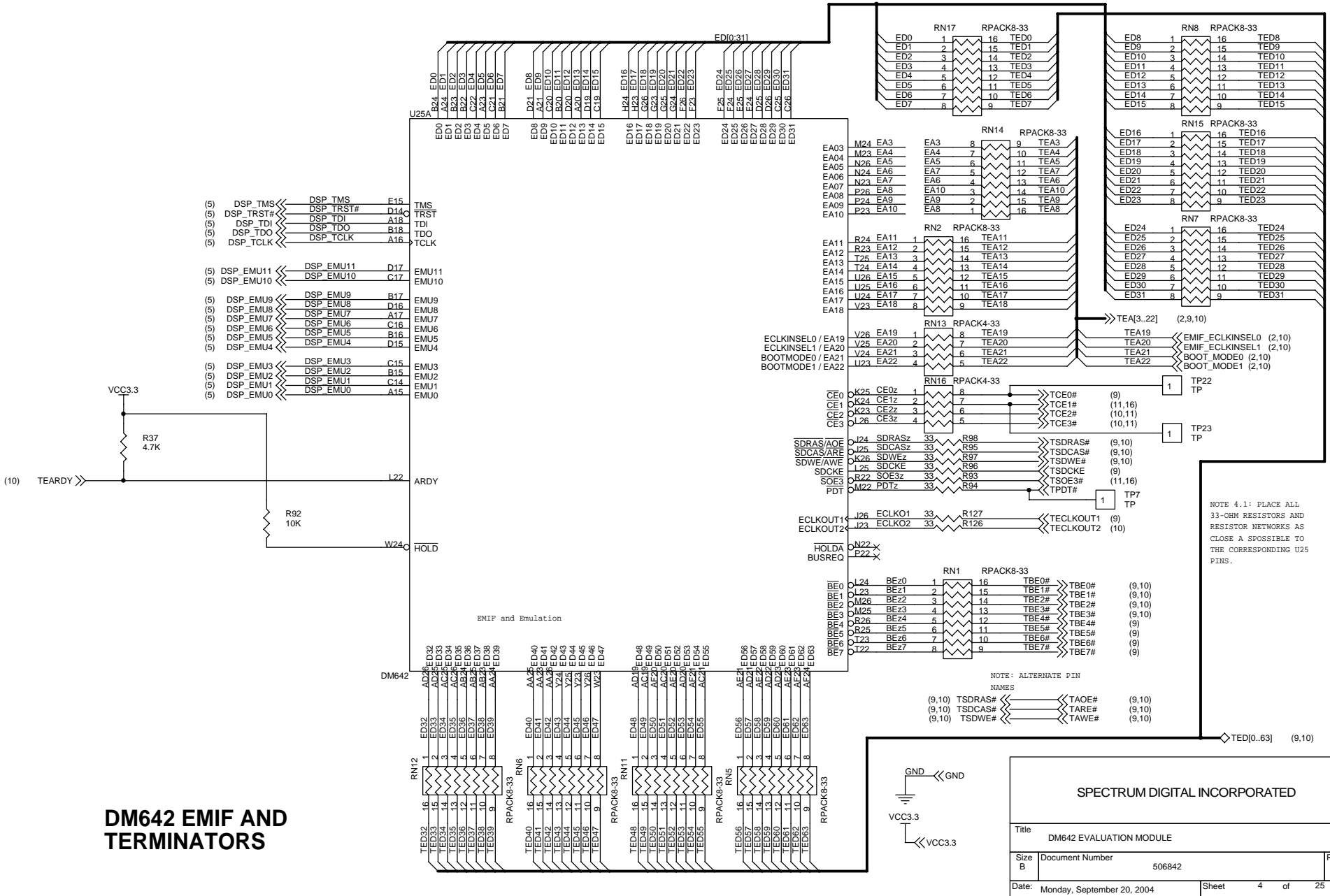
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Size B Document Number: 506842 Rev D

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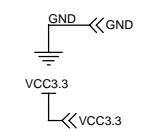
Date: Monday, September 20, 2004 Sheet 3 of 25

# DM642 EMIF AND TERMINATORS



NOTE: ALTERNATE PIN NAMES

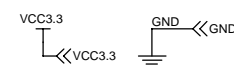
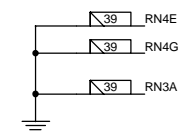
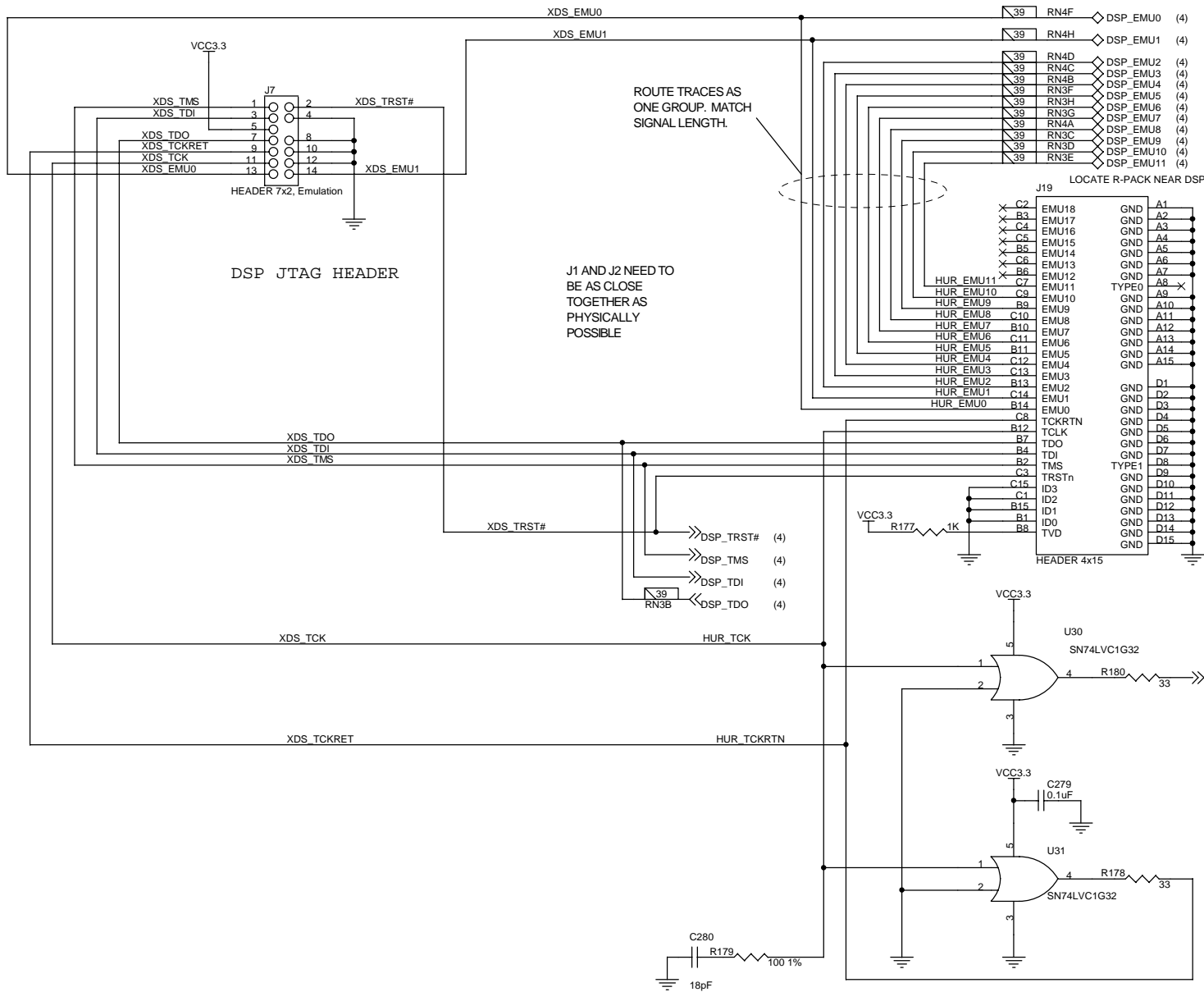
(9,10) TSDRAS#	TAOE#	(9,10)
(9,10) TSDCAS#	TARE#	(9,10)
(9,10) TSDWE#	TAWE#	(9,10)



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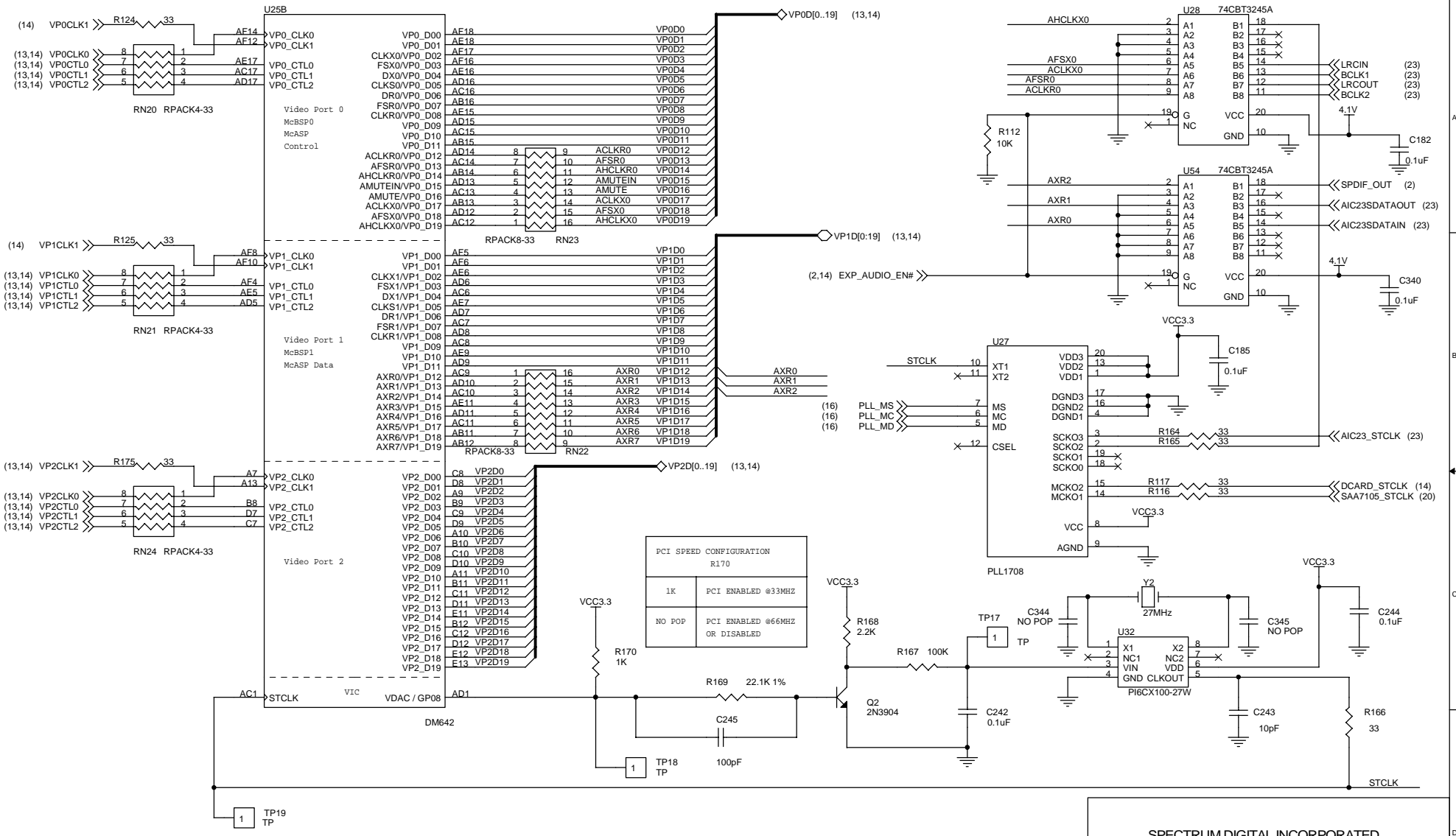
NOTE 4.1: PLACE ALL 33-OHM RESISTORS AND RESISTOR NETWORKS AS CLOSE AS POSSIBLE TO THE CORRESPONDING U25 PINS.

◇ TED[0..63] (9,10)



# EMULATION

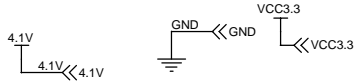
SPECTRUM DIGITAL INCORPORATED		
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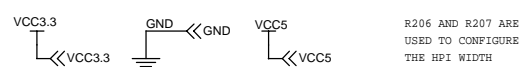
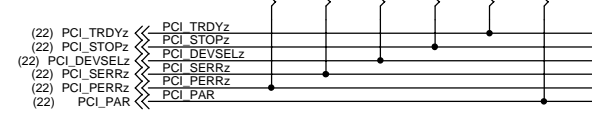
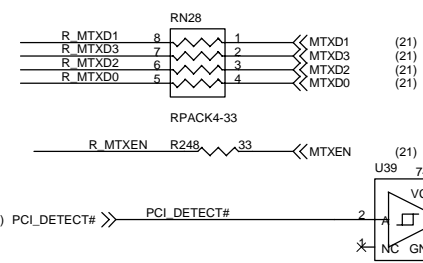
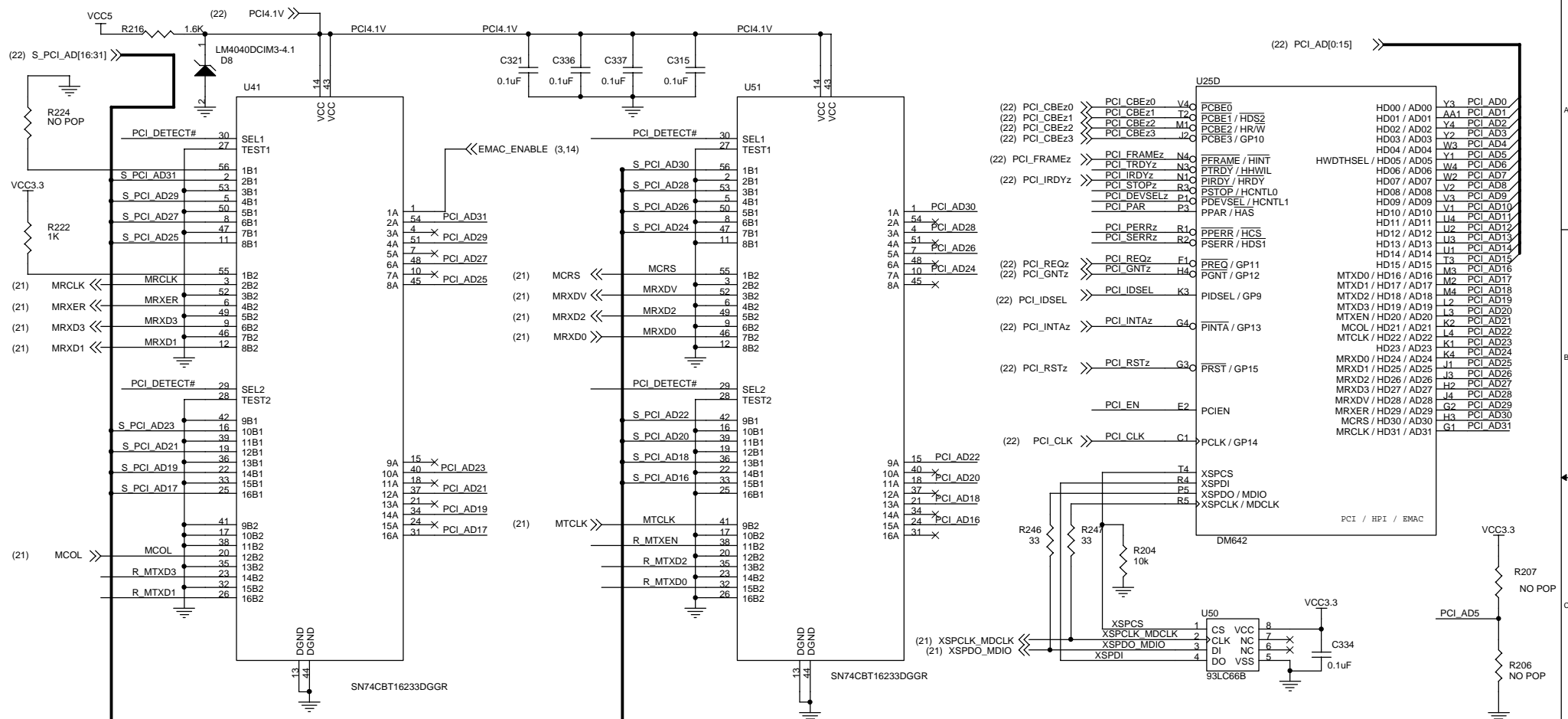


# DM642 VIDEO PORTS

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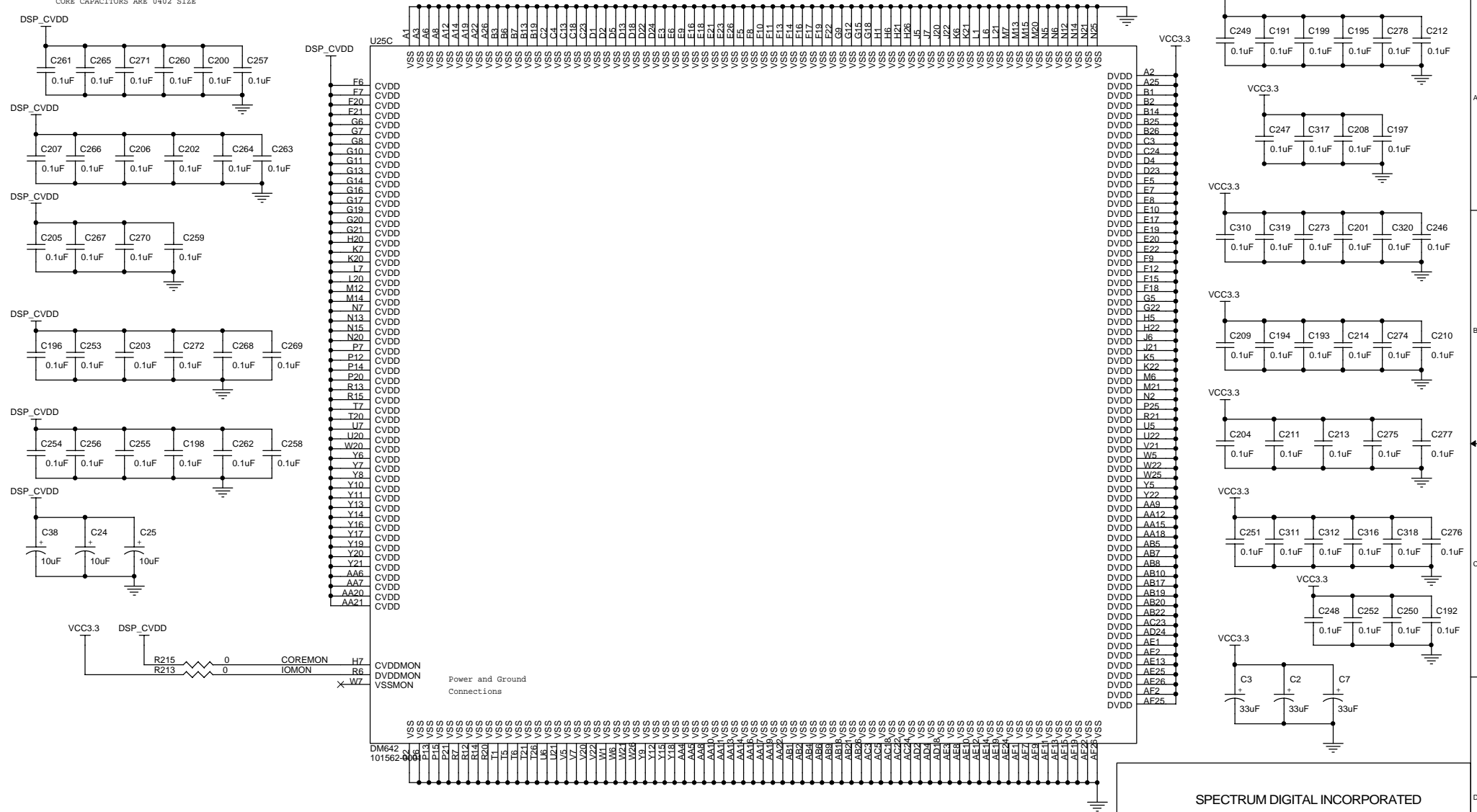




## DM642 PCI/HPI/EMAC INTERFACES

<b>SPECTRUM DIGITAL INCORPORATED</b>			
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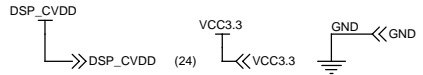
CORE CAPACITORS ARE 0402 SIZE



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# DM642 POWER PINS

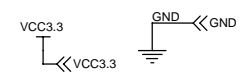
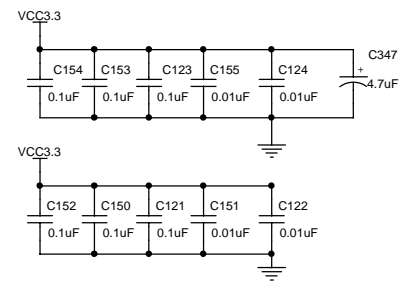
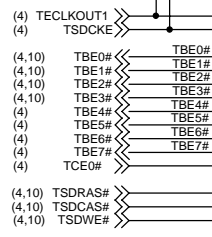
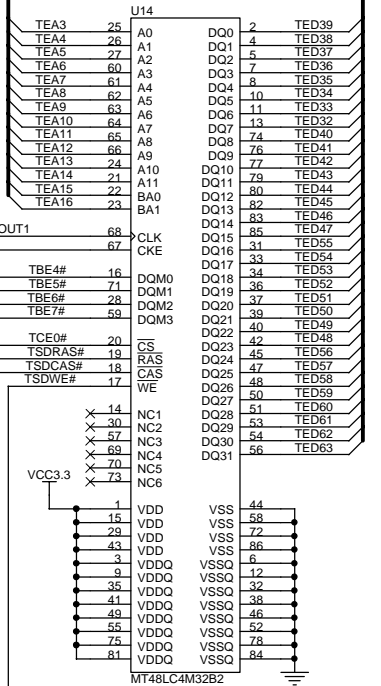
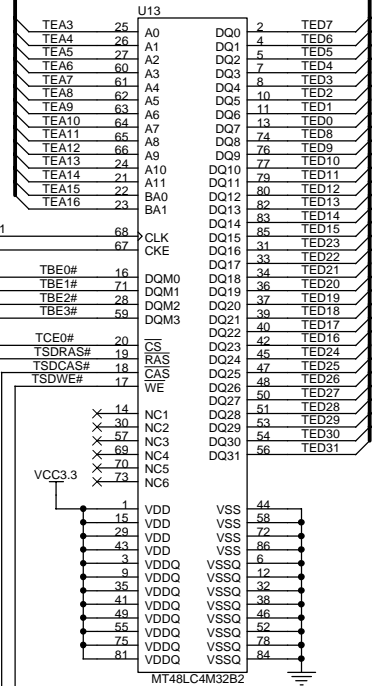




(2,4,10) TEA[3..22] <<

(4,10) TED[0..63] <<

TED[0:63]



# SDRAM MEMORY

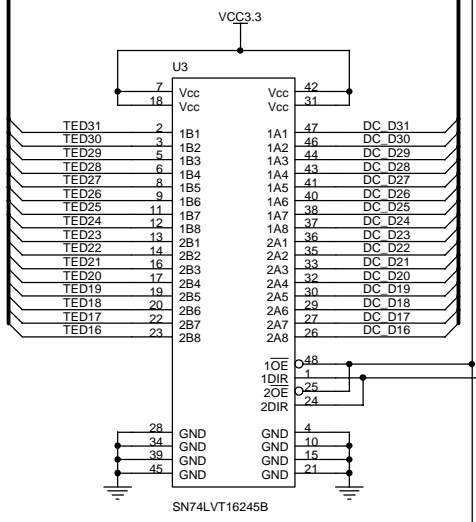
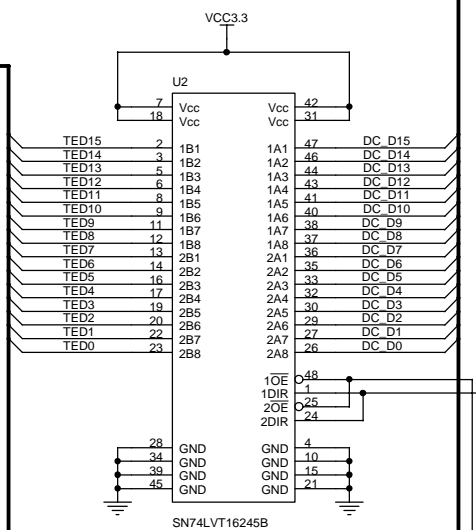
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(2,4,9) TEA[3..22]

(4,9) TED[0..63]

DC\_D[31..0] (11,15,16)  
DC\_A[22..3] (11,15,16)

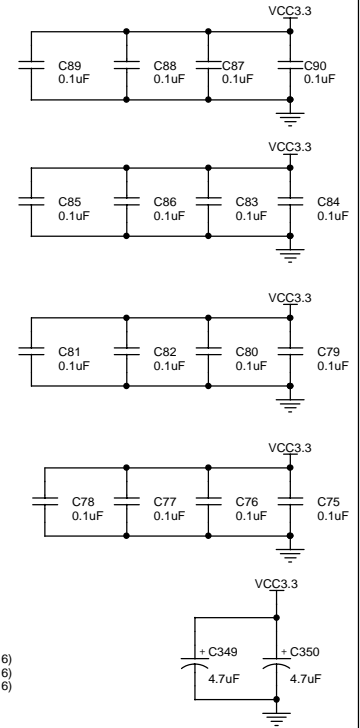
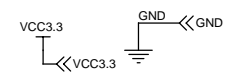
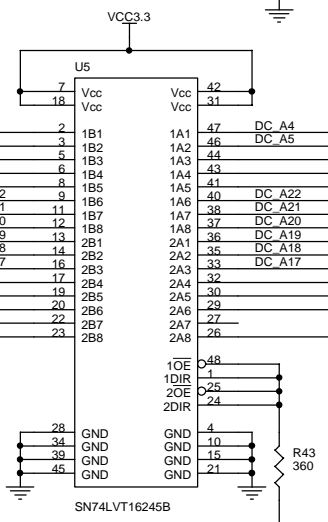
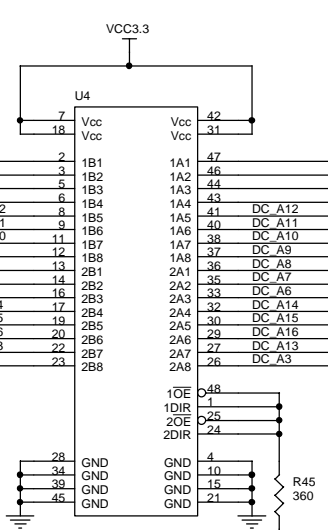


#OE DIR OPERATION  
 L L A<-B  
 L H A->B  
 H X ISOLATION

(4,9) TBE1#  
 (4,9) TBE3#  
 (4,9) TBE0#  
 (4,9) TBE2#

(4,9) TSDWE#  
 (4,9) TSDCAS#  
 (4,9) TSDRAS#

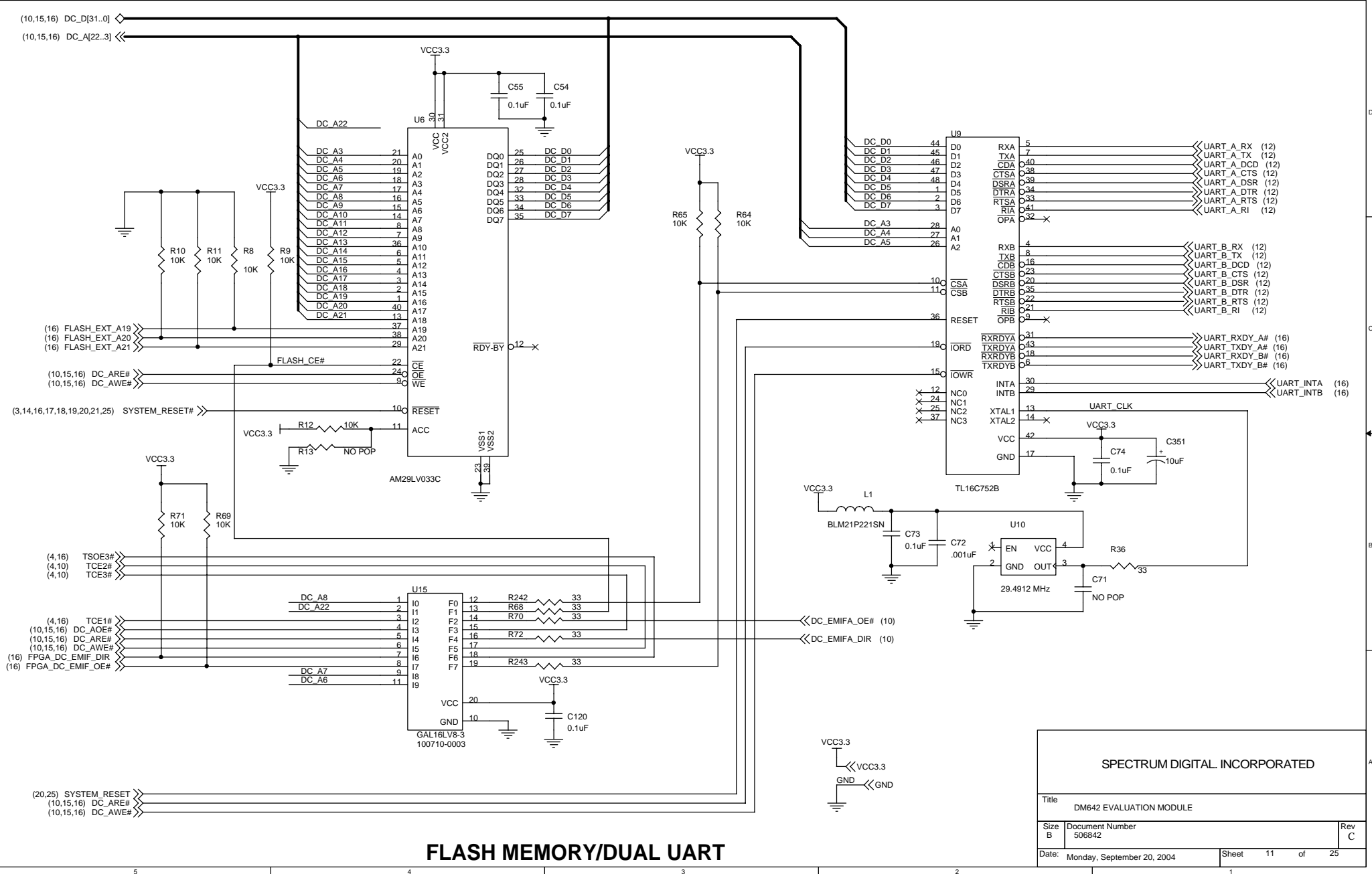
(4,11) TCE3#  
 (4,11) TCE2#  
 (15) DC\_ARDY  
 (4) TECLKOUT2



(11) DC\_EMIFA\_OE#  
 (11) DC\_EMIFA\_DIR

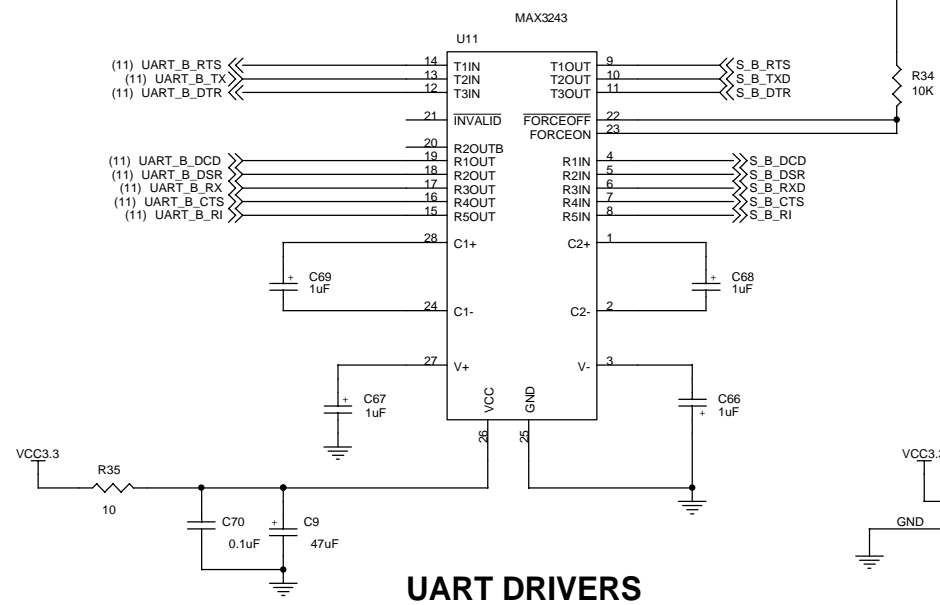
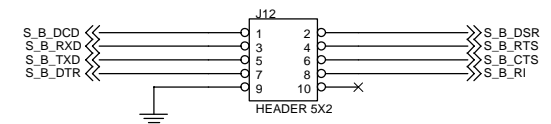
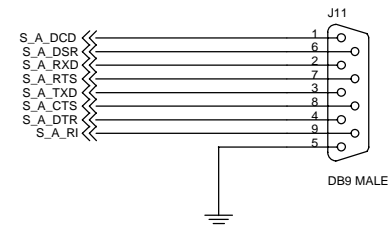
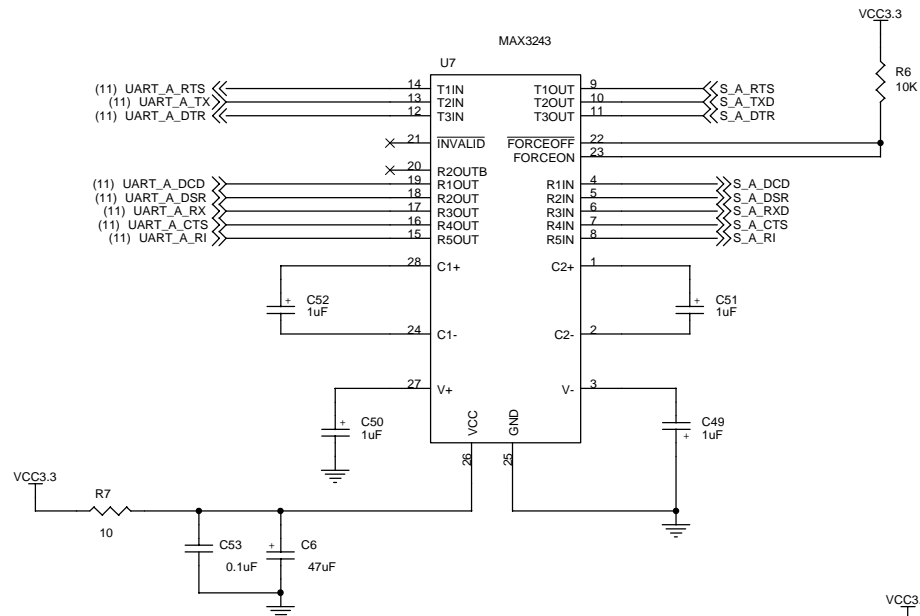
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## DAUGHTER CARD BUFFERING



# FLASH MEMORY/DUAL UART

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UART	NAME	UART IN/OUT
1	CARRIER DETECT	IN
2	RX DATA	IN
3	TX DATA	OUT
4	DTR	OUT
5	GND	GND
6	DSR	IN
7	RTS	OUT
8	CTS	IN
9	RING INDICATOR	IN

### UART DRIVERS

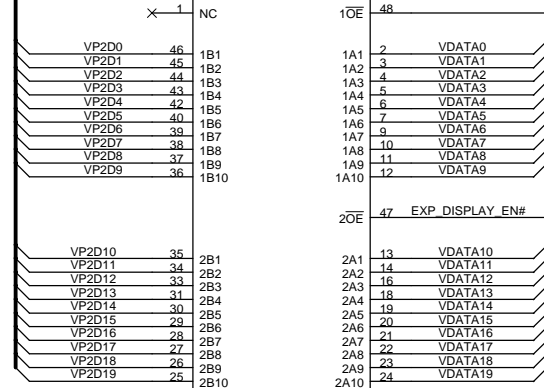
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(6,14) VP2D[0..19]

VP2D[0..19]

U47  
CBTD16210DGGR\_3  
101115-0001



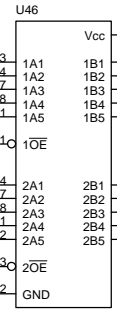
(14) EXP\_DISPLAY\_EN#

VDATA[0..19] << VDATA[0..19] (16)

(14) EXP\_DISPLAY\_EN#

(6,14) VP2CLK1  
(6,14) VP2CTL0  
(6,14) VP2CTL1  
(6,14) VP2CTL2  
(6,14) VP2CLK0

EXP\_DISPLAY\_EN#



SN74CBTS3384

4.1V

C91  
0.1uF

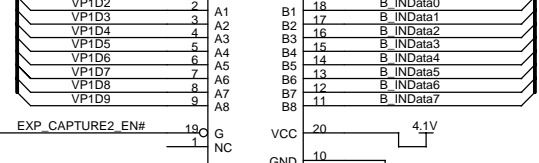
4.1V

C149  
0.1uF

(6,14) VP1D[0..19]

VP1D[0..19]

U52  
74CBT3245A



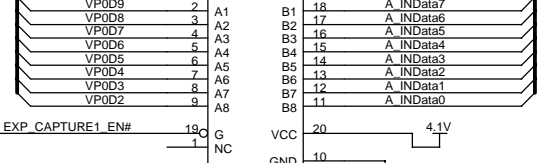
(14) EXP\_CAPTURE2\_EN#

B\_INData[0..7] (19)

(6,14) VP0D[0..19]

VP0D[0..19]

U53  
74CBT3245A



(14) EXP\_CAPTURE1\_EN#

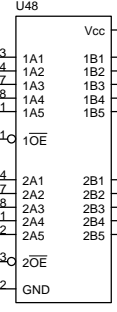
A\_INData[0..7] (19)

(6,14) VP0CTL0  
(6,14) VP0CTL1  
(6,14) VP0CTL2  
(6,14) VP0CLK0

EXP\_CAPTURE1\_EN#

(6,14) VP1CTL0  
(6,14) VP1CTL1  
(6,14) VP1CTL2  
(6,14) VP1CLK0

EXP\_CAPTURE2\_EN#



SN74CBTS3384

4.1V

C149  
0.1uF

R159  
10K

R160  
10K

R88  
360

C339  
0.1uF

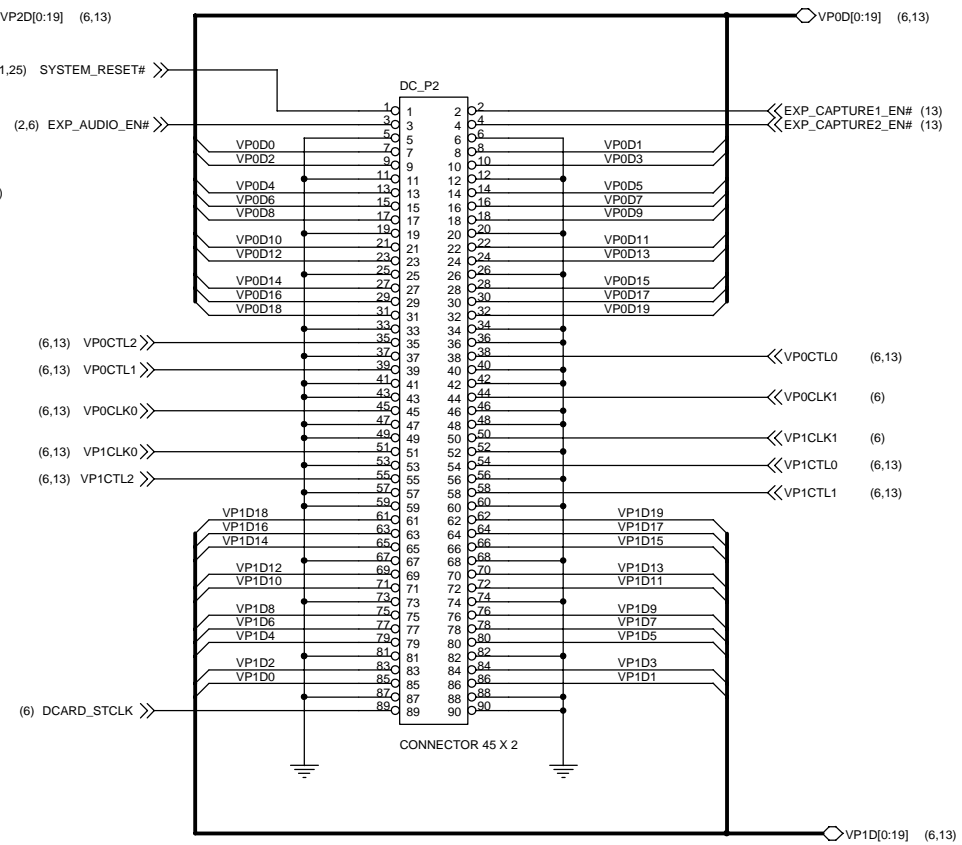
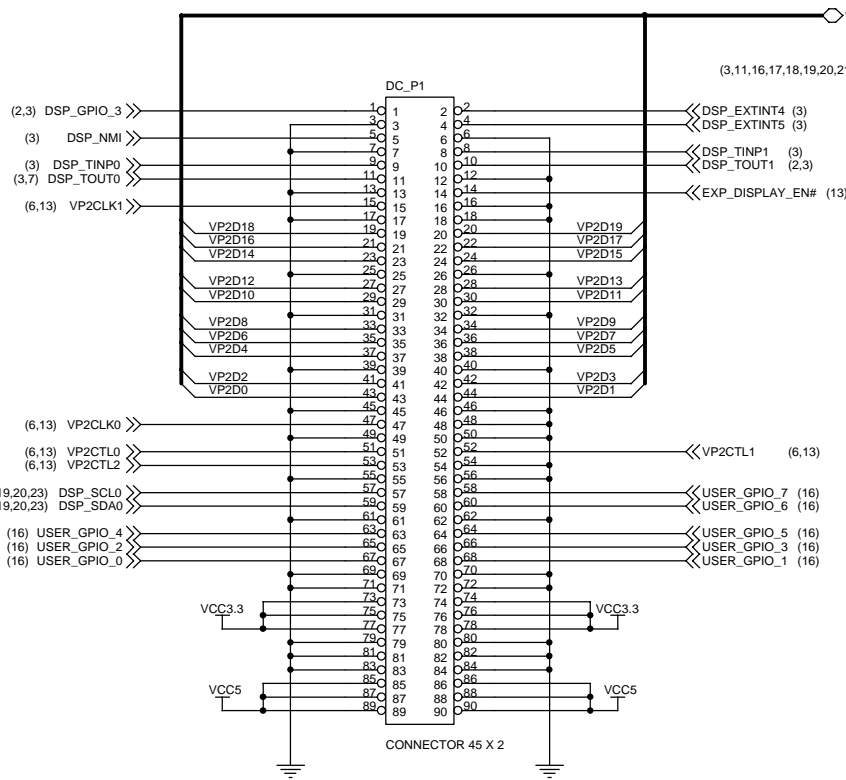
C183  
0.1uF

4.1V  
4.1V << 4.1V  
VCC5 << VCC5  
GND << GND

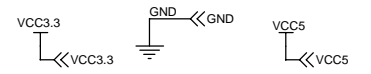
SPECTRUM DIGITAL, INCORPORATED

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### VIDEO PORT SWITCHES



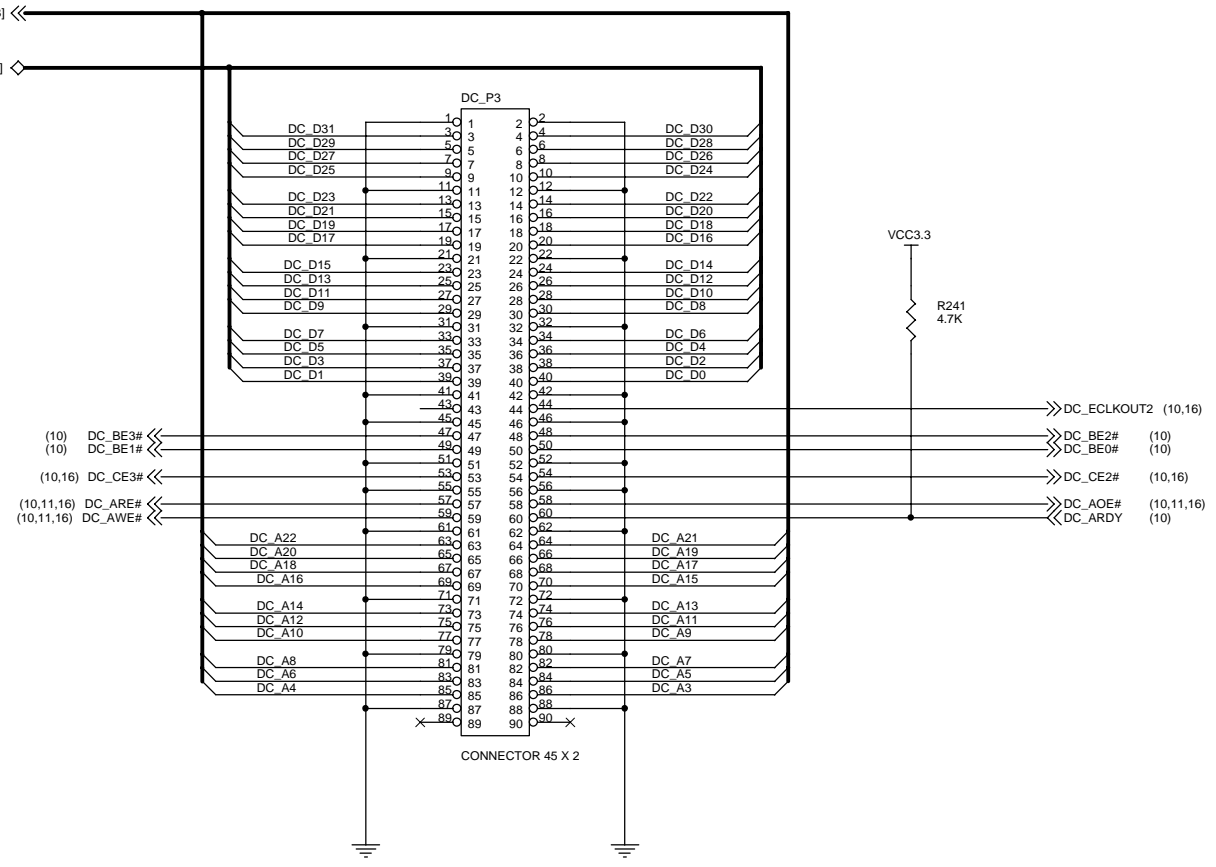
# VIDEO PORTS DAUGHTER CARD CONNECTIONS



SPECTRUM DIGITAL, INCORPORATED		
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(10,11,16) DC\_A[22..3] <<

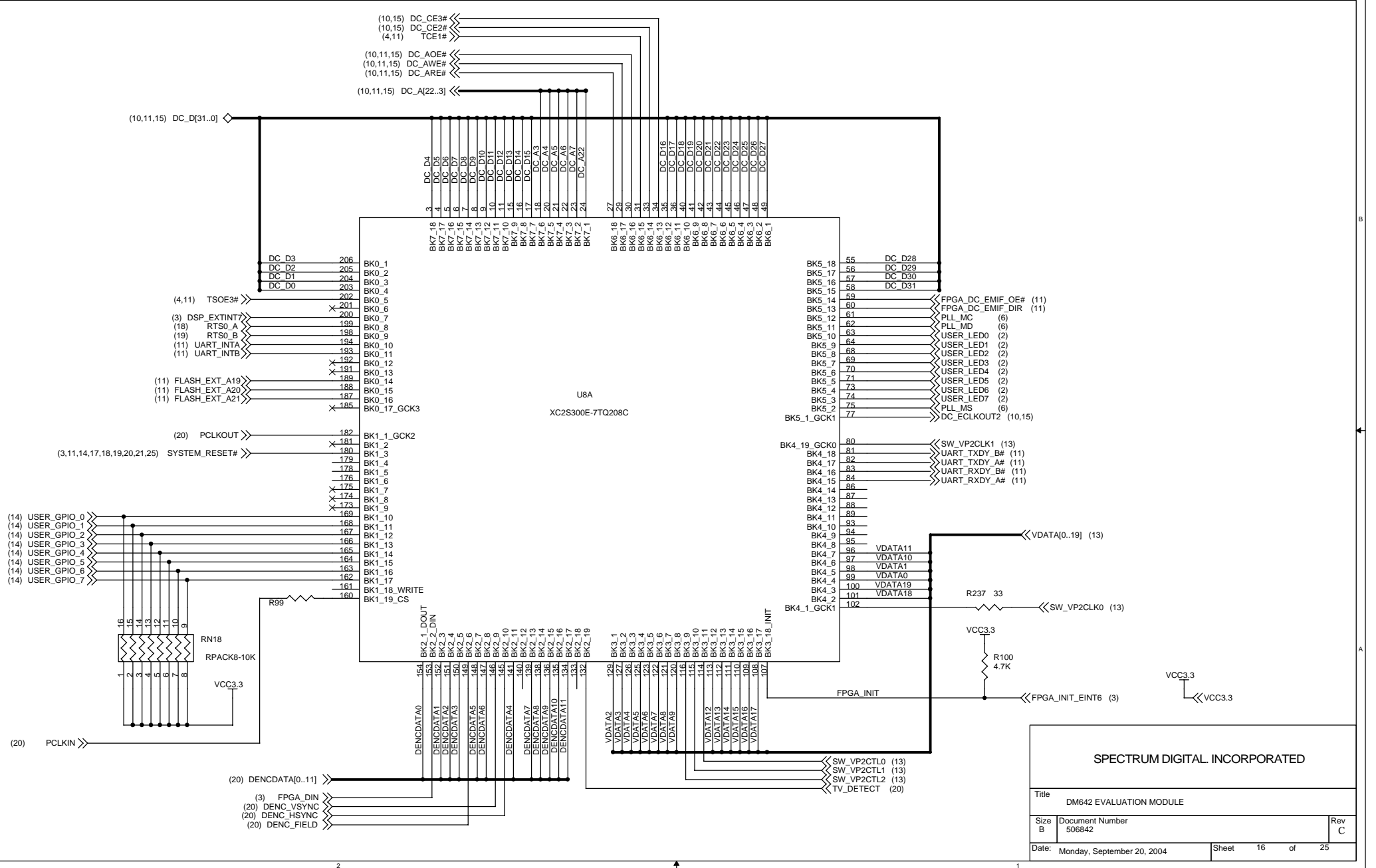
(10,11,16) DC\_D[31..0] <<



## EXTERNAL MEMORY INTERFACE DAUGHTER CARD CONNECTIONS

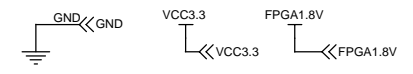
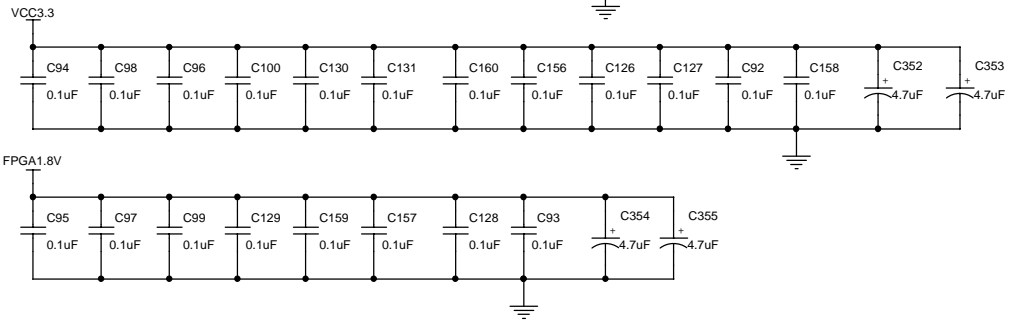
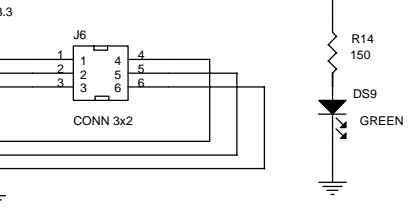
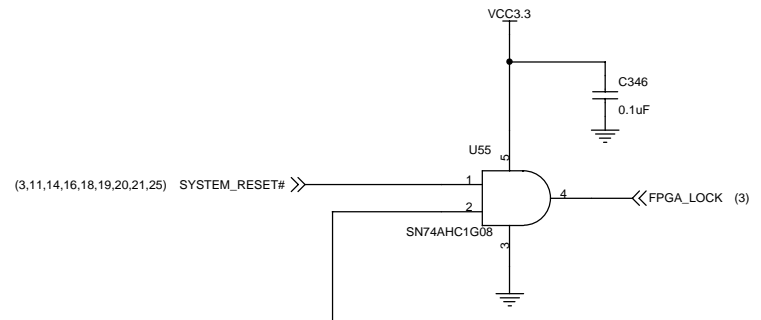
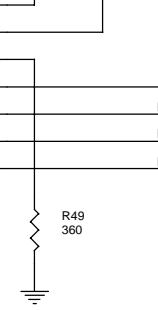
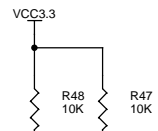
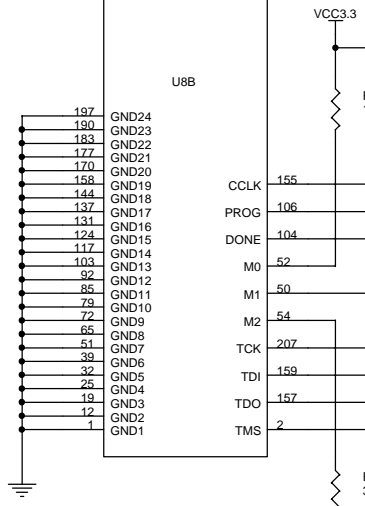
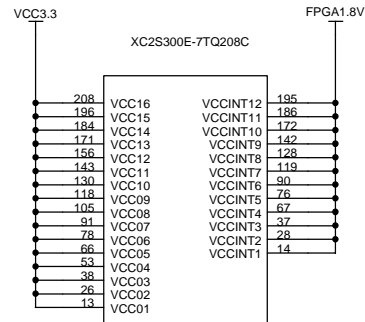


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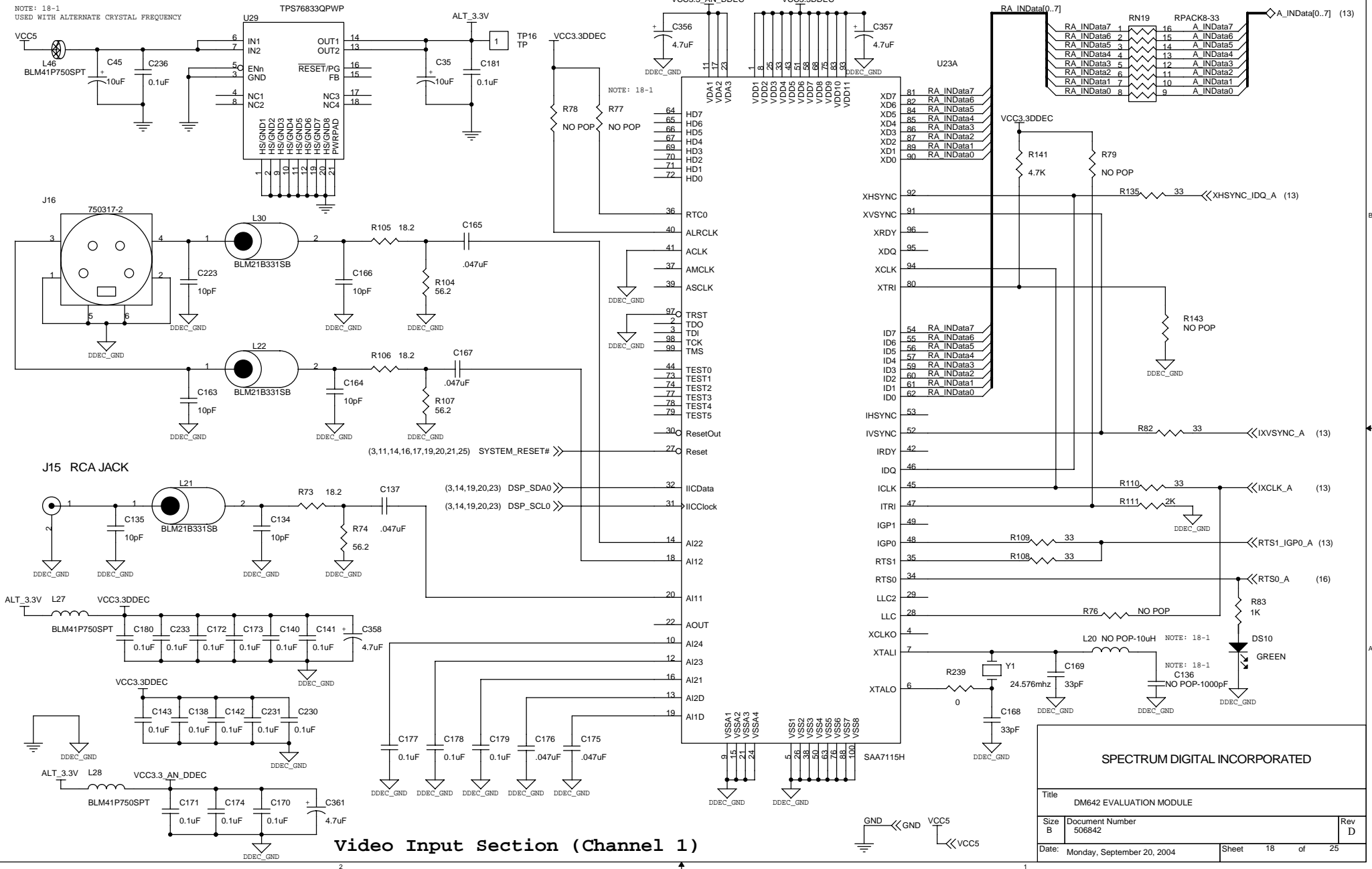
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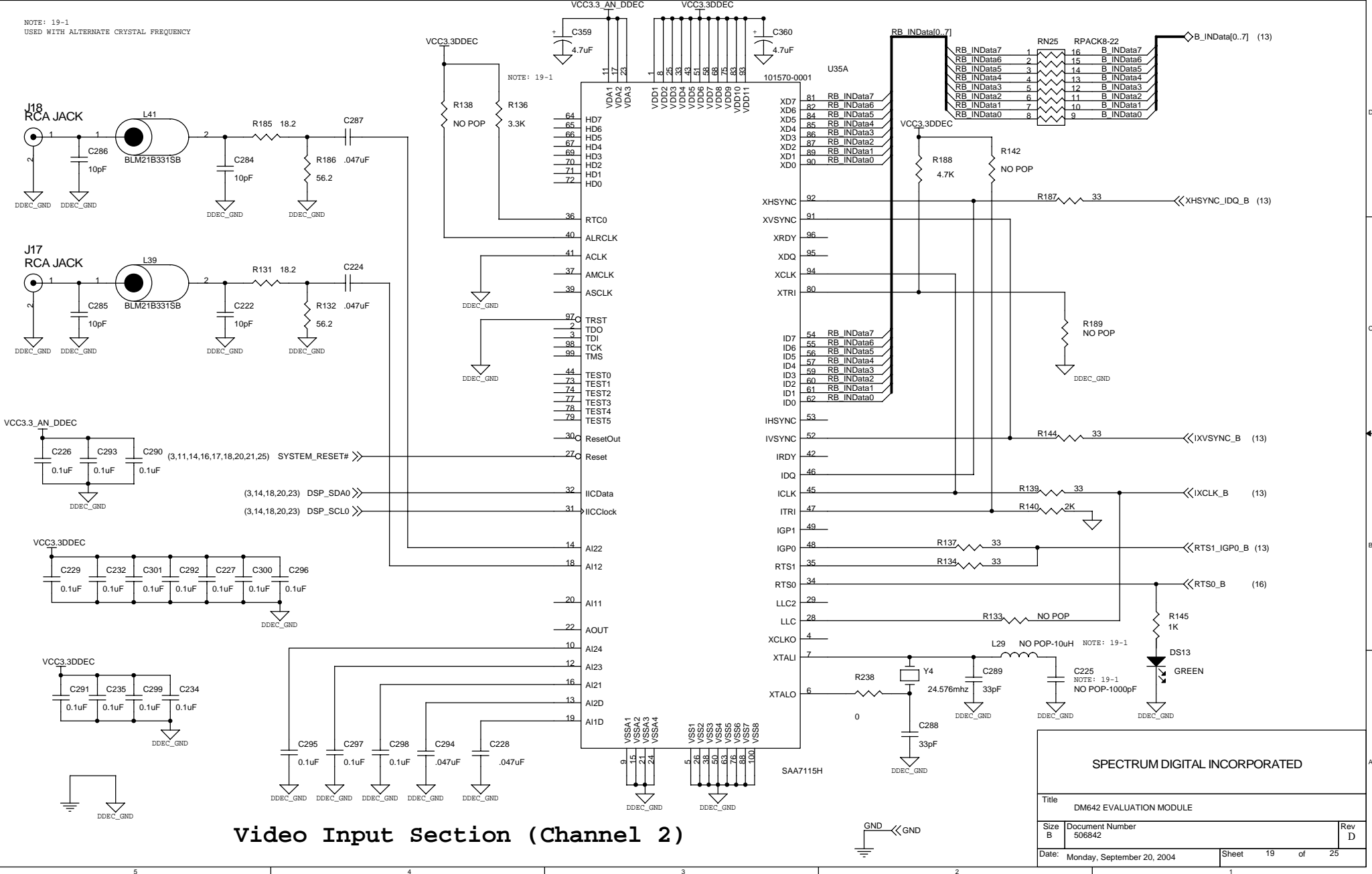
NOTE: 18-1  
USED WITH ALTERNATE CRYSTAL FREQUENCY



**Video Input Section (Channel 1)**

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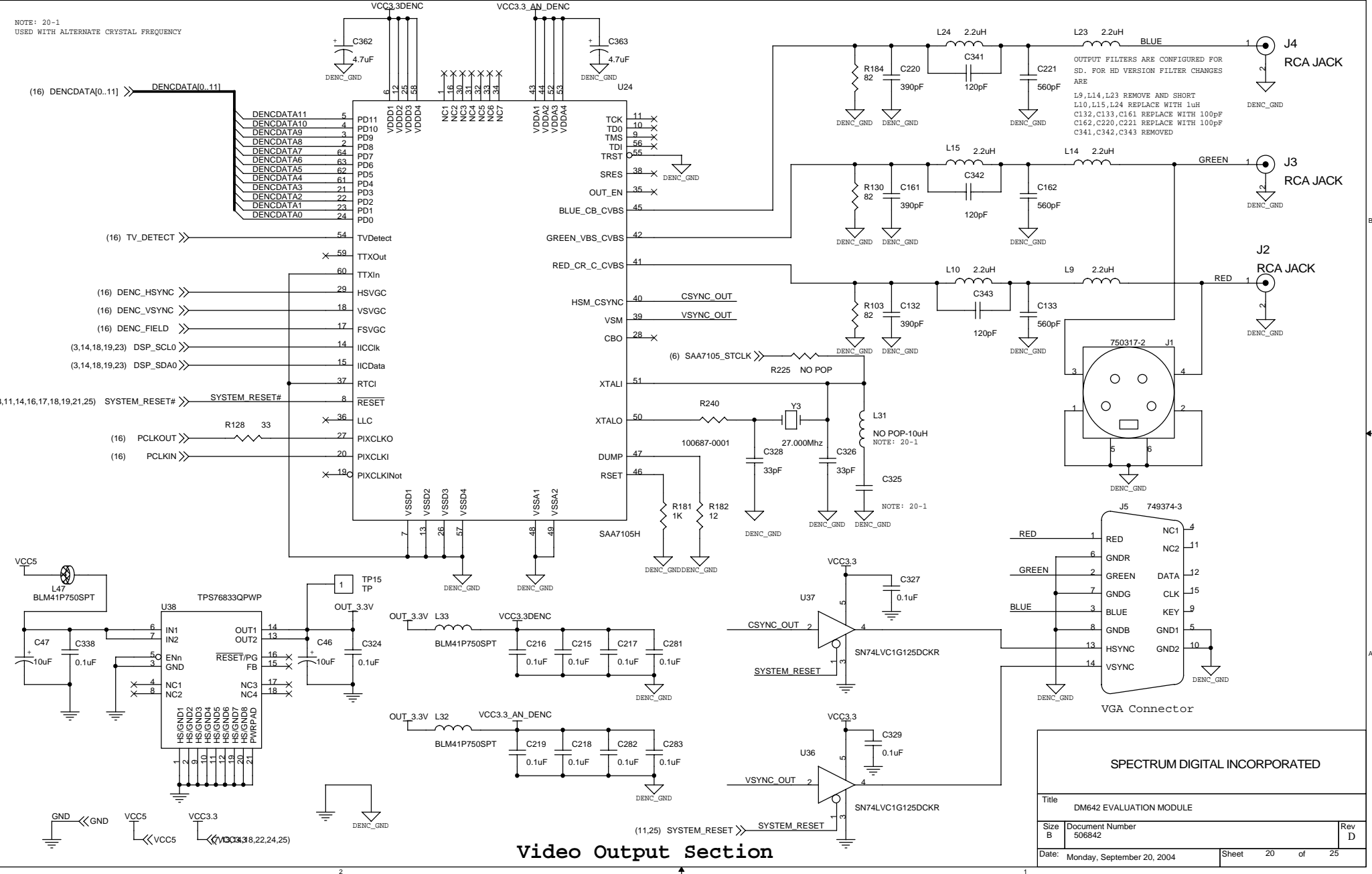
NOTE: 19-1  
USED WITH ALTERNATE CRYSTAL FREQUENCY



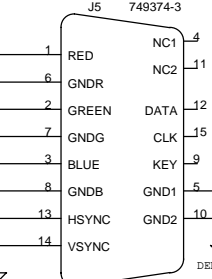
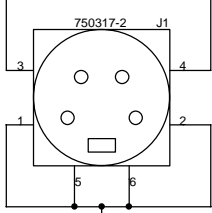
### Video Input Section (Channel 2)

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NOTE: 20-1  
USED WITH ALTERNATE CRYSTAL FREQUENCY

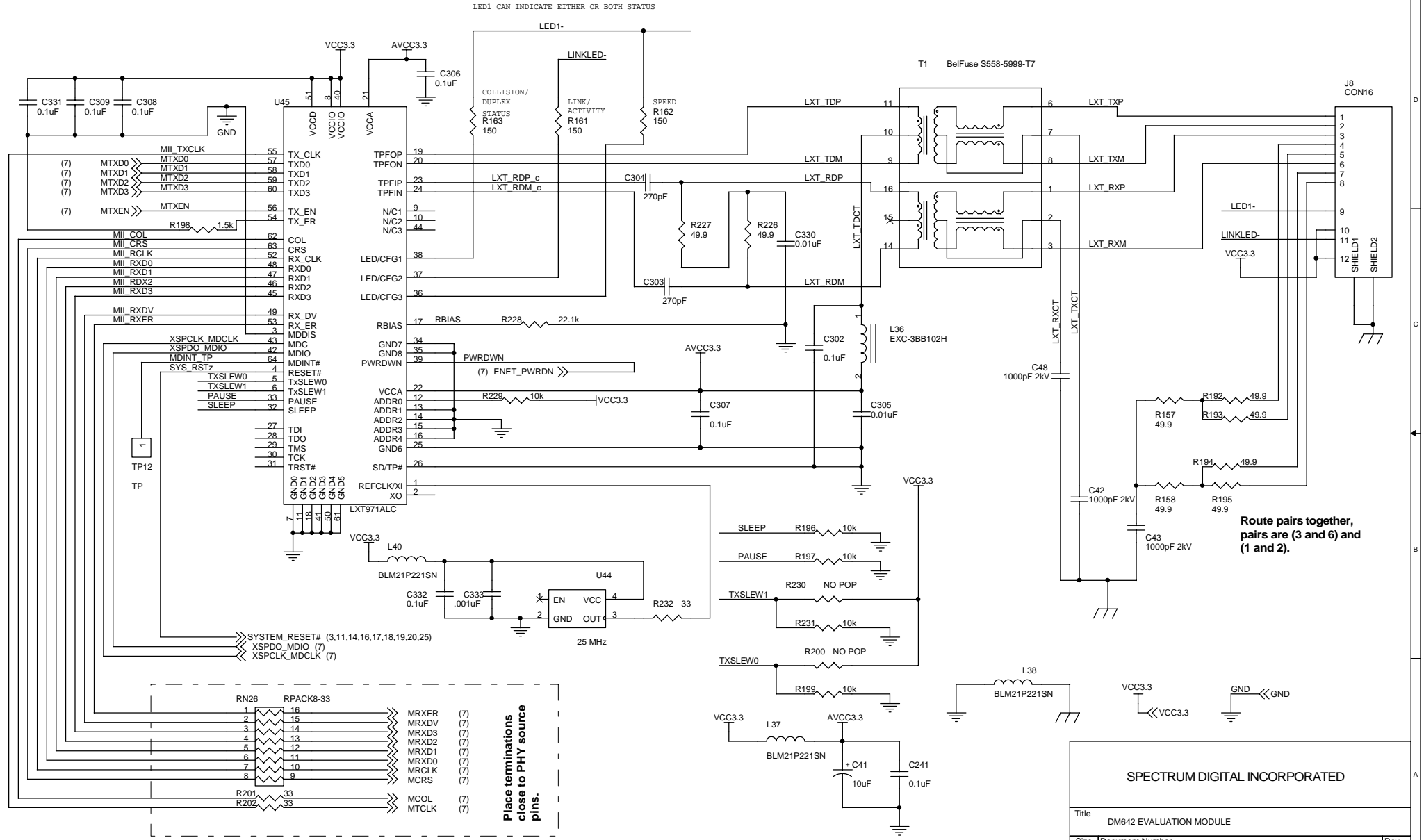


OUTPUT FILTERS ARE CONFIGURED FOR SD. FOR HD VERSION FILTER CHANGES ARE  
L9, L14, L23 REMOVE AND SHORT  
L10, L15, L24 REPLACE WITH 1uH  
C132, C133, C161 REPLACE WITH 100pF  
C162, C220, C221 REPLACE WITH 100pF  
C341, C342, C343 REMOVED



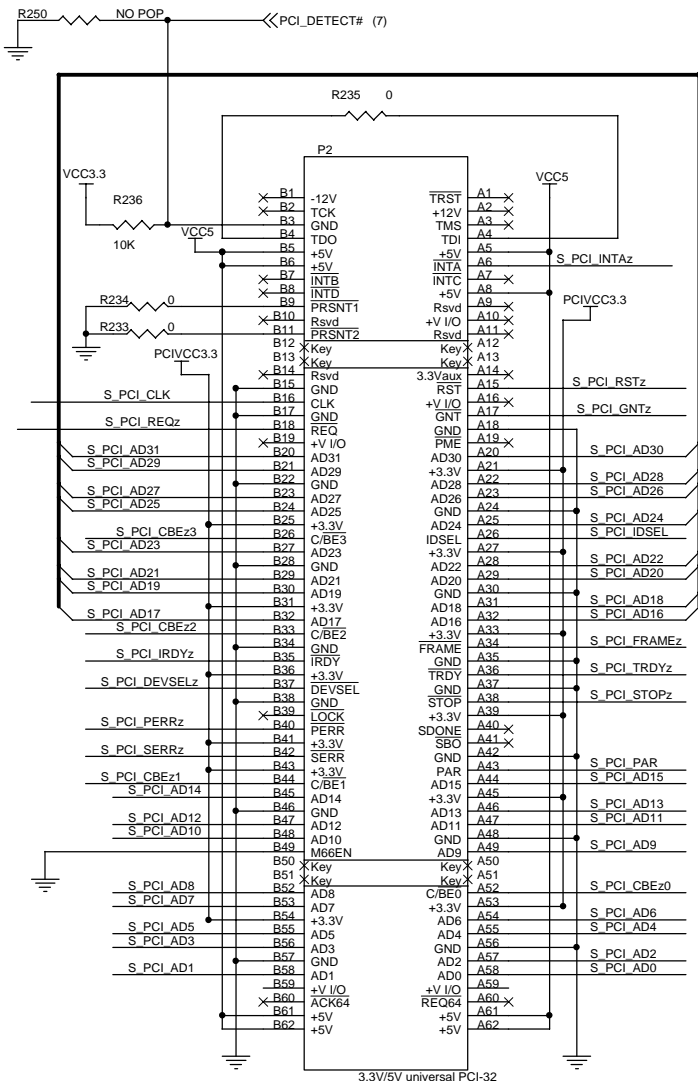
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### Video Output Section

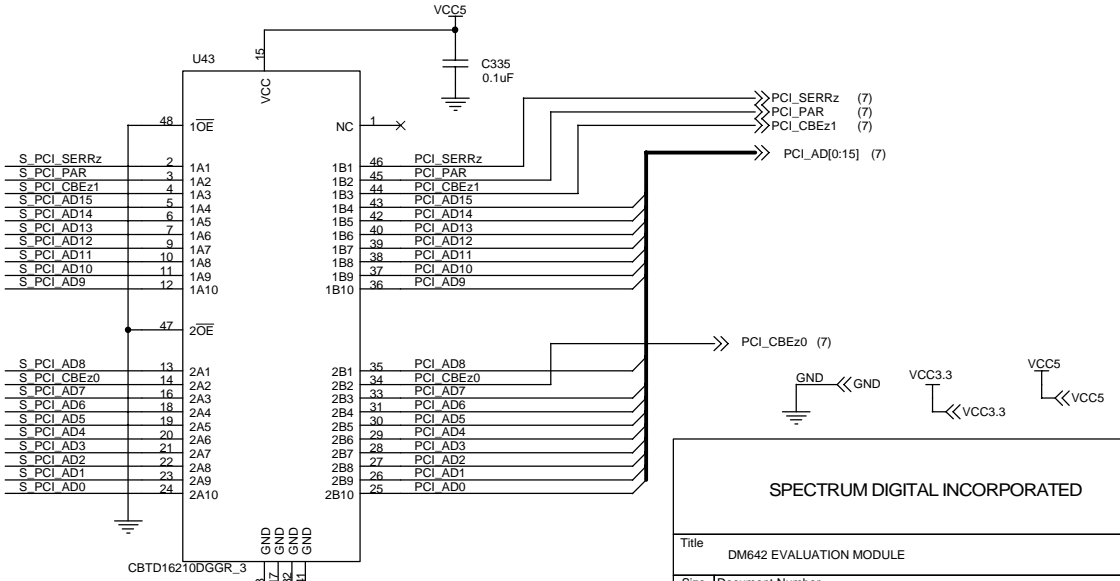
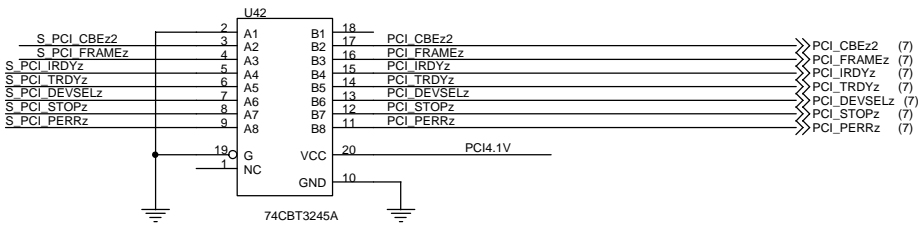
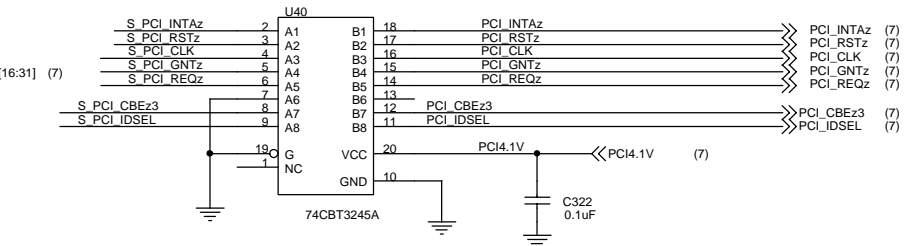


## ETHERNET PHY AND INTERFACE

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### PCI INTERFACE



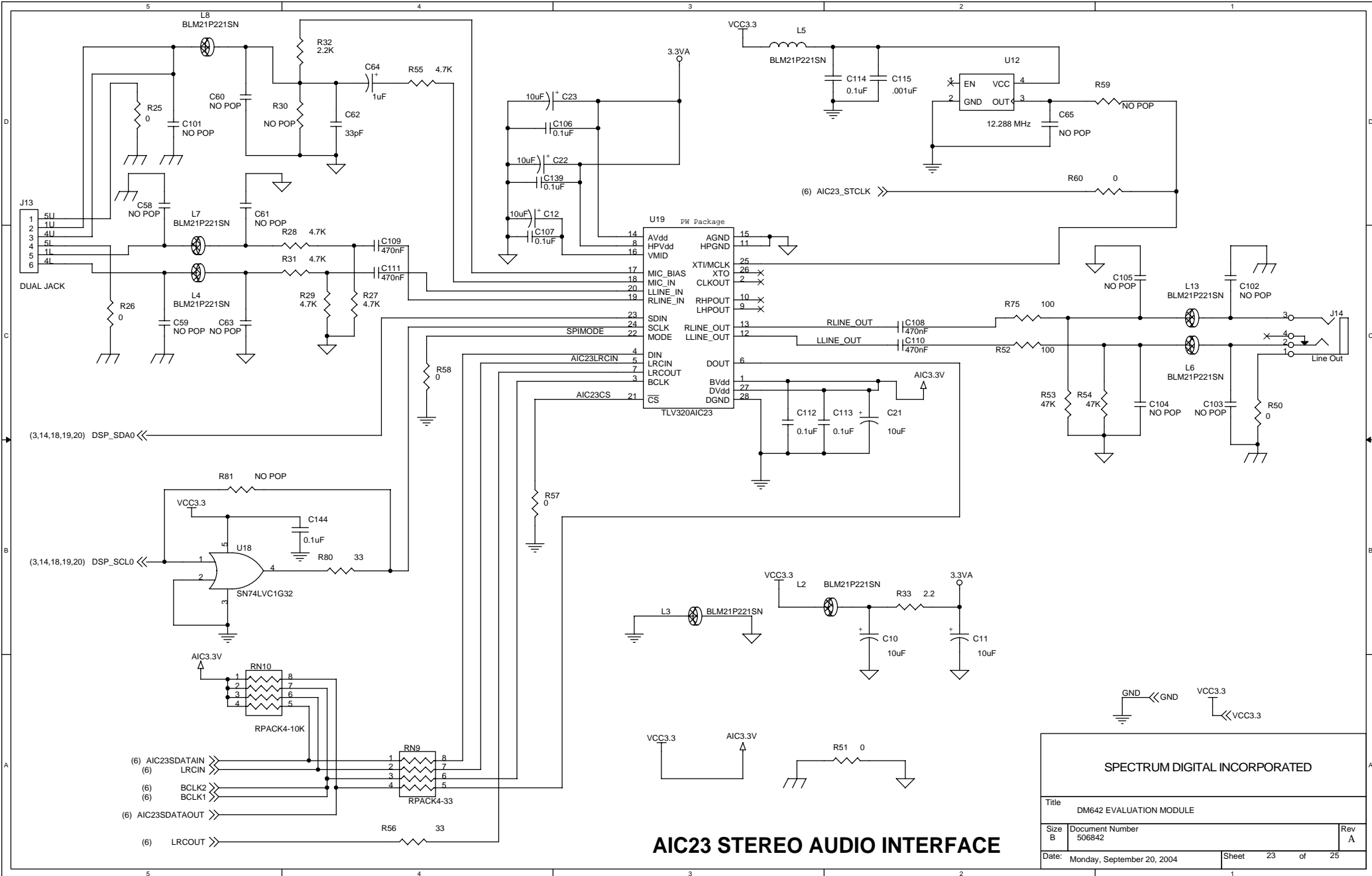
**SPECTRUM DIGITAL INCORPORATED**

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Title  
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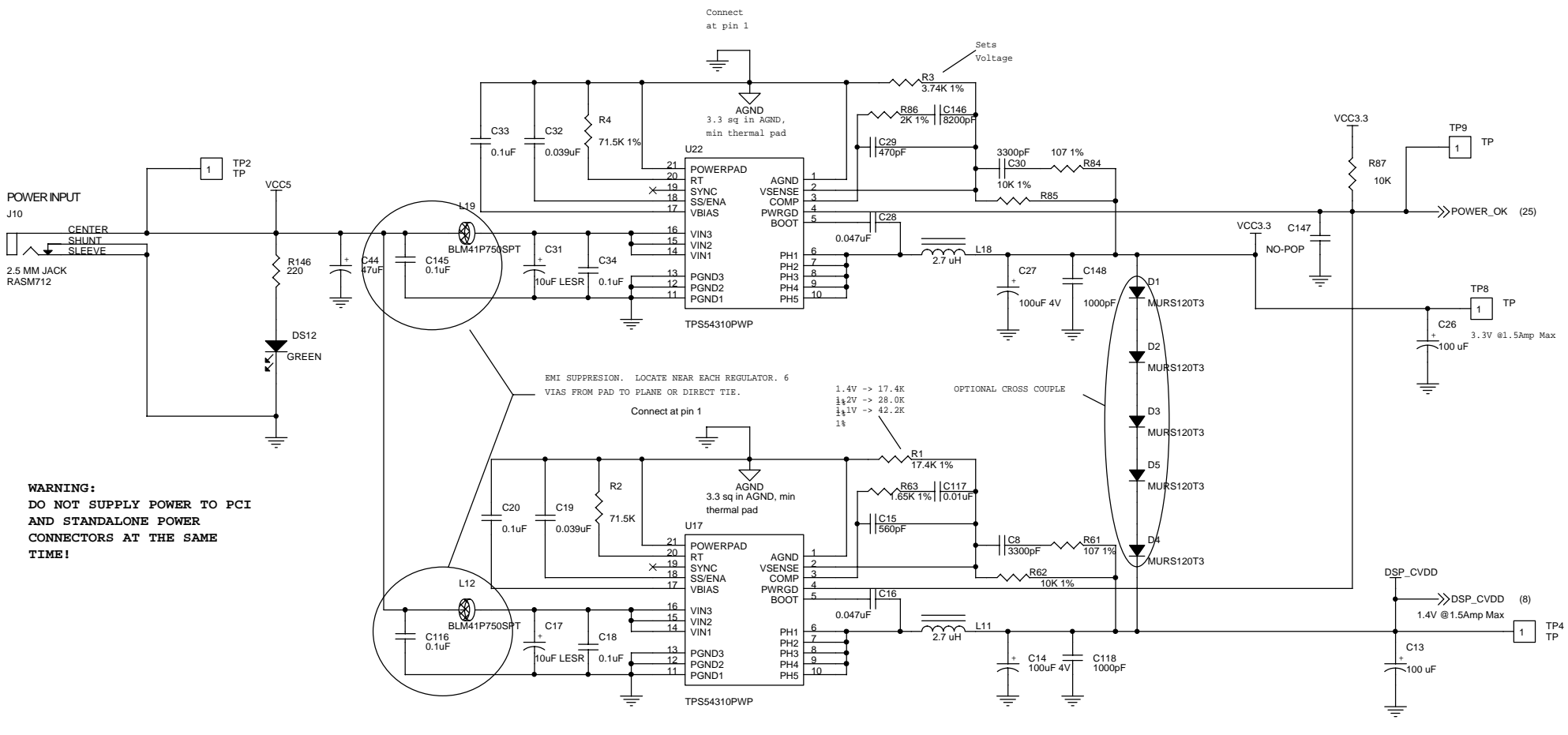
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# AIC23 STEREO AUDIO INTERFACE

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**WARNING:**  
DO NOT SUPPLY POWER TO PCI  
AND STANDALONE POWER  
CONNECTORS AT THE SAME  
TIME!

POWER ESTIMATES BASED ON SPRU190

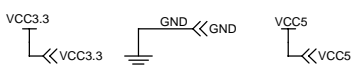
1.4V@600MHz	1.09 W	0.778A
3.3V@600MHz	0.52 W	0.157A ( no emif clk)

MEASURED CURRENT ON C6416TEB, ~0.7A@5V

EACH REGULATOR CAN SUPPLY UP TO 3A OF CURRENT. HOWEVER COMPONENT VALUES HAVE BEEN SELECTED FOR 1.5A OPERATION.

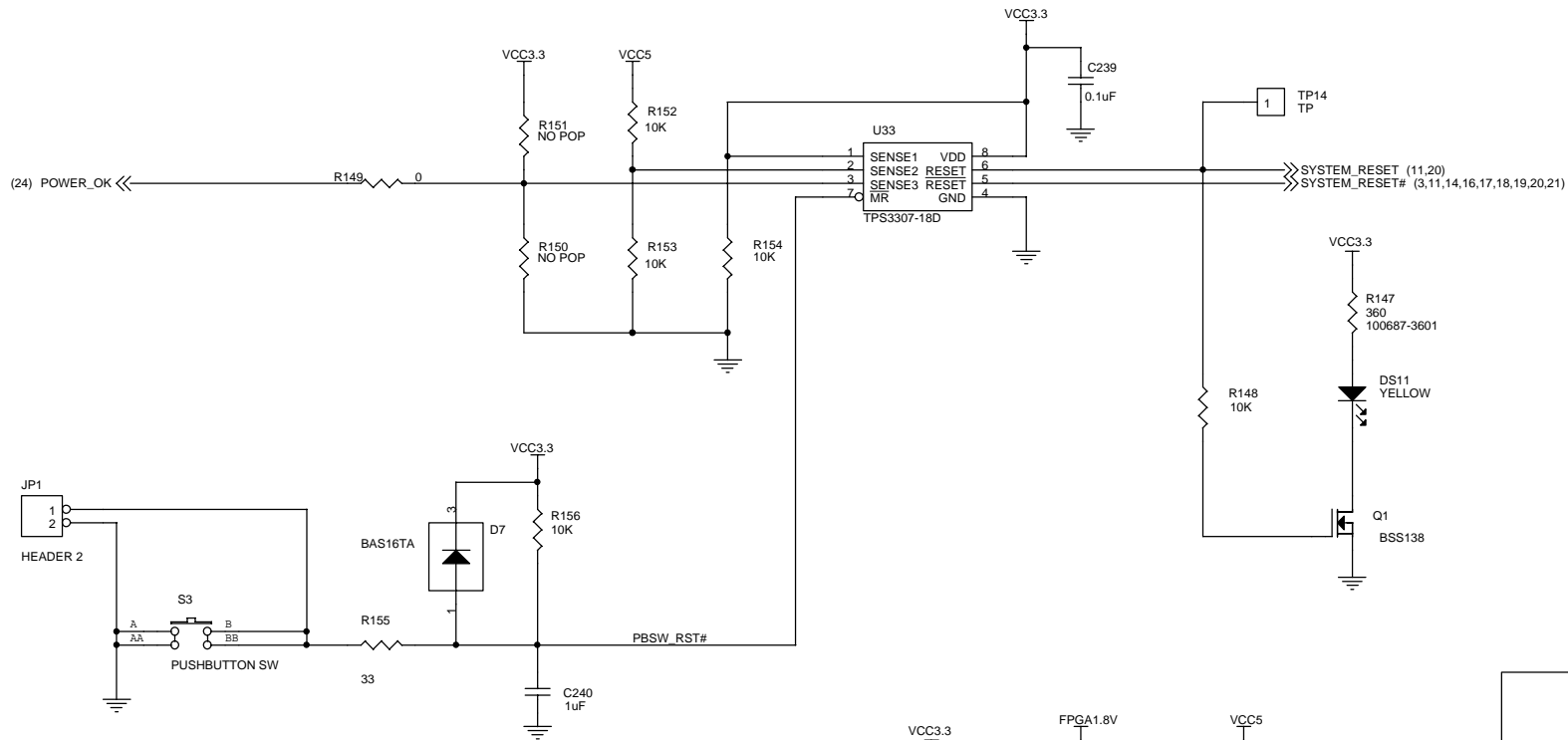
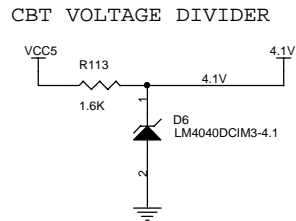
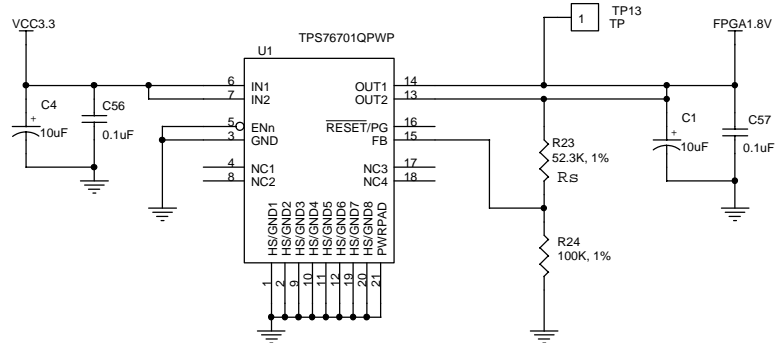
VALUES CALCULATED WITH SWIFT DESIGN TOOL 2.0. FOLLOW TPS54310 EVM LAYOUT

## POWER

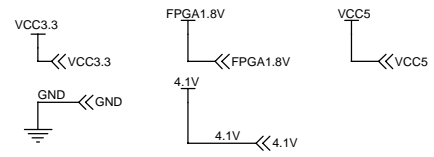


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### FPGA POWER AND RESET CIRCUITRY



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