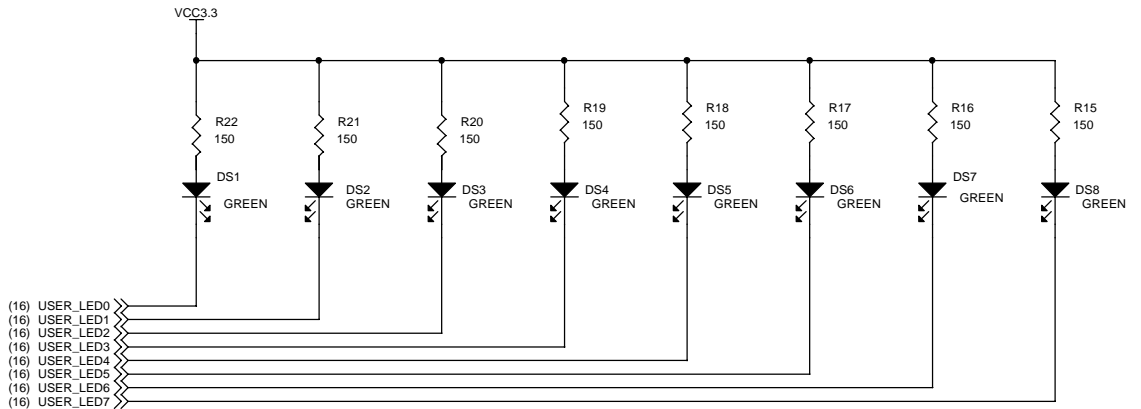
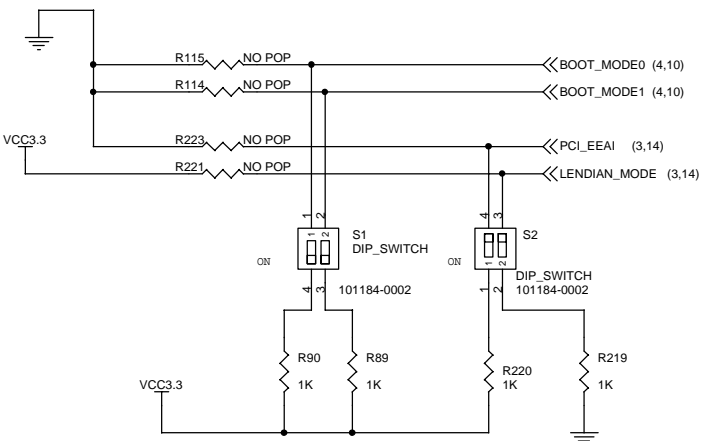


EMIF_ECLKINSEL[1:0]		
R42	R40	MODE SELECTED
NO POP	NO POP	ECLKIN(DEFAULT)
NO POP	1K OHM	CPU CLOCK /4 EMIF CLOCK
1K OHM	NO POP	CPU CLOCK /6 EMIF CLOCK
1K OHM	1K OHM	ECLKIN



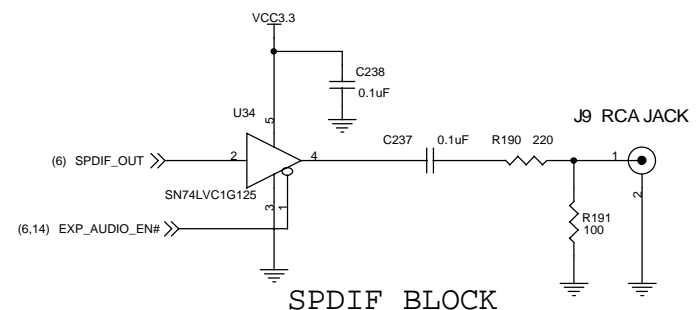
USER LEDS



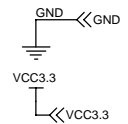
BOOT_MODE[1:0]		
S1-2	S1-1	MODE SELECTED
OFF	OFF	NO BOOT (DEFAULT)
OFF	ON	HPI/PCI BOOT MODE
ON	OFF	RESERVED
ON	ON	EMIF 8 BIT ROM BOOT

PCI MODE CONFIGURATION	
S2-1(PCI ROM)	MODE SELECTED
OFF	PCI EPROM DISABLED(DEFAULT)
ON	PCI ROM ENABLED

ENDIAN MODE CONFIGURATION	
S2-2(ENDIAN)	MODE SELECTED
OFF	LITTLE ENDIAN MODE (DEFAULT)
ON	BIG ENDIAN MODE

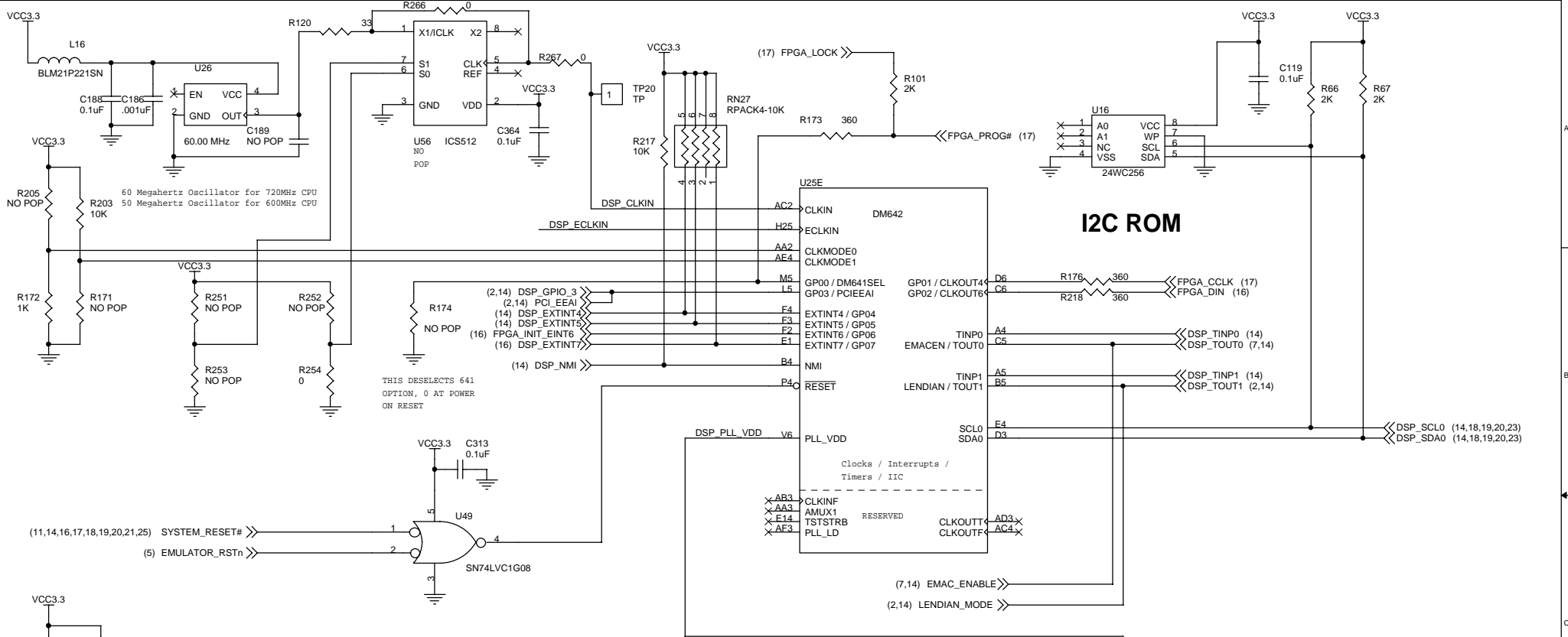


SPDIF BLOCK



LEDS/SWITCHES/CONFIGURATION INPUTS

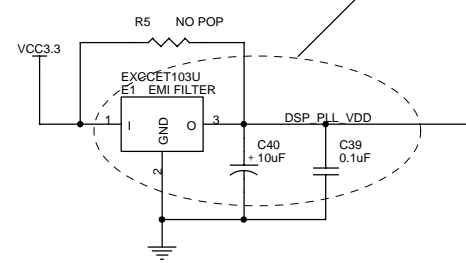
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THIS DESELECTS 641 OPTION, 0 AT POWER ON RESET

Place all PLL external components as close to the DSP. All PLL external components must be on a single side of the board.

S1	S0	MULTIPLY	OUTPUT
0	0	4X	100 MHz
0	OPEN	5.33X	133.25 MHz
0	1	5X	125 MHz
OPEN	0	2.5X	62.5 MHz
OPEN	OPEN	2X	50 MHz
OPEN	1	3.33X	83.25 MHz
1	0	6X	150 MHz
1	OPEN	3X	75 MHz
1	1	8X	200 MHz

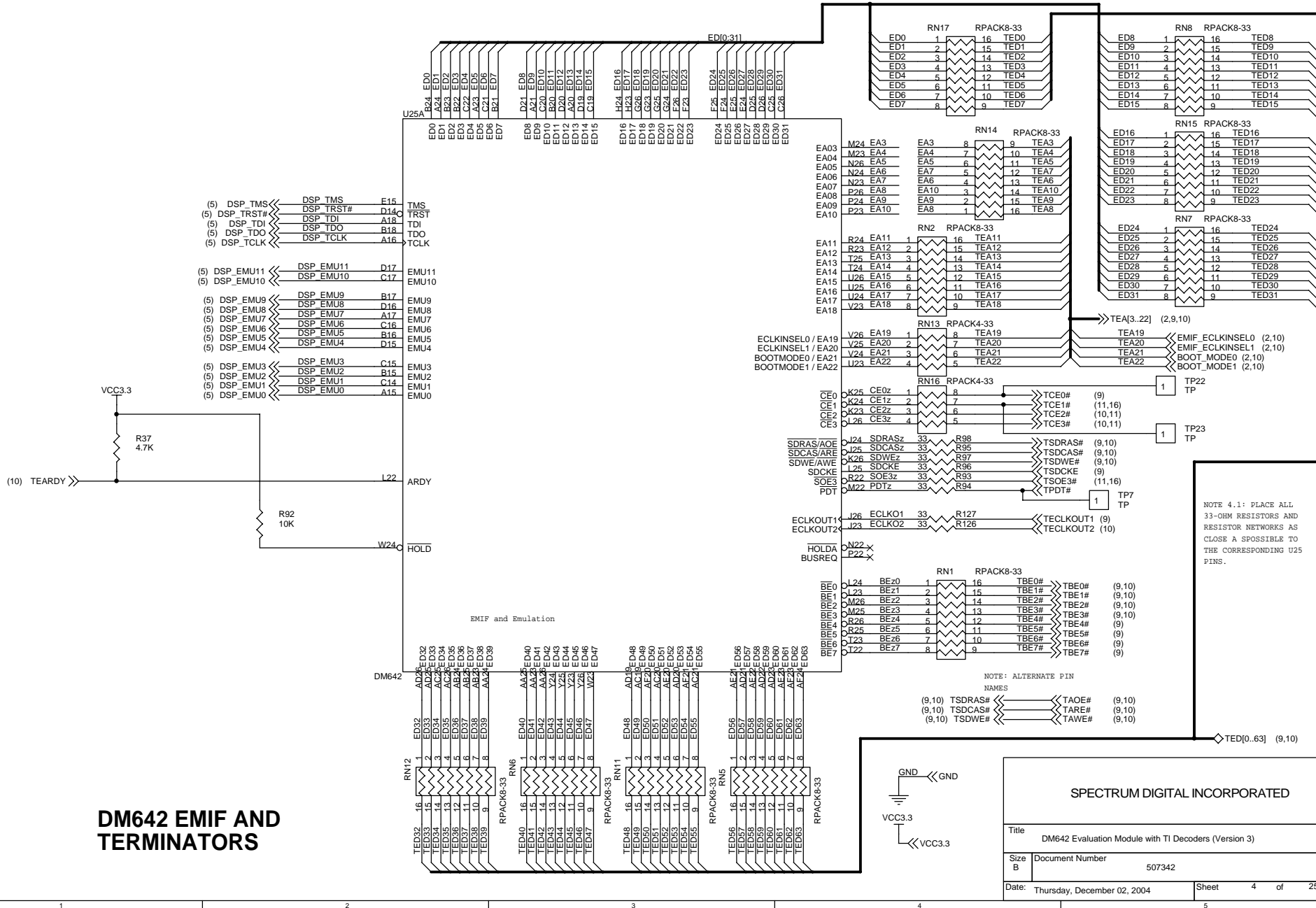


DM642 CLOCKS, RESET CIRCUITRY, I2C INTERFACE

SPECTRUM DIGITAL INCORPORATED

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DM642 EMIF AND TERMINATORS

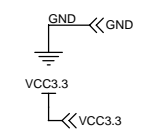


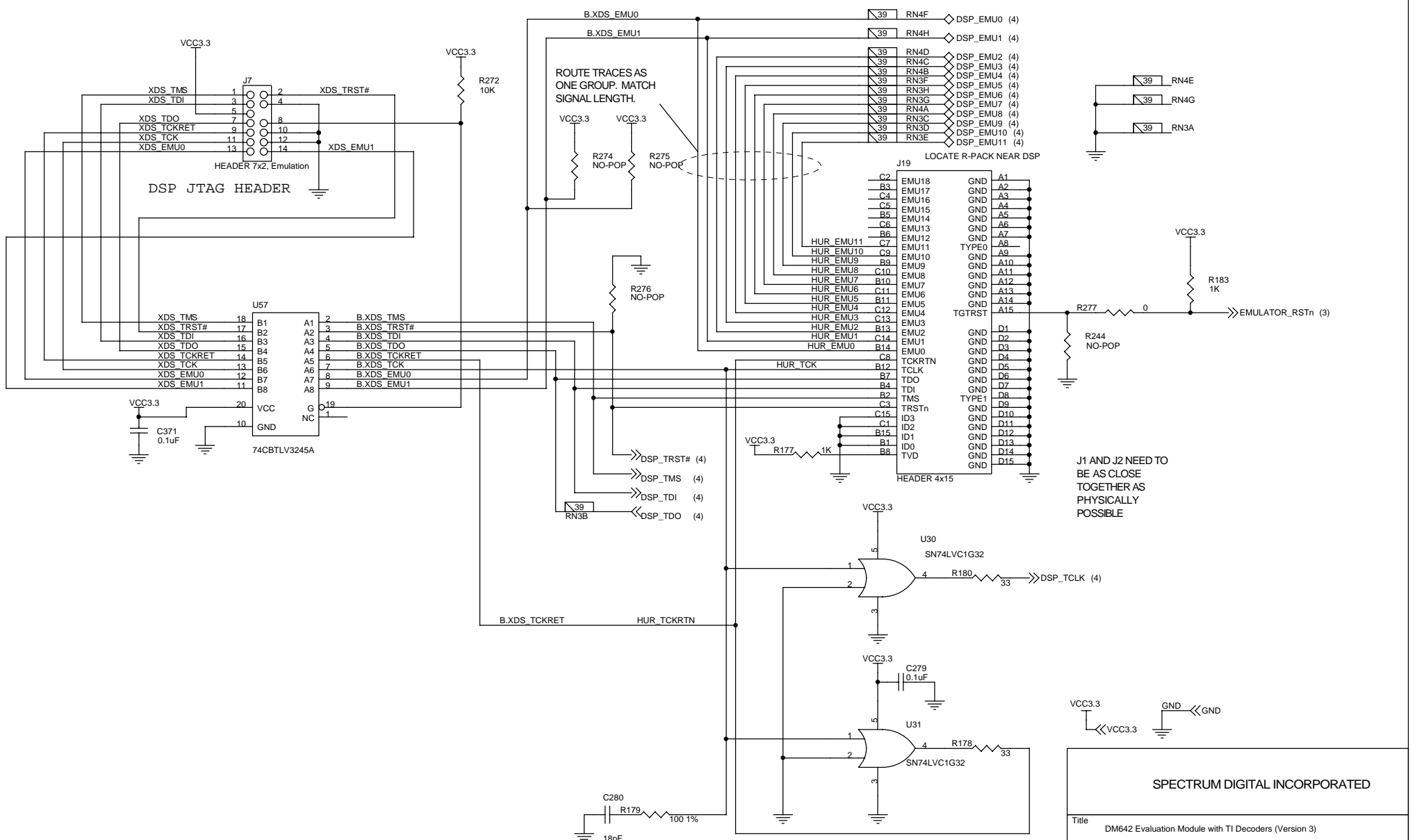
SPECTRUM DIGITAL INCORPORATED

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NOTE 4.1: PLACE ALL 33-OHM RESISTORS AND RESISTOR NETWORKS AS CLOSE AS POSSIBLE TO THE CORRESPONDING U25 PINS.

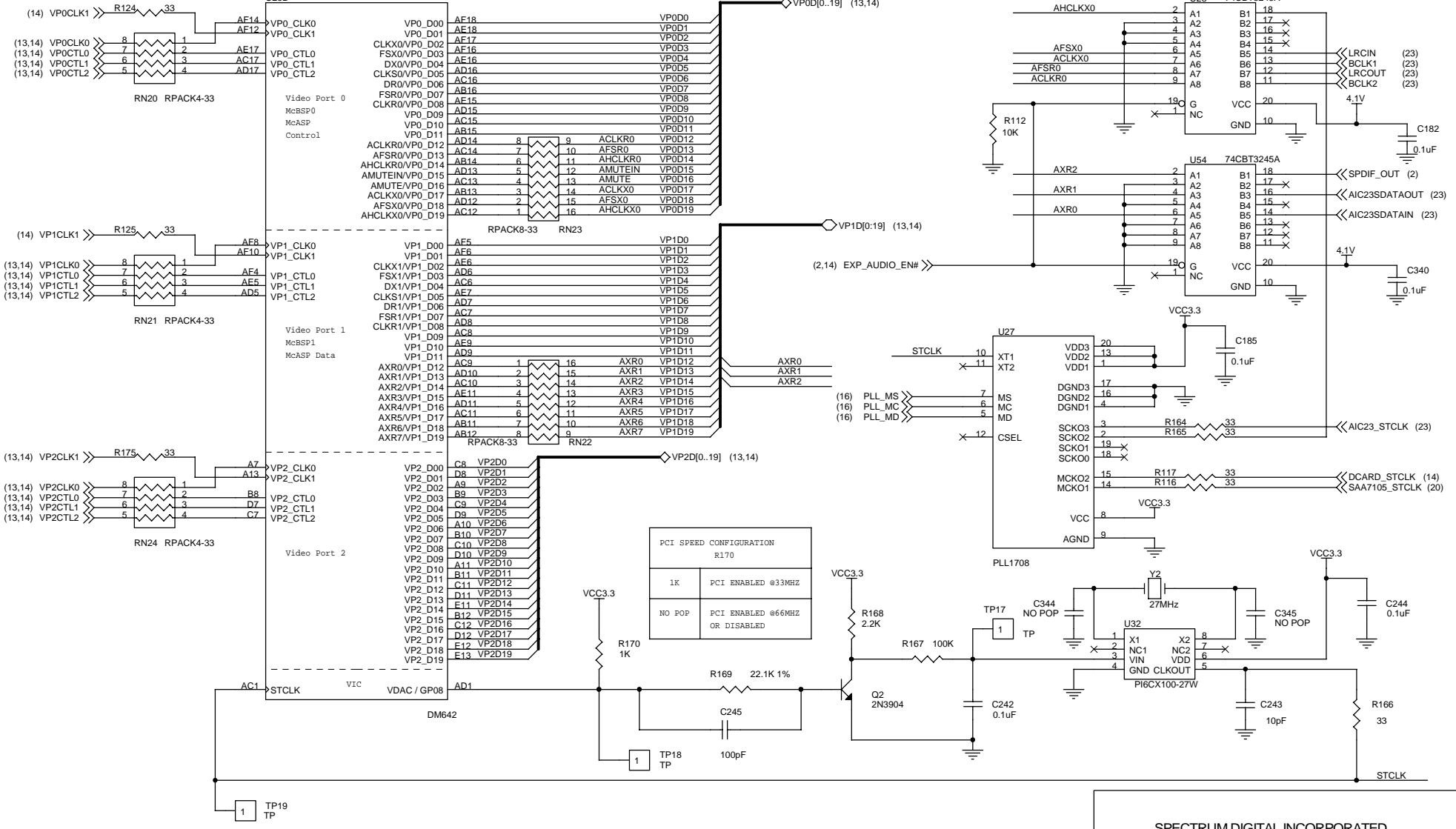
NOTE: ALTERNATE PIN NAMES





EMULATION

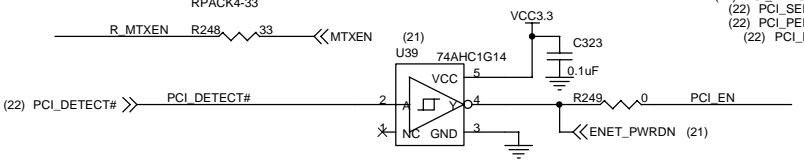
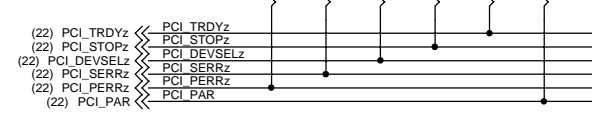
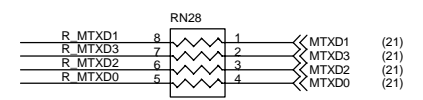
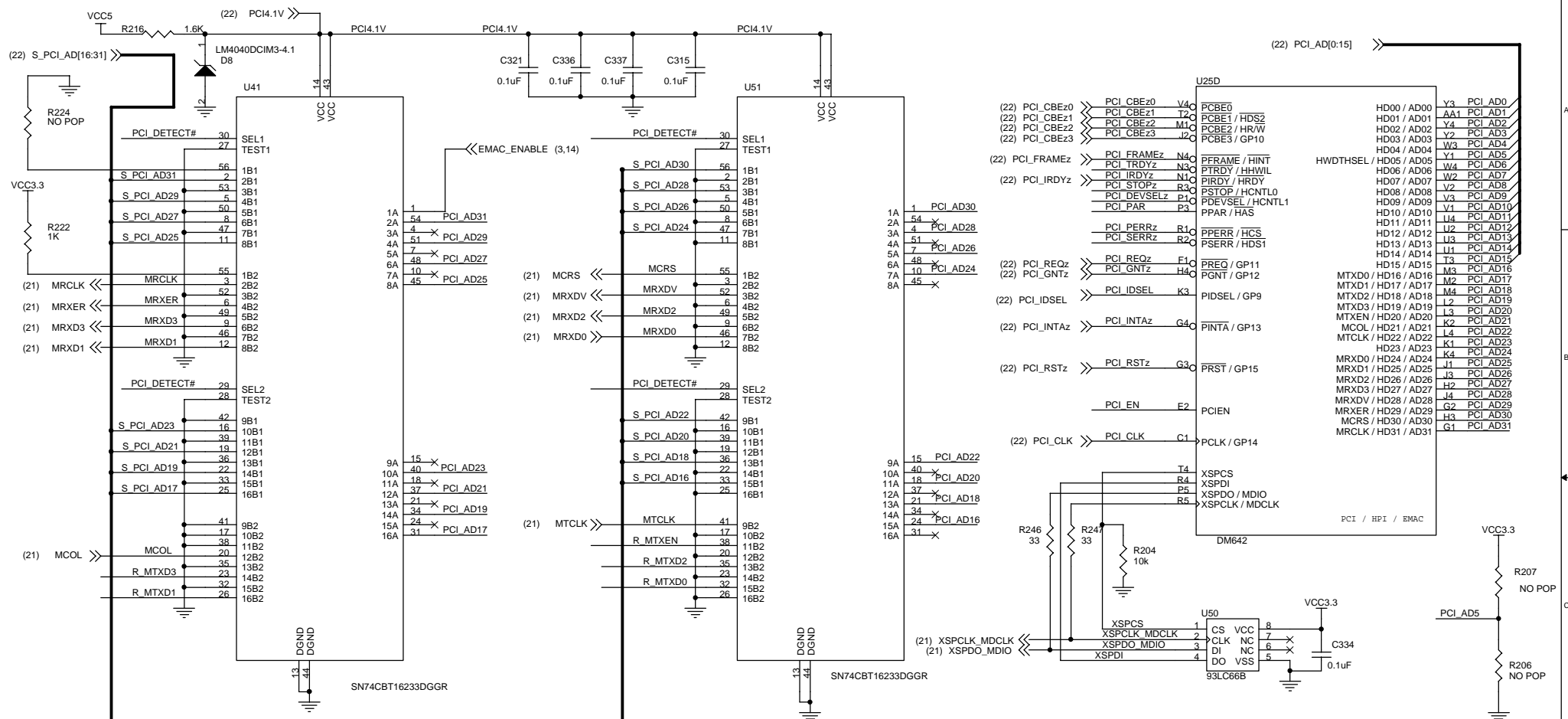
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DM642 VIDEO PORTS

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DM642 PCI/HPI/EMAC INTERFACES

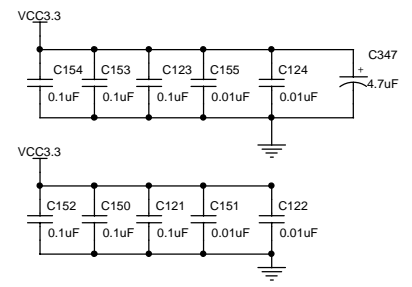
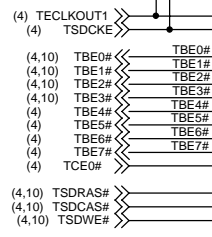
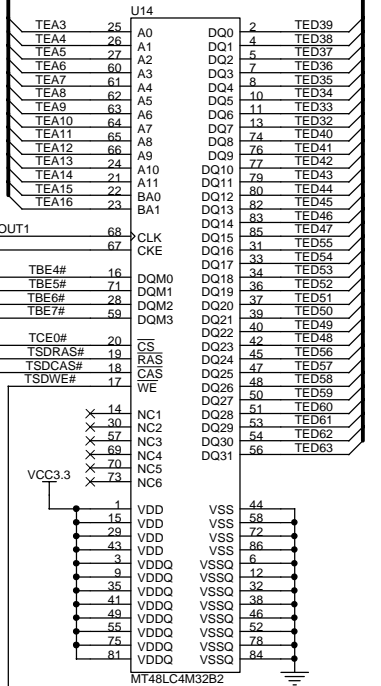
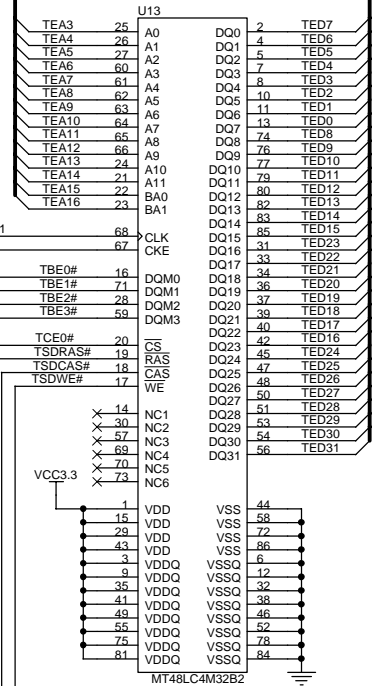
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R206 AND R207 ARE USED TO CONFIGURE THE HPI WIDTH

(2,4,10) TEA[3..22] <<<

(4,10) TED[0..63] <<<

TED[0:63]



SDRAM MEMORY

SPECTRUM DIGITAL, INCORPORATED

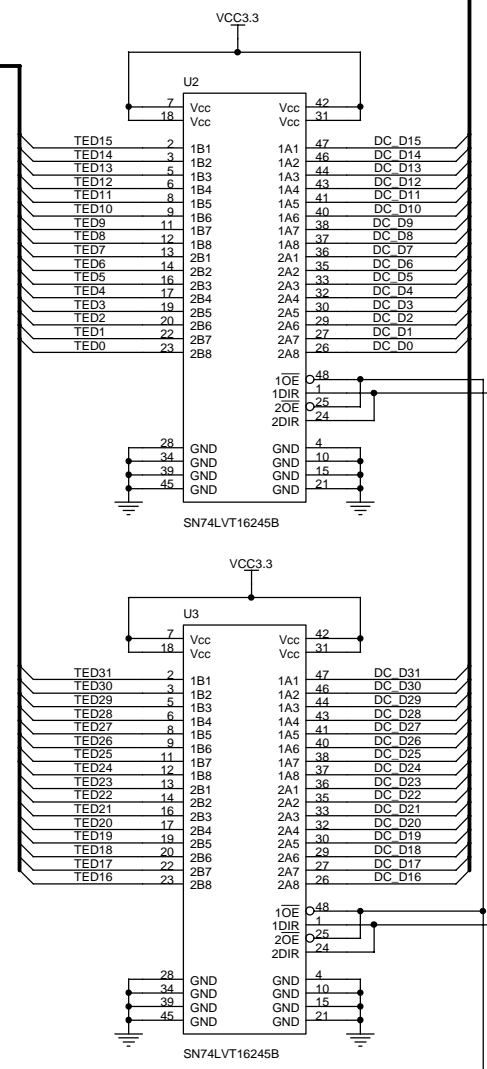
Title		
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(2,4,9) TEA[3..22]

(4,9) TED[0..63]

DC_D[31..0] (11,15,16)

DC_A[22..3] (11,15,16)



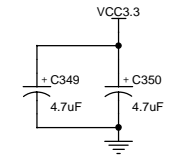
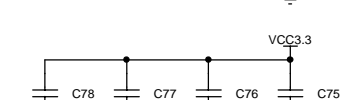
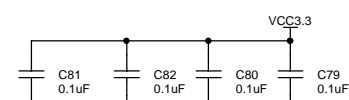
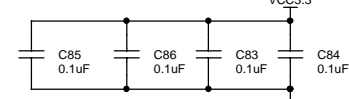
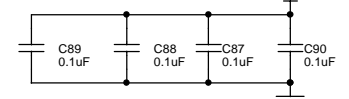
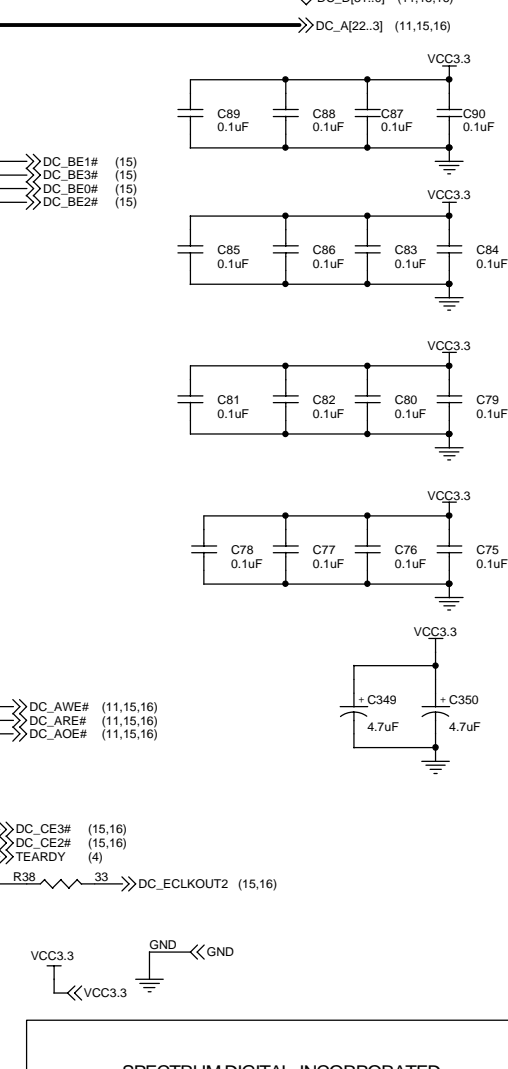
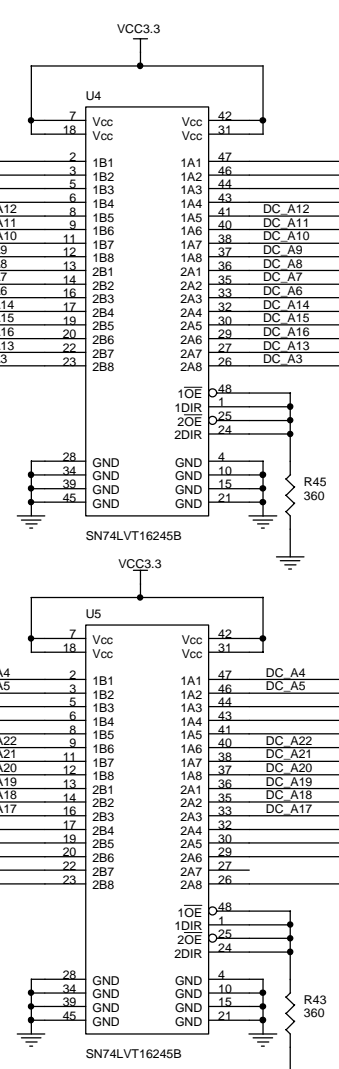
#OE DIR OPERATION
 L L A ← B
 L H A → B
 H X ISOLATION

(4,9) TBE1#
 (4,9) TBE3#
 (4,9) TBE0#
 (4,9) TBE2#

(4,9) TSDWE#
 (4,9) TSDCAS#
 (4,9) TSDRAS#

(4,11) TCE3#
 (4,11) TCE2#
 (15) DC_ARDY

(4) TECLKOUT2

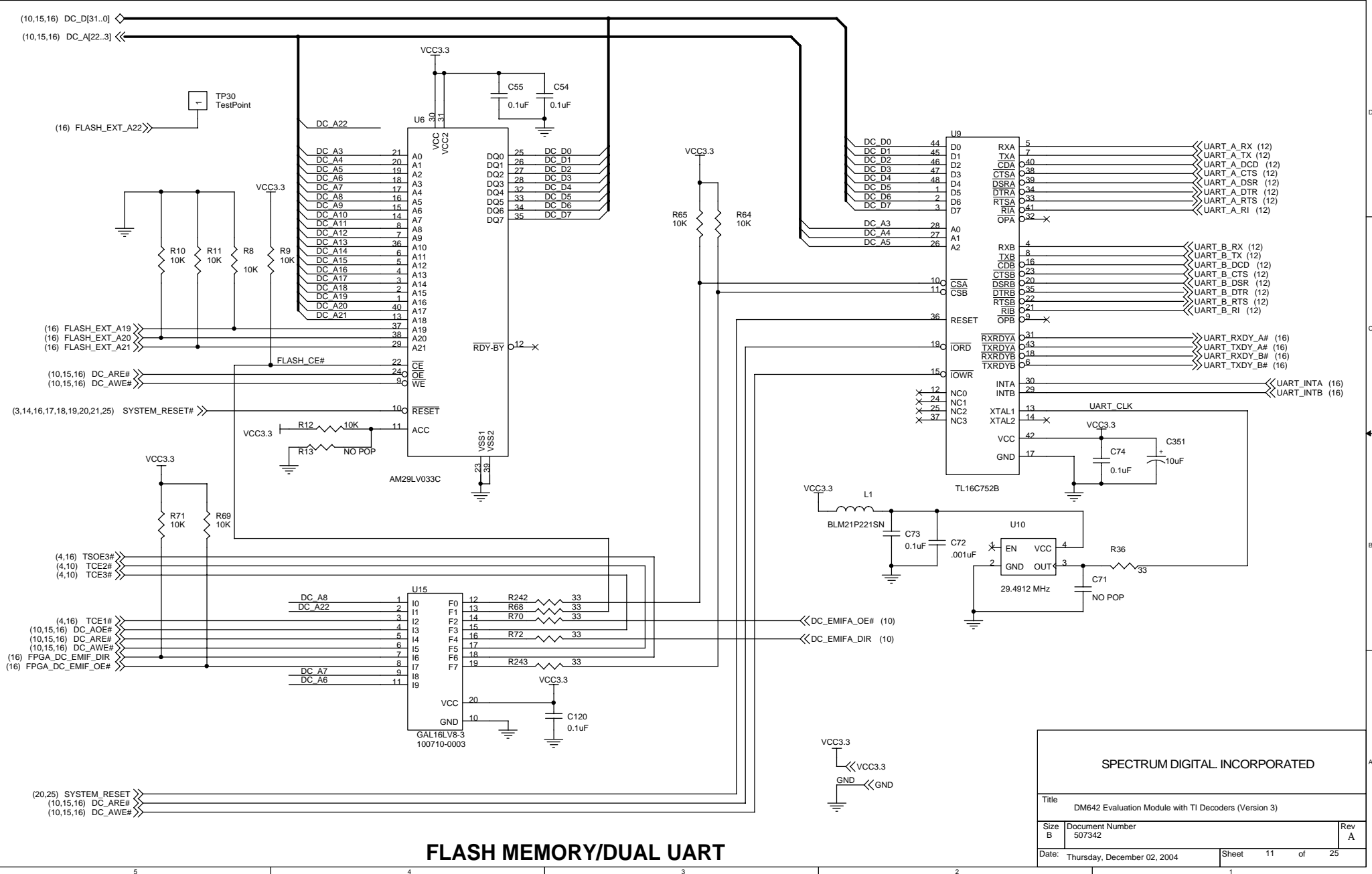


(11) DC_EMIFA_OE#

(11) DC_EMIFA_DIR

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DAUGHTER CARD BUFFERING



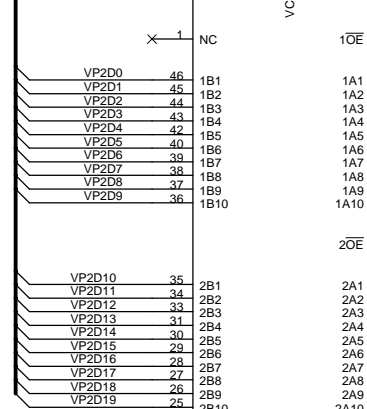
FLASH MEMORY/DUAL UART

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(6,14) VP2D[0..19]

VP2D[0..19]

U47
CBTD16210DGGR_3
101115-0001



(14) EXP_DISPLAY_EN#

VDATA[0..19] << VDATA[0..19] (16)

(6,14) VP2CLK1
(6,14) VP2CTL0
(6,14) VP2CTL1
(6,14) VP2CTL2
(6,14) VP2CLK0

EXP_DISPLAY_EN#

4.1V

U46
Vcc 24
1A1 1B1
1A2 1B2
1A3 1B3
1A4 1B4
1A5 1B5

1OE

2A1 2B1

17 16

2A2 2B2

18 19

2A3 2B3

20 21

2A4 2B4

22 23

2A5 2B5

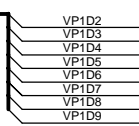
13OE

12GND

SN74CBTS3384

>> SW_VP2CLK1 (16)
>> SW_VP2CTL0 (16)
>> SW_VP2CTL1 (16)
>> SW_VP2CTL2 (16)
>> SW_VP2CLK0 (16)

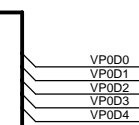
(6,14) VP1D[0..19]



(14) EXP_CAPTURE2_EN#

EXP_CAPTURE2_EN#

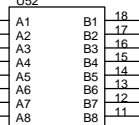
(6,14) VP0D[0..19]



(14) EXP_CAPTURE1_EN#

EXP_CAPTURE1_EN#

U52
74CBT3245A



19G

20VCC

1NC

10GND

SN74CBTS3384

4.1V

18B INData0

17B INData1

16B INData2

15B INData3

14B INData4

13B INData5

12B INData6

11B INData7

20VCC

19G

1NC

10GND

SN74CBTS3384

4.1V

24Vcc

1A1 1B1

2 5

1A2 1B2

7 6

1A3 1B3

8 9

1A4 1B4

11 10

1A5 1B5

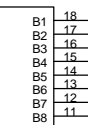
1OE

13GND

12GND

SN74CBTS3384

U53



24Vcc

1A1 1B1

2 5

1A2 1B2

7 6

1A3 1B3

8 9

1A4 1B4

11 10

1A5 1B5

1OE

13GND

12GND

SN74CBTS3384

4.1V

24Vcc

1A1 1B1

2 5

1A2 1B2

7 6

1A3 1B3

8 9

1A4 1B4

11 10

1A5 1B5

1OE

13GND

12GND

SN74CBTS3384

4.1V

24Vcc

1A1 1B1

2 5

1A2 1B2

7 6

1A3 1B3

8 9

1A4 1B4

11 10

1A5 1B5

1OE

13GND

12GND

SN74CBTS3384

4.1V

24Vcc

1A1 1B1

2 5

1A2 1B2

7 6

1A3 1B3

8 9

1A4 1B4

11 10

1A5 1B5

1OE

13GND

12GND

SN74CBTS3384

4.1V

24Vcc

1A1 1B1

2 5

1A2 1B2

7 6

1A3 1B3

8 9

1A4 1B4

11 10

1A5 1B5

1OE

13GND

12GND

SN74CBTS3384

4.1V

24Vcc

1A1 1B1

2 5

1A2 1B2

7 6

1A3 1B3

8 9

1A4 1B4

11 10

1A5 1B5

1OE

13GND

12GND

SN74CBTS3384

4.1V

24Vcc

1A1 1B1

2 5

1A2 1B2

7 6

1A3 1B3

8 9

1A4 1B4

11 10

1A5 1B5

1OE

13GND

12GND

SN74CBTS3384

4.1V

24Vcc

1A1 1B1

2 5

1A2 1B2

7 6

1A3 1B3

8 9

1A4 1B4

11 10

1A5 1B5

1OE

13GND

12GND

SN74CBTS3384

4.1V

24Vcc

1A1 1B1

2 5

1A2 1B2

7 6

1A3 1B3

8 9

1A4 1B4

11 10

1A5 1B5

1OE

13GND

12GND

SN74CBTS3384

4.1V

24Vcc

1A1 1B1

2 5

1A2 1B2

7 6

1A3 1B3

8 9

1A4 1B4

11 10

1A5 1B5

1OE

13GND

12GND

SN74CBTS3384

4.1V

24Vcc

1A1 1B1

2 5

1A2 1B2

7 6

1A3 1B3

8 9

1A4 1B4

11 10

1A5 1B5

1OE

13GND

12GND

SN74CBTS3384

4.1V

24Vcc

1A1 1B1

2 5

1A2 1B2

7 6

1A3 1B3

8 9

1A4 1B4

11 10

1A5 1B5

1OE

13GND

12GND

SN74CBTS3384

4.1V

24Vcc

1A1 1B1

2 5

1A2 1B2

7 6

1A3 1B3

8 9

1A4 1B4

11 10

1A5 1B5

1OE

13GND

12GND

SN74CBTS3384

4.1V

24Vcc

1A1 1B1

2 5

1A2 1B2

7 6

1A3 1B3

8 9

1A4 1B4

11 10

1A5 1B5

1OE

13GND

12GND

SN74CBTS3384

4.1V

24Vcc

1A1 1B1

2 5

1A2 1B2

7 6

1A3 1B3

8 9

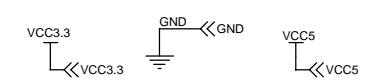
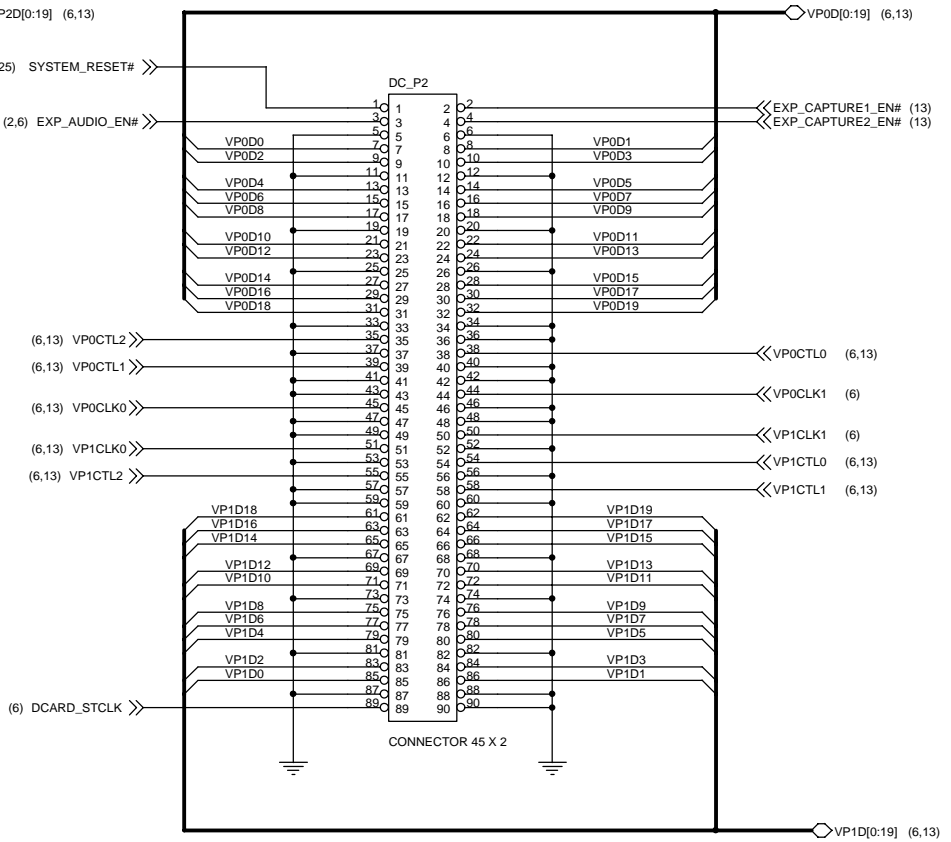
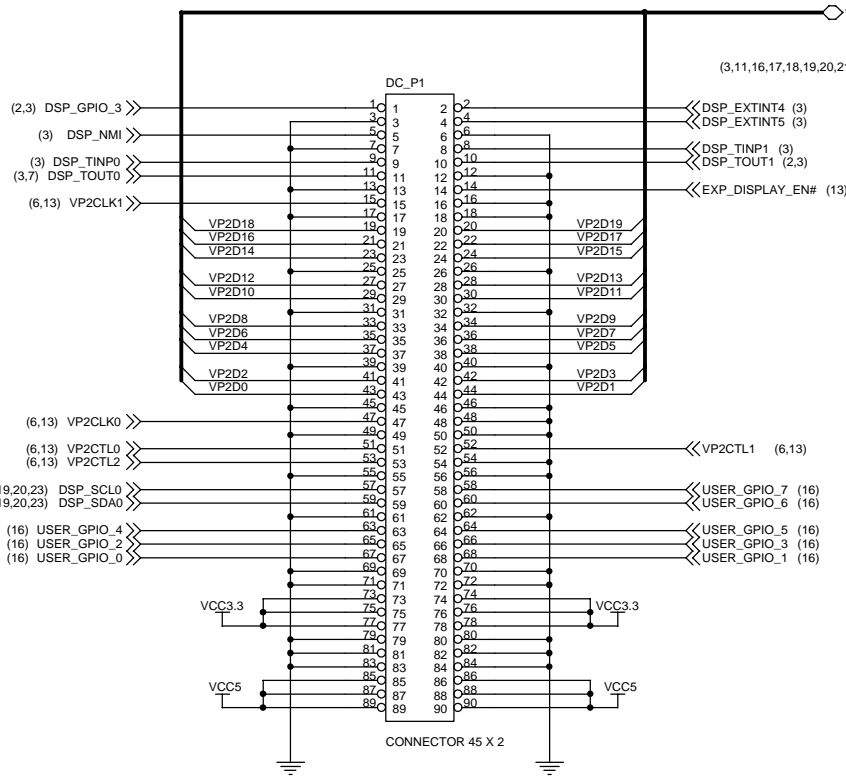
1A4 1B4

11 10

1A5 1B5

1OE

13

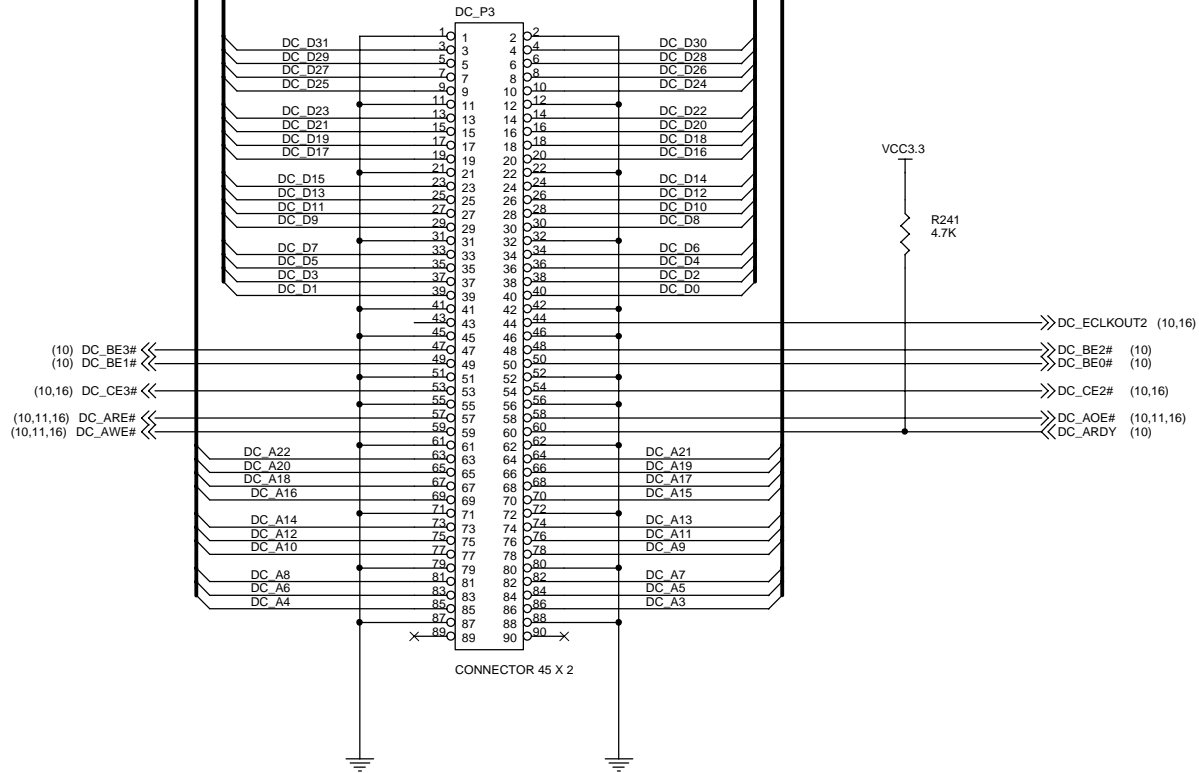


VIDEO PORTS DAUGHTER CARD CONNECTIONS

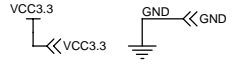
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(10,11,16) DC_A[22..3] <<

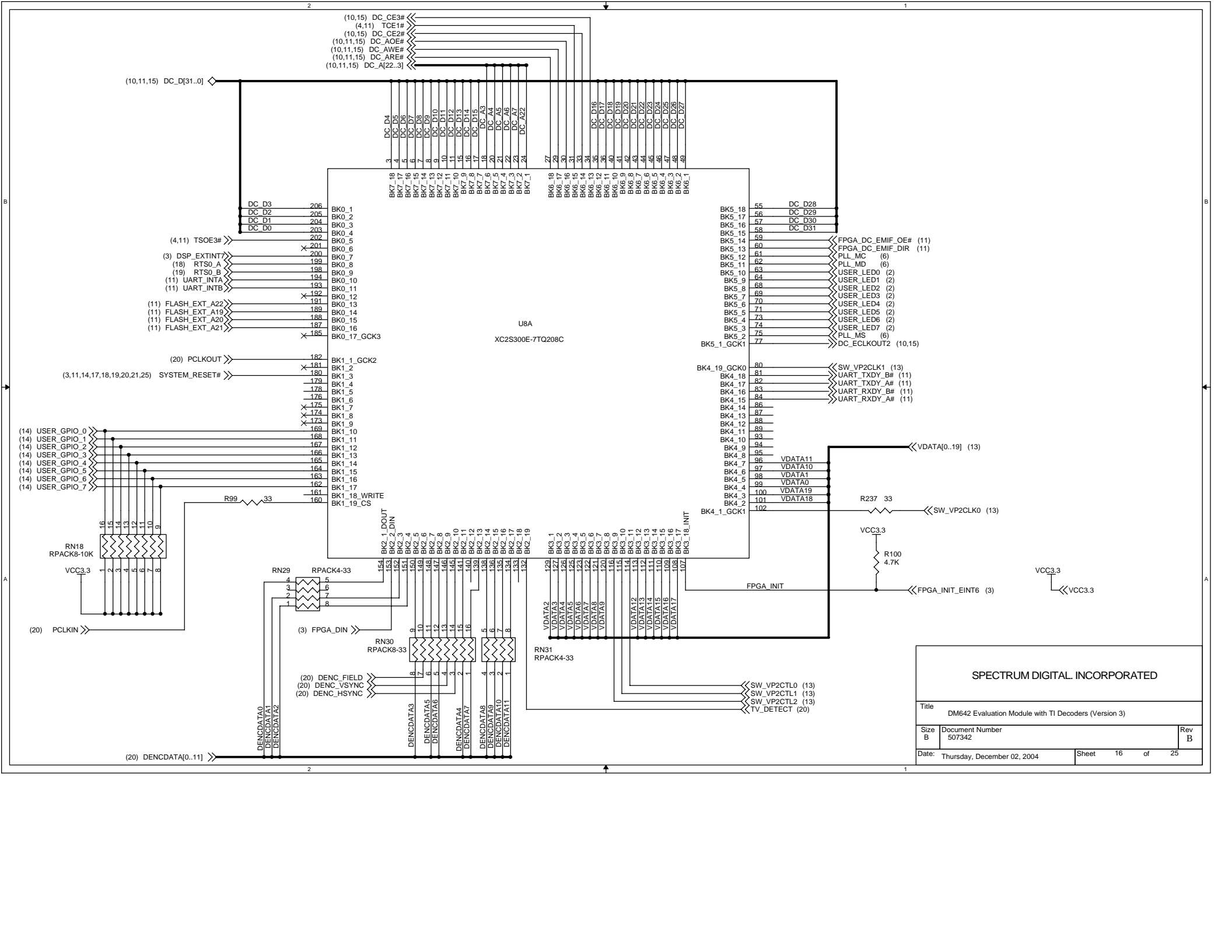
(10,11,16) DC_D[31..0] <<



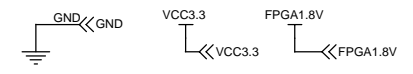
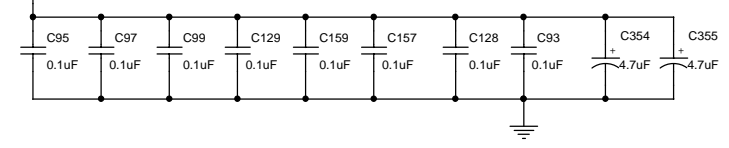
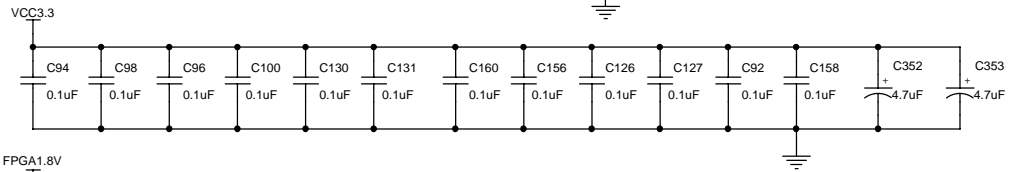
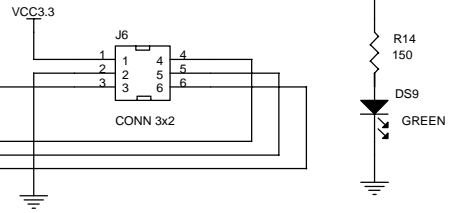
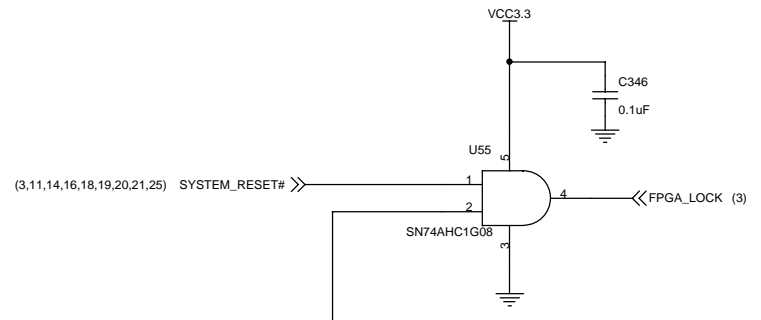
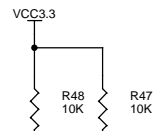
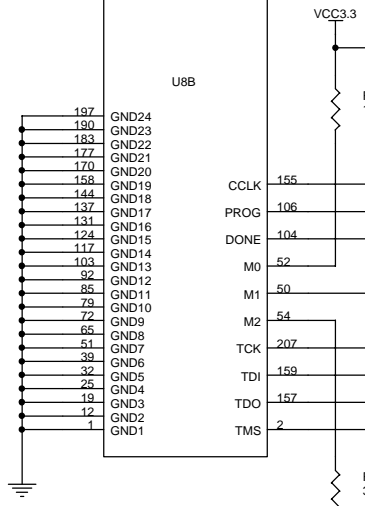
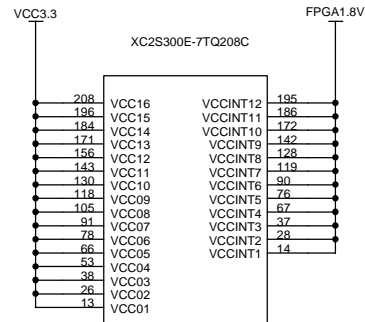
EXTERNAL MEMORY INTERFACE DAUGHTER CARD CONNECTIONS



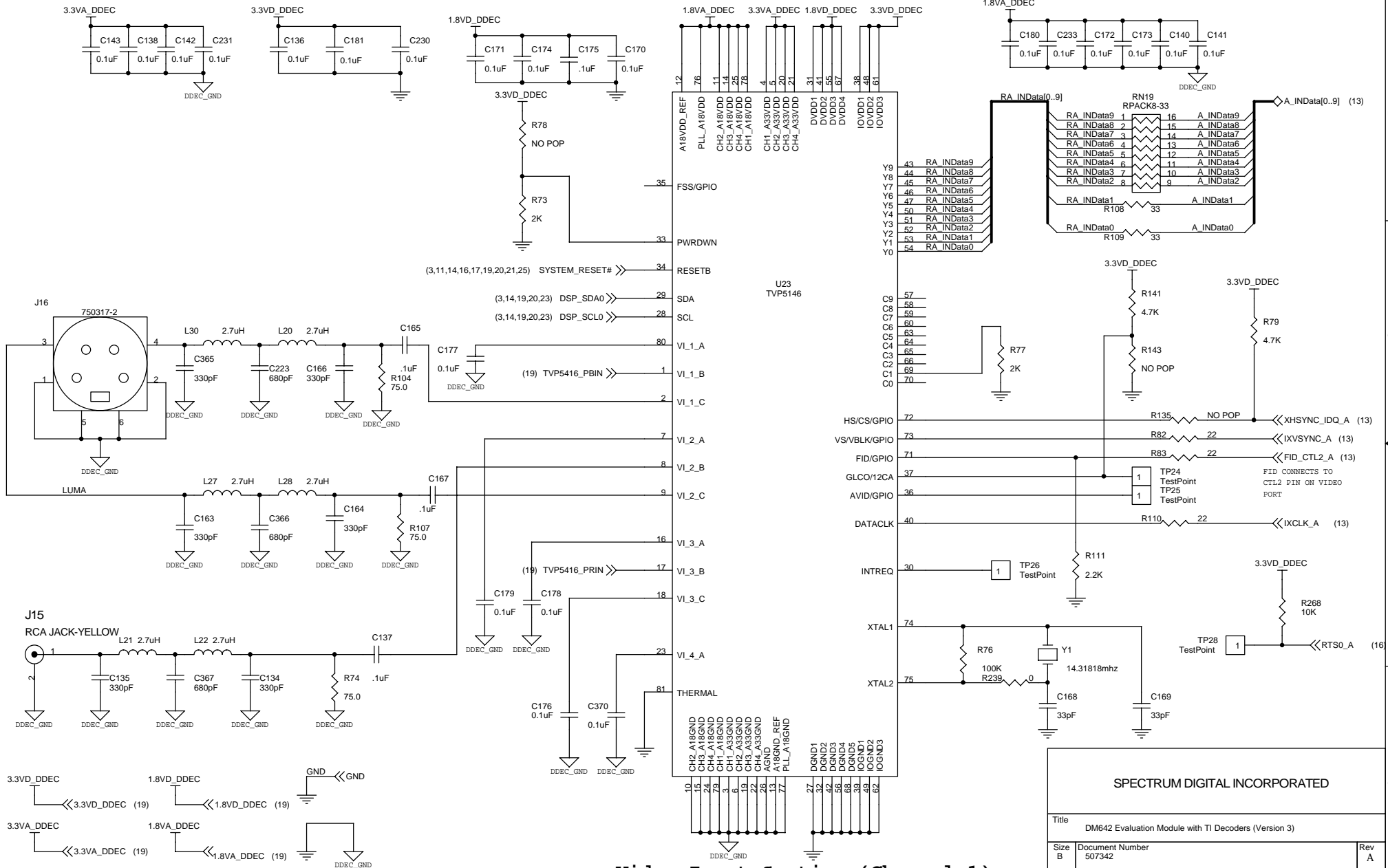
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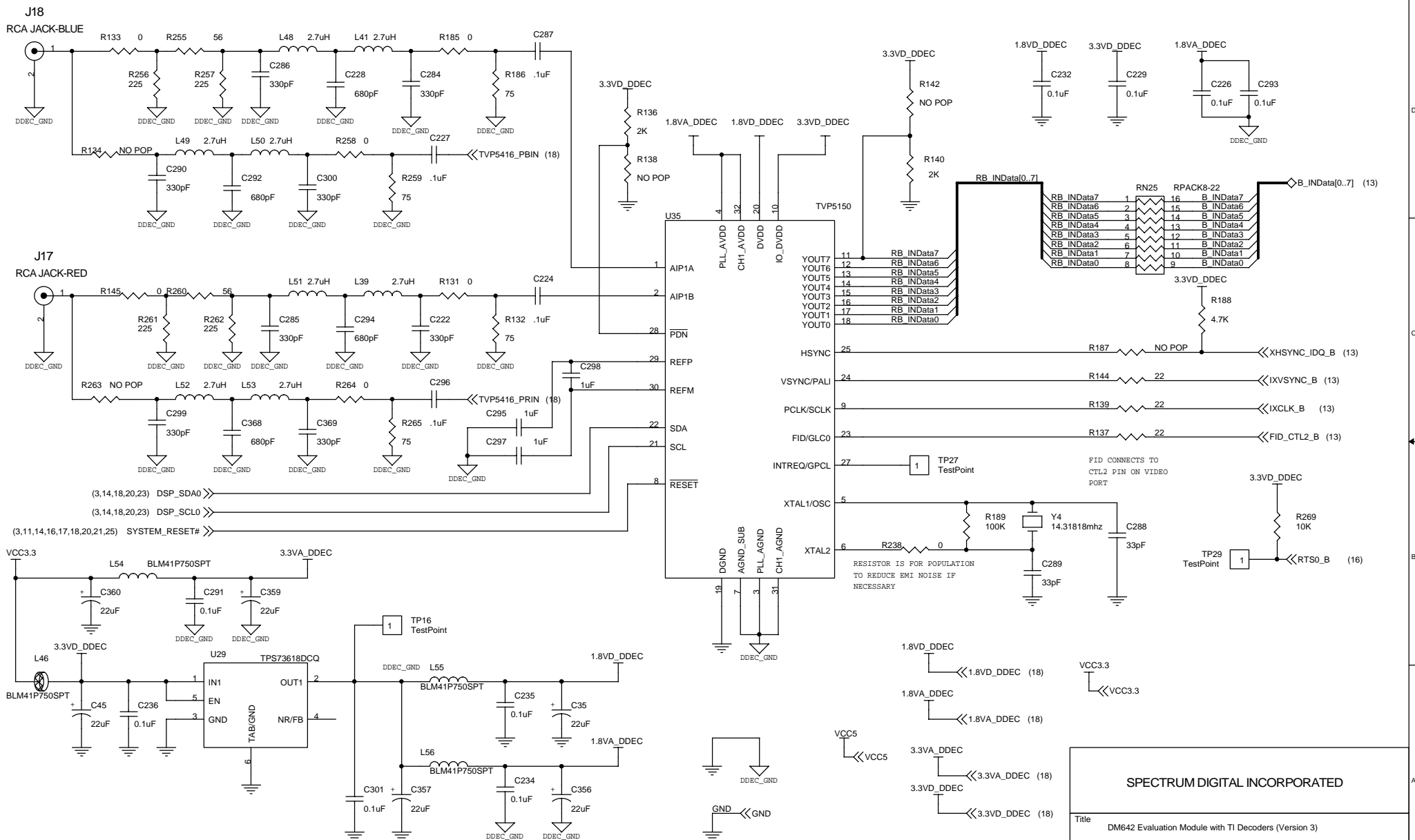


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Video Input Section (Channel 1)

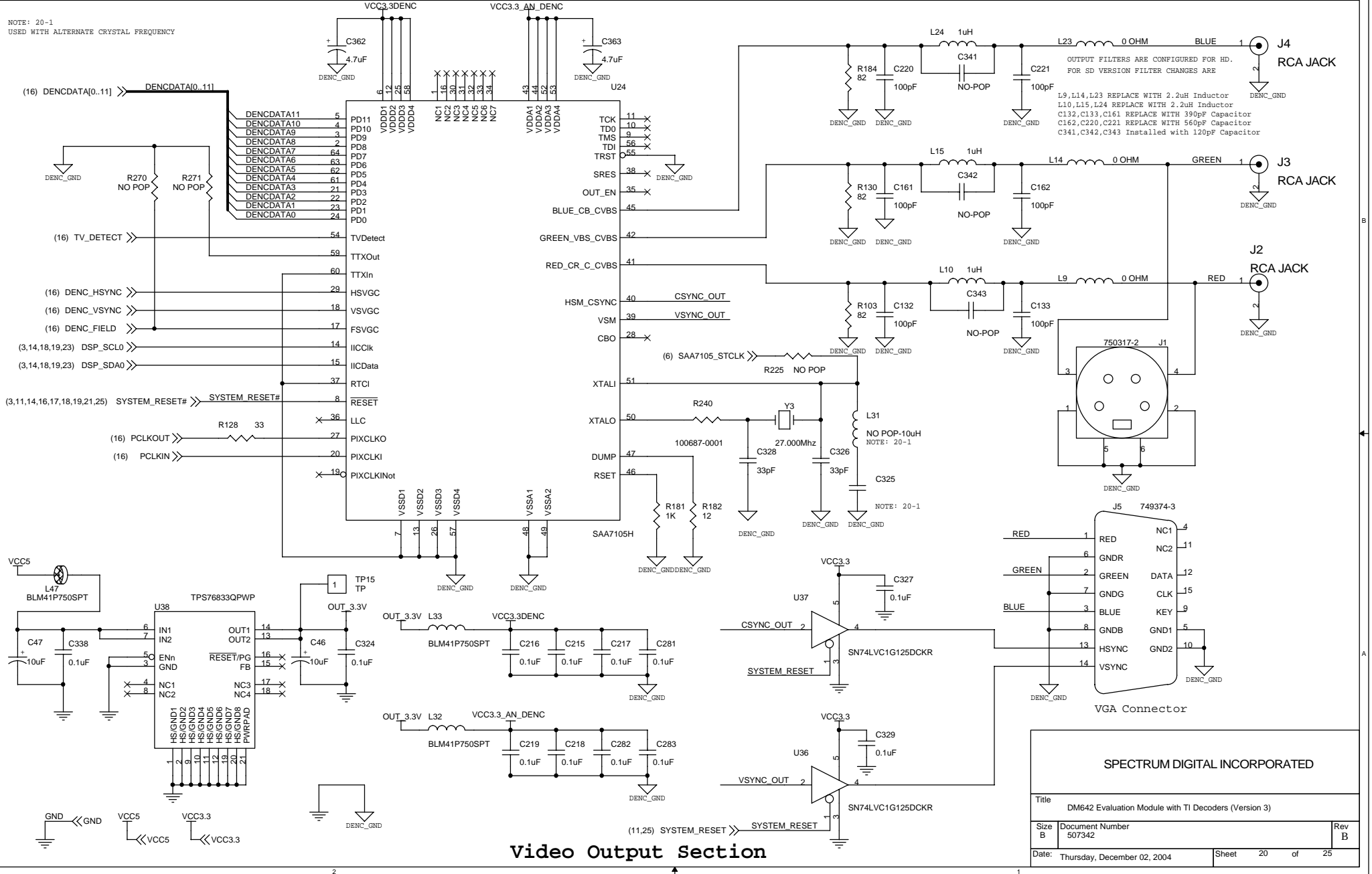
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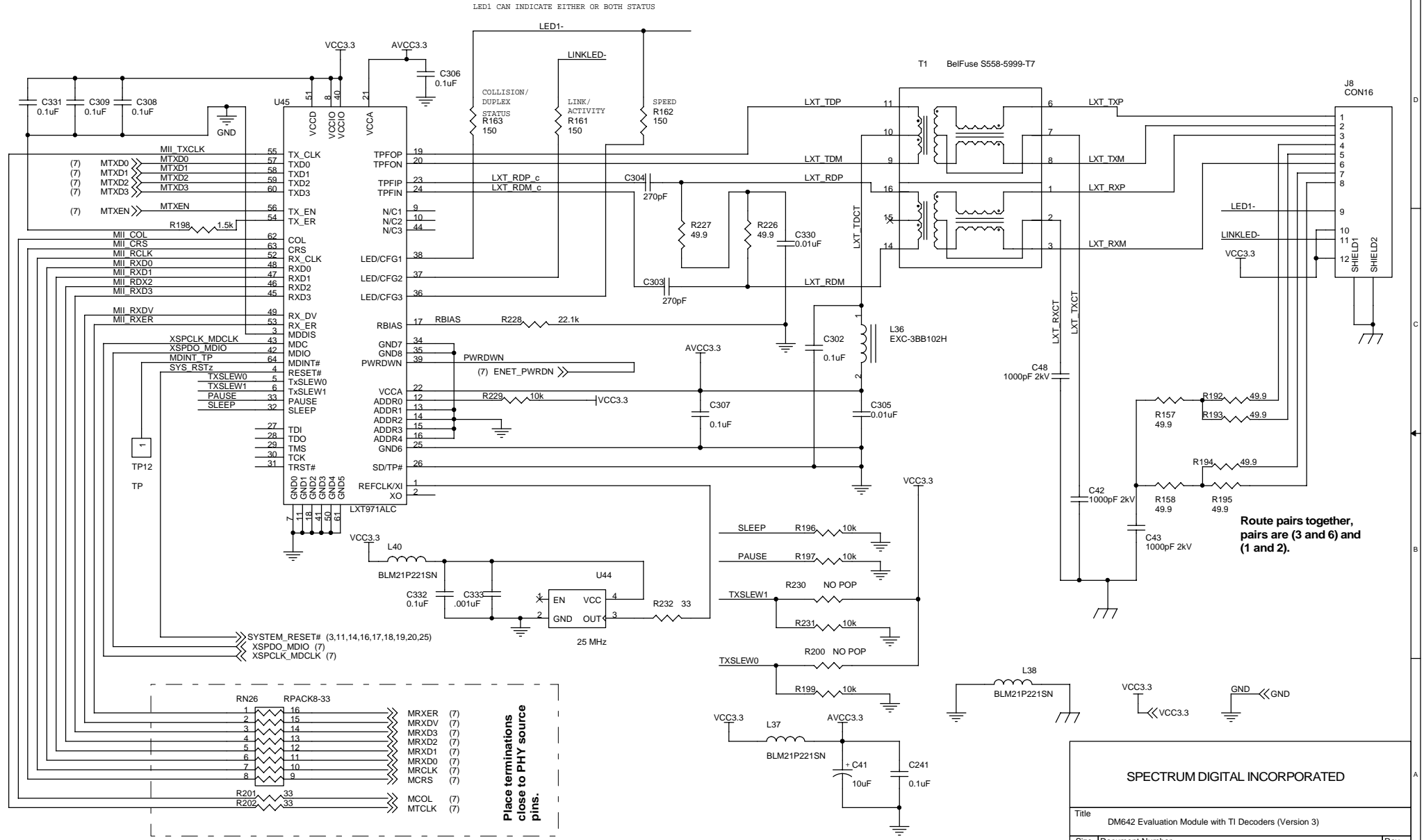
Video Input Section (Channel 2)

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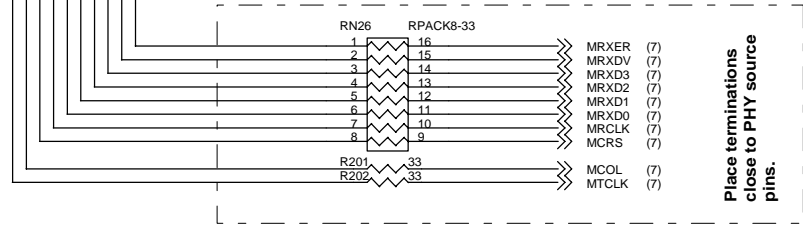
NOTE: 20-1
USED WITH ALTERNATE CRYSTAL FREQUENCY



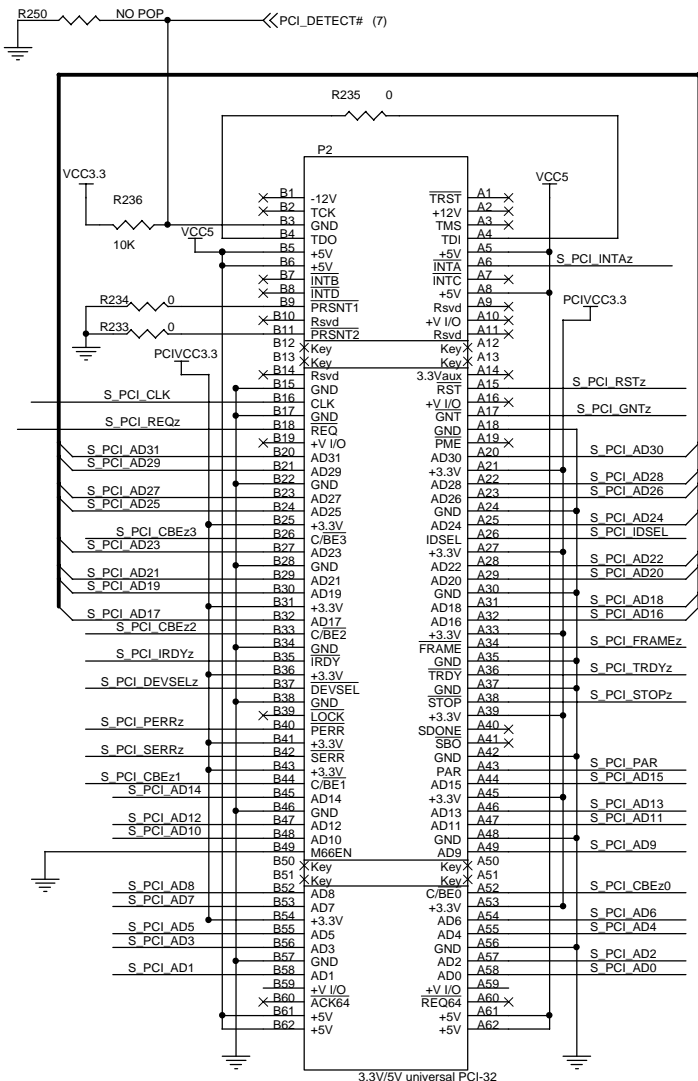
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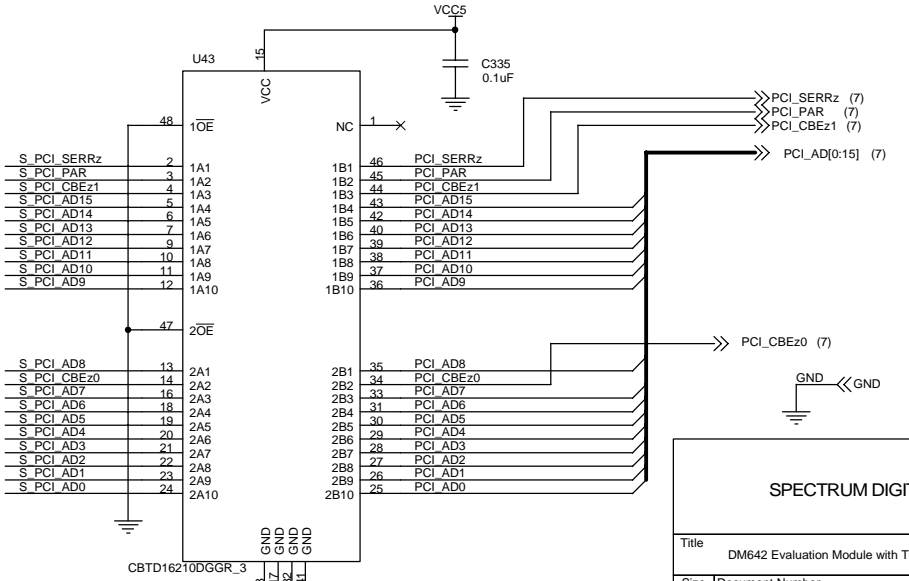
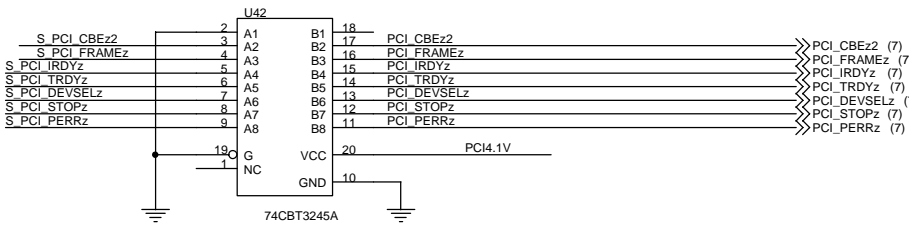
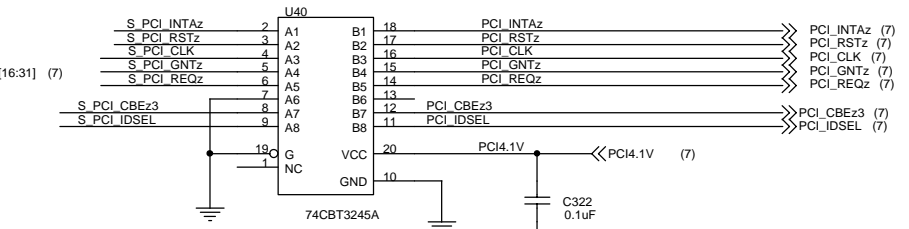
ETHERNET PHY AND INTERFACE



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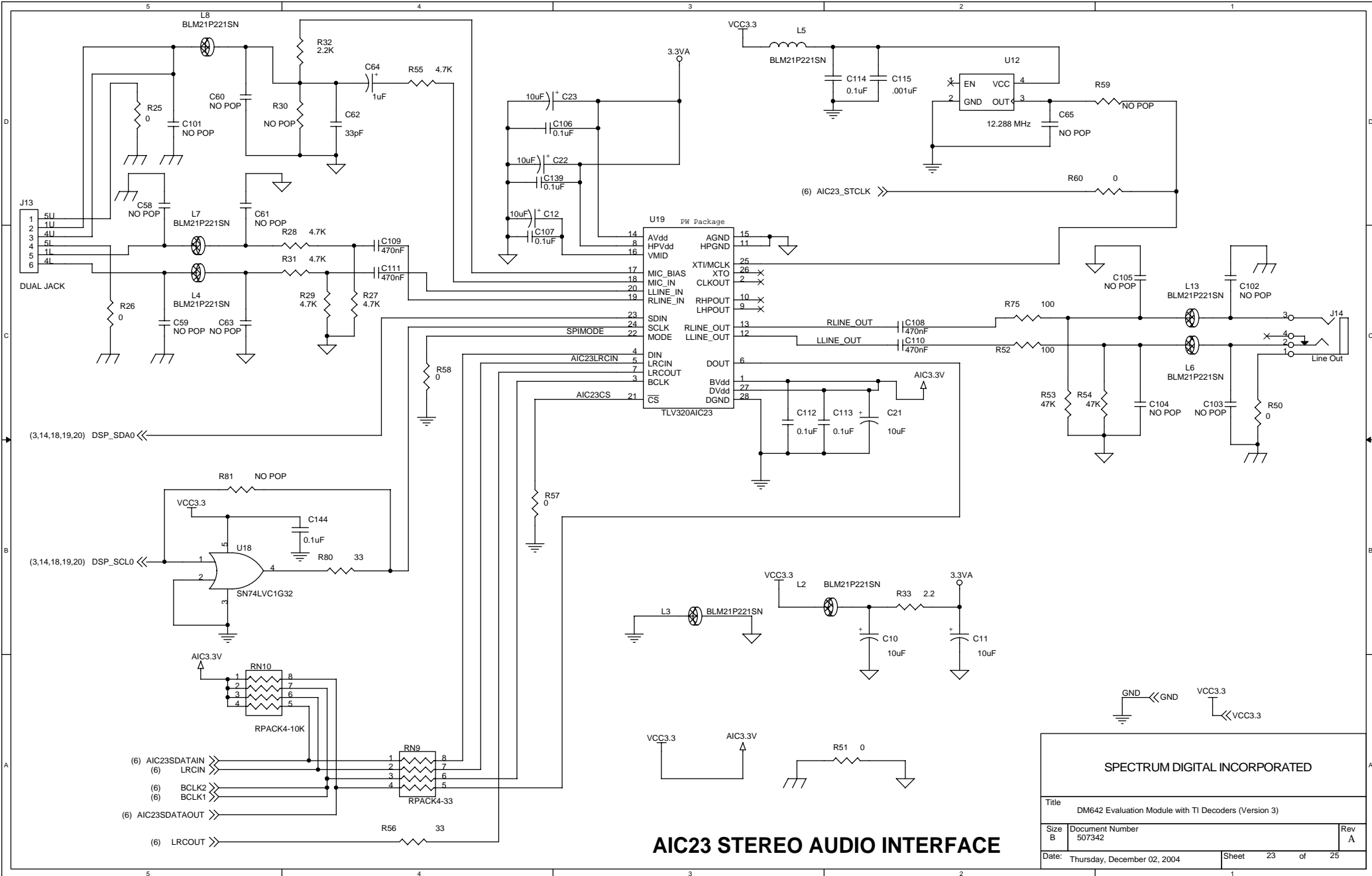
PCI INTERFACE



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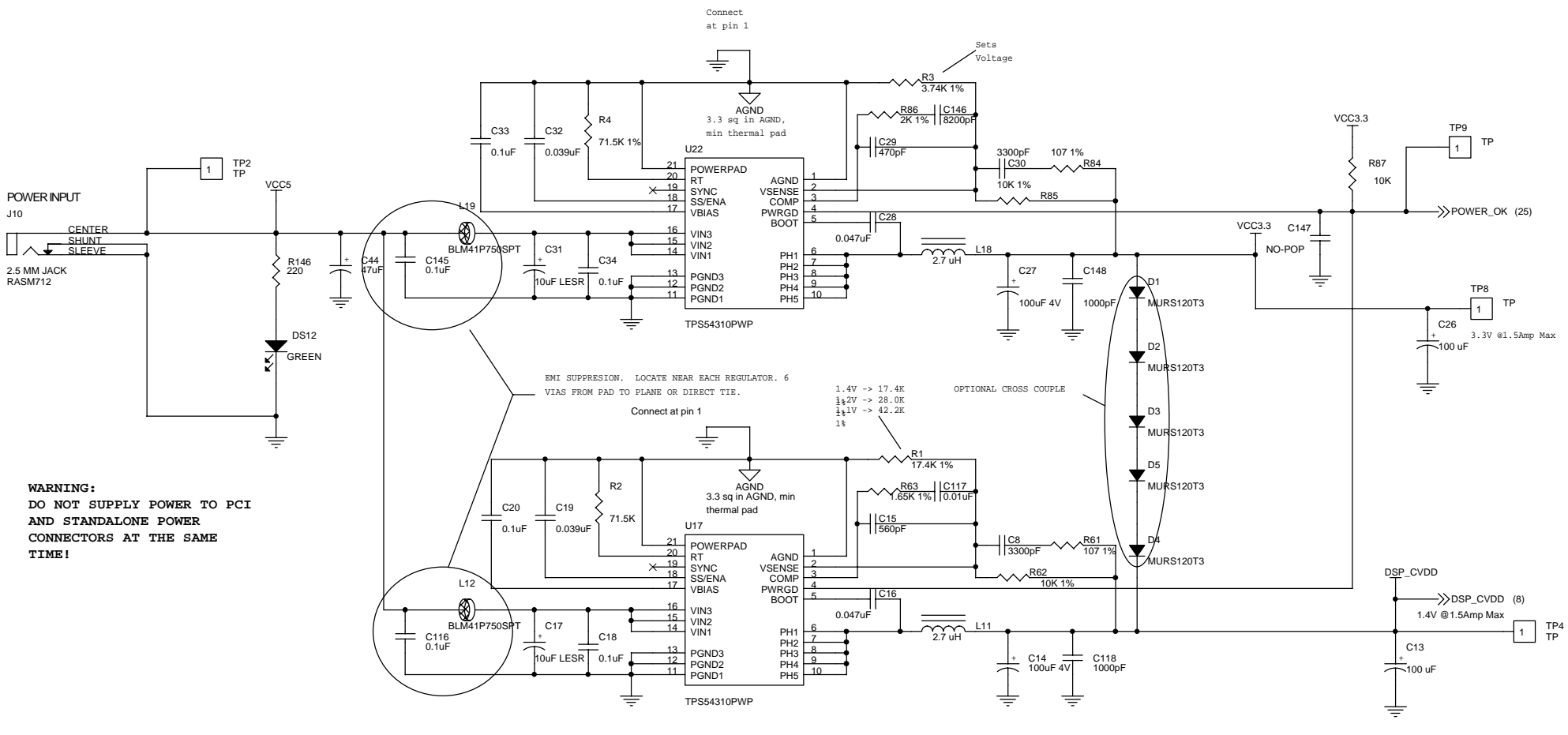
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AIC23 STEREO AUDIO INTERFACE

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WARNING:
DO NOT SUPPLY POWER TO PCI
AND STANDALONE POWER
CONNECTORS AT THE SAME
TIME!

POWER ESTIMATES BASED ON SPRU190

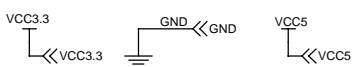
1.4V@600MHz	1.09 W	0.778A
3.3V@600MHz	0.52 W	0.157A (no emif clk)

MEASURED CURRENT ON C6416TEB, ~0.7A@5V

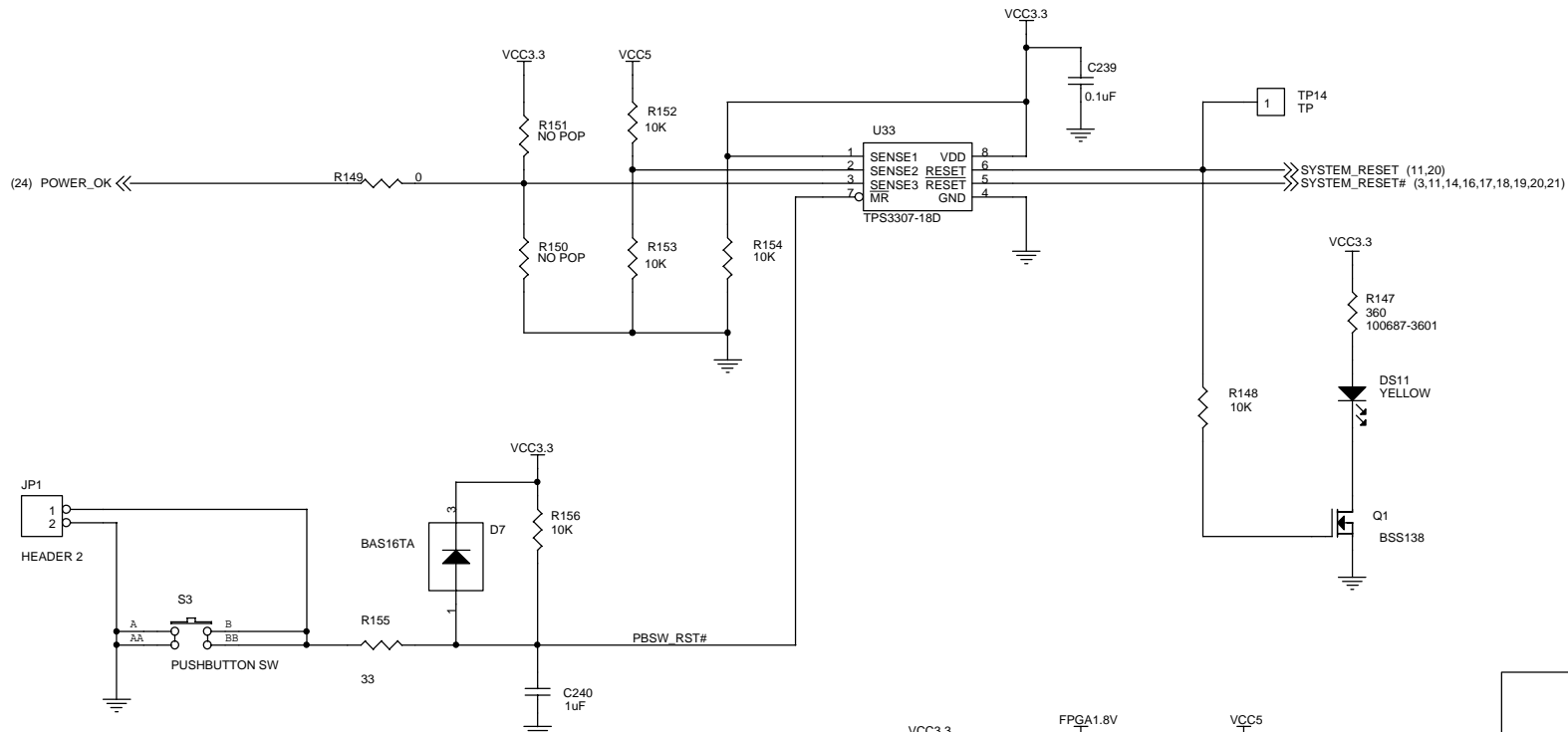
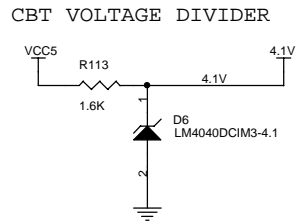
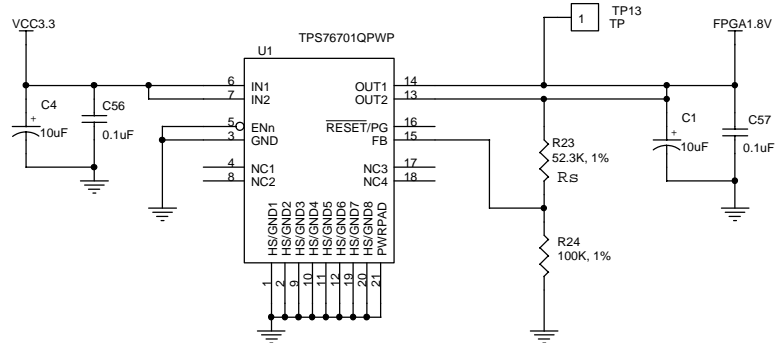
EACH REGULATOR CAN SUPPLY UP TO 3A OF CURRENT. HOWEVER COMPONENT VALUES HAVE BEEN SELECTED FOR 1.5A OPERATION.

VALUES CALCULATED WITH SWIFT DESIGN TOOL 2.0. FOLLOW TPS54310 EVM LAYOUT

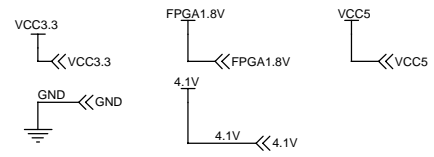
POWER



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FPGA POWER AND RESET CIRCUITRY



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